Mixed-Signal Design of a Digital Input Power Amplifier for Automotive Audio Applications

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Abstract

With reference to digital input power amplifier for automotive audio applications, the paper presents an exhaustive exploration of the huge mixed-signal space to find optimal trade-offs among different cost-functions: distortion, efficiency, circuit complexity and sensitivity. Different architectural solutions are modelled and compared in a Simulink/Spice framework. All building blocks (i.e. oversampling filter, noise shaping, type of PWM modulation, type of feedback, power stage, LC filter) are optimized considering the whole system performance. A novel mixed-signal scheme is finally derived and prototyped.

1. Introduction

The audio amplifiers market for automotive entertainment is characterized by the demand of small size and high efficiency schemes. Linear amplifier topology has been dominant for the last half century due to its low distortion performance but the achievable power density is limited by the physical size and costs of cooling hardware and power devices. With respect to the market need linear amplifiers are too heavy and dissipate too power. Particularly for booster amplifiers with output power in the range of 40-50 W or higher, switching drivers are the best suited solution [1]. Several switching-based schemes, class D PWM amplifiers, or hybrid class A-D or B-D ones have been proposed in the literature [2-4] to achieve roughly the same low-distortion performances of linear amplifiers but with a higher power efficiency and hence smaller size and cost. However the schemes proposed in [2-4] are analog amplifiers while, nowadays, most of audio and speech sources are digital: e.g. CD and DVD supports, MP3 files, Digital Audio Broadcasting radio. A Digital to Analog converter, optimized for at least 16-bit CD-quality PCM signals, has to be inserted before the analog amplifier; this increases size, cost and sources of noise/distortion of the overall digital audio system. An alternative promising solution is a direct amplification of the digital source based on the switching architecture in Fig. 1: a digital processing circuit converts the PCM signal in a PWM one which is amplified by an inverter power stage and then provided to the speaker after low-pass LC filtering. The aim is integrating all the processing part in a single chip while using discrete off-chip components only for the output transistors and LC filter [1]. Based on such topology several architectures can be devised with different tradeoffs between circuit complexity and performance in terms of distortion, power efficiency and sensitivity to parameter changes. Specific solutions have been proposed by academia or industry [1, 5-8, 10] but they focus on the optimization of one main cost function, mainly distortion in academia [6,10] or efficiency in industry [5]. An exhaustive exploration of the whole mixed-signal design space to find an optimal trade-off among all the cost-functions (distortion, efficiency, circuit complexity and sensitivity) is still missing and will be addressed in this paper. In Section 2 several possible implementations of the basic scheme in Fig. 1 are proposed and modelled in a Simulink/Spice environment. Section 3 details specific optimizations for each building block of the above architectures as oversampling filter, noise shaping, type of PWM modulation, type of feedback, inverter power stage and LC filter. Architectural comparison results are showed in Section 4. The selected optimal architecture is then implemented using commercial Power MOS for the power stage [9] while the digital part, through an HDL semi-custom flow, is synthesized on FPGA. Conclusions are drawn in Section 5.

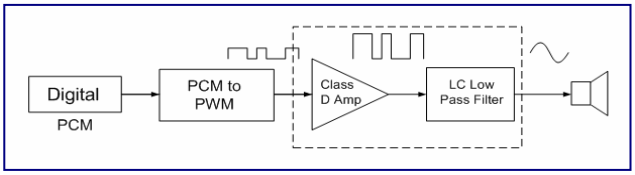

Fig. 1: Digital input power audio amplifier

2. Mixed-Signal Architecture

A direct conversion of the 16-bit 44.1-KHz PCM stream to PWM, as in Fig. 1, is not a good choice. An oversampling unit and a noise shaper have to be added before the PCM to PWM converter. If the PWM carrier frequency is 44.1 KHz as the original PCM then the output LC filter has to guarantee a -3dB pass-band of 20 KHz removing all the other spectral components which start to be significant from 44 KHz. Such specifications are hard to achieve at low cost for a LC power filter. The analog filtering specifications can be released working with an oversampled (↑M factor in Fig. 2) PCM signal and hence with a much higher (↑M) PWM carrier frequency. The higher is the factor M, the larger is the transition band for the analog filter but also the higher is the complexity increase for the digital part. Moreover, when converting the 16-bit oversampled PCM signal to PWM the minimum impulse time is $1/(44100 \cdot M \cdot 2^{16})$ sec and the maximum frequency is its inverse $2.89 \cdot M$ GHz. To reduce such time and frequency requirements while

still using oversampling and keeping the CD audio quality, a noise shaper has to be added. This unit can reduce the used bits, e.g. from 16 to 8 with a decrease of time and frequency requirements to roughly (88.6/M) ns and 11.89·M MHz, while the added quantization noise can be spread outside the audio band. The noise shaping performance depends on the order and hence the complexity of the shaping filter. From the above discussion it clearly emerges that the optimal amplifier design can be achieved only after an exhaustive exploration of the mixed-signal design space with a trade-off between different requirements. Such considerations also refer to the other building blocks of the architecture in Fig. 1. PWM can be 2 or 3 states. In 2-state PWM the signal is switching between maximum and minimum supply voltage values, the two states V^+ and V^-. Even for low-level signals binary modulation continuously provides energy to the filter and the load. If the modulating input is null the PWM wave is still switching with a 50% duty cycle. The signal provided to the load is null but switching losses are paid thus reducing power efficiency. The 3-state PWM signal switches between V^+ and 0 when the input signal is positive, otherwise between V^- and 0. In case of null input there is no switching activity and hence switching losses are reduced. 3-state PWM reduces by a factor 2 the voltage swing supported by the power MOS allowing also the reduction of electromagnetic interference and a better behaviour of the power devices. However the increased number of states leads to an increased complexity for the digital 3-state PWM modulator. As far as feedback topology is concerned different approaches can be adopted. Some architectures proposed in the literature implement open loop amplifiers [5] avoiding the problem of how to reinsert the power output signal in the low-power digital processing chain. Other works, to reduce sensitivity and distortion, reinsert the pre-filtered output PWM signal according to a mixed signal feedback scheme [6,10] or they just take into account the sign of the output current implementing a simple 1-bit digital feedback [7]. To explore such huge mixed-signal design space tens of different architectures have been modelled, simulated and compared in a Simulink/Spice frame-work. Simulink models permit a rapid design, test and comparison of mixed-signal schemes. To keep a good comparison accuracy the Simulink models for the power stage have been verified vs. their Spice models. For sake of space this paper describes and compares just the four more representative schemes (AD, AD1, AD2 and AD3 in Fig. 2) to understand the different optimizations and trade-offs carried out. All of them share the same oversampling and noise shaping units described in Section 3.1. AD and AD3 implement open loop 2- and 3-state PWM schemes with automatic dead time insertion. AD-2 is a 2-state PWM with dead time compensation (DTC) by a 1-bit digital feedback. AD-1 is a 2-state PWM with a mixed signal feedback scheme called PEDEC (Pulse Edge Delay Error Control) [6]. With respect to [6], a more complex mixed-signal feedback correction scheme has been proposed in [10] promising a higher rejection of power stage non-linearity. The scheme in [10] refers to a multi chip implementation of the signal processing part: one chip for the digital circuitry and another, also including a 7-bit flash ADC, for the mixed-signal feedback correction. Being too complex vs. the consumer-market need the scheme in [10] is not consider in the comparison.

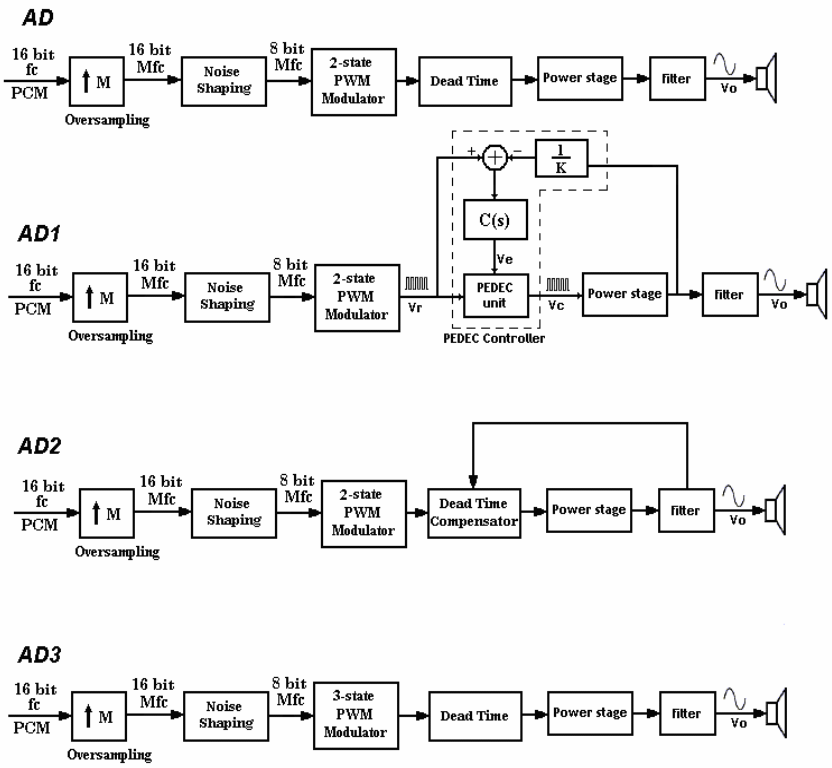

Fig. 2: Mixed signal architectures for digital audio amplifier

All reported simulations refer to the case study of max 70 Wrms (or 35 Wrms) power delivered to a 4 Ohm (or 8 Ohm) speaker. After defining in the Simulink/Spice environment all optimizations and trade-offs the final system design can be carried out as a PCB (printed circuit board) implementing the digital part with a FPGA and the power stage [9] and LC filter by discrete devices. The high power efficiency achieved permits to work with 70 Wrms output without extra cooling hardware or specific PCB layout tricks.

3. Circuit Design Optimizations

3.1 Oversampling and Noise Shaping

Oversampling by a factor M is realized first inserting M-1 zeros after each original sample (zero padding) and then filtering the new stream with an interpolating filter

to remove high frequency spurious repetitions of the baseband signal. As stated in Section 2 the factor M and the type of interpolating filter have to be determined as a trade-off between released specification for the LC output filter and increased complexity for the digital part. Thanks to the Simulink/Spice system model we determined a good trade-off using M=8, thus creating a 352.8 KHz PCM signal. As concerns the interpolating filter the minimization of signal distortion, i.e. the elimination of zero-padding signal replica with no phase distortion, can be achieved with a 196th-order FIR filter. Such solution is too expensive and in the literature alternative solutions, e.g. a 7th-order IIR elliptic filter in [8], can be found. In this case phase shift problems arise. Moreover the above filters use 32-bit floating point coefficients. Analyzing the system performances in our Simulink/Spice environment we have designed a 32th-order FIR filter which implements with 12-bit fixed-point coefficients a low-pass hamming window and leads to negligible distortion increase vs. the optimal value of the 196th-order FIR. As concerns noise shaping its circuit scheme is reported in Fig. 3 reducing the used bits from 16 to 8. Since the oversampling factor is M=8 then the output circuitry works with a minimum impulse time of 88.6/M=11 ns. The noise transfer function (NTF) in Fig. 4 depends on the digital filter H(z). The trade-off between complexity of the shaping filter and SNR of the output audio signal has been achieved using a 5th-order integer-coefficient FIR being:

$$NTF = \frac{Ens(z)}{Erq(z)} = H(z) - 1, \quad H(z) = 1 - (1 - z^{-1})^5$$

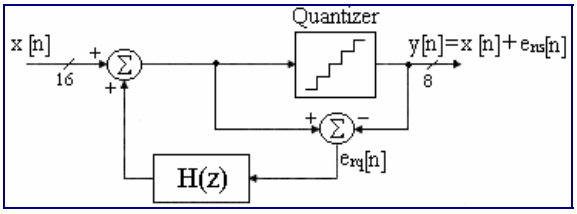

Fig. 3: Noise shaping circuit

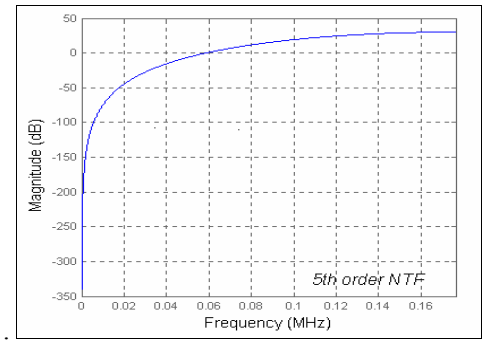

Fig. 4: Noise transfer function

3.2 PCM to PWM Conversion and Power Stage

To generate a 2-state PWM digital wave, i.e. to generate in Fig. 5 the time intervals where the wave is high or low, each 8-bit sample of the noise shaped and oversampled PCM stream is compared to a digital saw-tooth waveform. 3-state PWM modulation is realized using two 2-state PWM modulators, one for positive input samples and the other for negative samples: after controlling the sign of each sample only one of the two 2-state modulators is enabled.

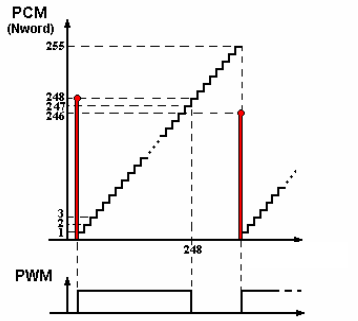

Fig. 5: PCM to PWM converter

3-state PWM modulation doubles the cost of the 2-state one but the complexity of the whole system is comparable. Indeed, as showed in Section 4, the overall digital circuitry complexity is dominated by the noise shaping and oversampling filters which are common to 3- and 2-state PWM. To be noted that before driving the power stage, proper guard intervals have to be inserted at the beginning and end of each PWM word to take into account the switching delay time of the selected power MOS devices. The minimal time resolution of the PWM wave is 11 ns, determined by the oversampling and noise shaping choices, which is smaller than the switching transition time of typical power MOS, 20 ns for our selected devices [9]. If the time guard intervals are not inserted, PWM words with duty cycles of few % or near 100 %, (i.e. with high or low time intervals of tens of ns), can't be correctly managed by the power stage and hence distortions will arise. Moreover, since the switching on and off times of P and N MOS are not the same, for each transition of the PWM signal there is the risk of short-circuits between the voltage supplies (a MOS is already on while the other is not completely off). To avoid this power wasting phenomena extra dead time intervals have to be inserted when the PWM wave is switching. On the other hand the higher are the inserted time guard and dead time intervals, the higher is the reduction of the amplifier dynamic range. An optimal trade-off can be found by simulating in the Simulink/ Spice environment all the amplifier including also the power MOS time response. As example, Fig. 6 shows for AD3 the % total harmonic distortion (THD) vs. the time guard value tg: distortion is minimized using a 40 ns tg.

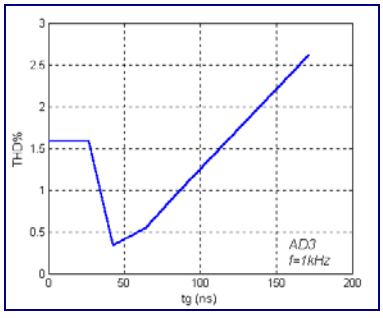

Fig. 6: THD vs. time guard tg

Fig. 7 reports the schematic of the full bridge power stage using power MOS from [9]. The LC filter is a 4th-order Butterworth with 20 KHz cut-off. To be noted that the higher is the target output power, the more convenient is a power-bridge solution based only on NMOS vs. a complementary NMOS/PMOS one as in Fig. 7. In the former a NMOS plus a charge-pump based gate driver is used instead of the PMOS transistor.

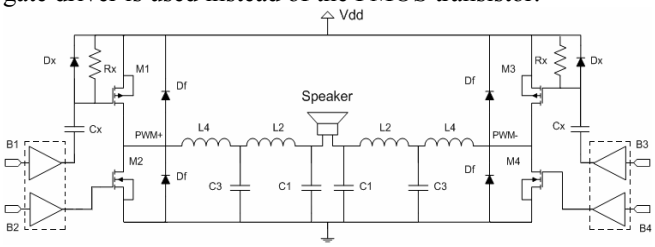

Fig. 7: Full bridge power stage schematic (Vdd=25V, digital input levels 0 and 5V)

3.3 Feedback Topology

In the above approach, implemented in AD and AD3, the PWM wave is modified according to an open loop topology to minimize distortion and power wasting due to non-ideal behaviour of the power stage. Open loop configuration is optimized by simulating the whole mixed-signal scheme, but if a circuit parameter changes there isn't a compensating mechanism. Several works in the literature adopt a feedback topology to reduce the system sensitivity to parameter changes. Among them, two techniques provided good results when applied to our case study. The first, realized in AD1, compares the output wave of the PWM modulator (Vr in AD1 in Fig. 2) with a scaled version of the power output PWM signal. Their difference is sent to a low-pass analog controller, C(s), extracting the DC component of the error. The error level Ve is then used in the PEDEC unit to proper insert time delays in the PWM modulator thus driving the power stage with a corrected PWM signal, Vc in Fig. 2. This approach provides good results, see Section 4, but is not useful for a low-cost realization since requires an analog feedback network. A simpler feedback correction is proposed in [7]. The sign of the output current provided to the load is used as 1-bit control to check which output transistor is on and to change consequently the dead time value. As proved in Section 4, this simple control is effective to reduce the amplifier sensitivity to parameter changes. In [7] it has been proposed only for 2-state PWM. In this work this approach has been redesigned for 3-state PWM creating a new scheme: AD4, 1-bit feedback extension of the open loop AD3.

4. Architecture Trade-offs and Prototype

4.1 Architectural Comparisons and Trade-offs

With reference to max 70 Wrms on a 4Ohm load, Fig. 8 shows the achieved results in terms of power efficiency and THD+N (plus noise) for the different architectures. The best power efficiency is achieved by AD3 reaching 97% in the range 20 to 70 Wrms. With such high efficiency the power devices of the full bridge are dissipating less than 0.5 W avoiding extra cooling hardware. These results outperform classic DAC plus analog amplifier solutions (e.g. using the hybrid analog scheme in [4] the max. efficiency is below 77%). AD and AD2, 2-state schemes with open loop and 1-bit feedback topologies, achieve the same AD3 efficiency only for high power levels. For small signals the 2-state PWM schemes dissipate power with an efficiency reduction of 20% vs. the 3-state. Comparing AD2 and AD1 it emerges that the 1-bit digital feedback doesn't affect efficiency while PEDEC mixed-signal feedback reduces the efficiency. As concerns THD+N, AD1 and AD3 achieve the best results while AD the worst.

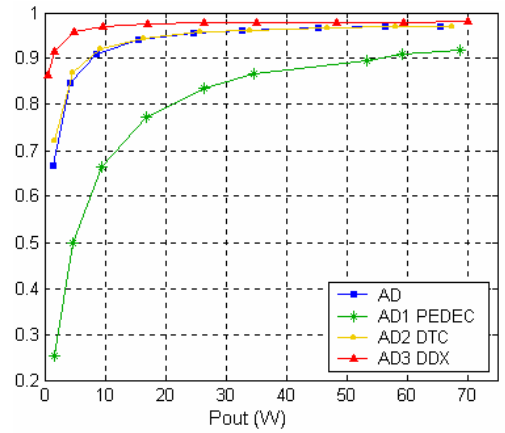

Fig. 8: Architectural comparison, power efficiency vs. Pout

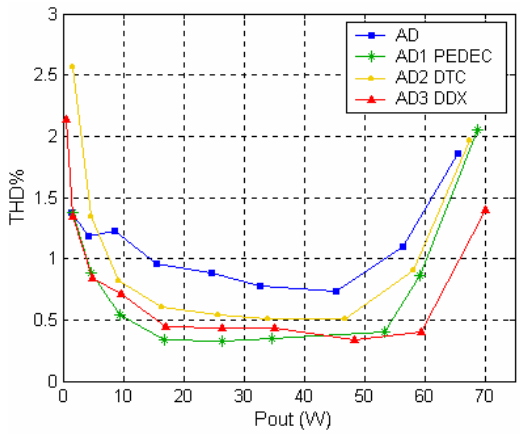

Fig. 9: Architectural comparison, THD+N vs. Pout

Comparing AD1, AD2 and AD3 vs. AD proves that using mixed-signal or 1-bit feedback topology or using 3-state PWM all contribute to distortion reduction. The best distortion-efficiency performances are achieved by AD3. Such results are due to the many simulations carried out that allowed for an optimal tuning of all analog/digital design parameters. However, if a parameter changes there isn't a compensating mechanism. The sensitivity of the electronic system to parameter changes is an important figure of merit in the automotive environment which is characterized by high temperature range variations, EMI and EMC problems,

power supply ripple. As example, Fig. 10 shows how the THD+N results degrade in AD3 and AD2 when the output load changes to 8 Ohm. It emerges the high sensitivity of AD3 vs. AD2.

This is why we devised a new architecture, AD4: after the optimized oversampling and noise shaping units described in Section 3.1, the PCM signal is converted in a 3-state PWM wave with 1-bit dead time compensation driving the full bridge power stage of Fig. 8. AD4 outperforms know schemes featuring the same good efficiency and distortion of AD3 but with a reduced sensitivity, as in AD2.

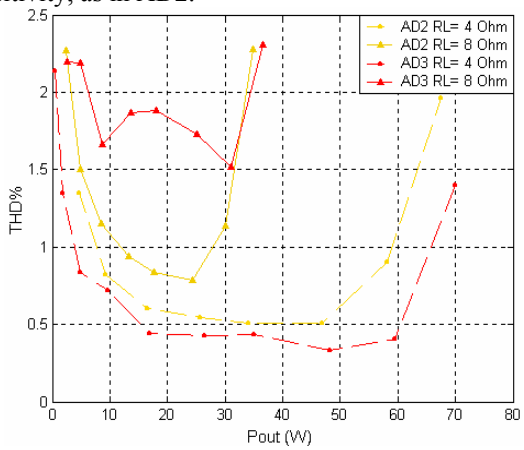

Fig. 10: Architecture sensitivity example, THD+N vs. load

4.2 Implementation of the Digital Input Power Audio Amplifier

The digital processing part of the digital input power audio amplifier has been implemented through a semi-custom HDL flow. Synthesis results in a 0.18 um CMOS standard-cells technology show that the digital complexity is 11 and 10.7 Kgates for a 3- and 2-state scheme respectively. The modulator cost is only 5% while 12% and 82% are due to noise shaping and oversampling. The digital part has been implemented in a Xilinx Virtex V100 FPGA: 89% of resources used with a power cost of 100 mW.

To assess the flexibility of the digital amplifier idea and of its mixed-signal design another configuration, reported in Fig. 11, has been implemented for a 1 channel at 45 Wrms with CD-quality input: it uses Altera FPGA technology for the digital part and a 3-state PWM full-bridge NMOS configuration for the power stage.

5. Conclusion

The design of digital input power amplifiers for automotive audio applications is presented in the paper. An exhaustive exploration of the huge mixed-signal design space is carried out to find optimal trade-offs among different cost-functions: distortion, efficiency, circuit complexity, sensitivity. Different architectures are modelled and compared in a Simulink/Spice framework and their building blocks (noise shaping, over sampling, PWM modulator, feedback topology, power stage and LC filter) are carefully optimized considering the whole system performance. A novel mixed-signal scheme is finally derived and prototyped in a PCB design using discrete power MOS for the power stage while the digital part is synthesized on a low-complex FPGA.

Acknowledgments

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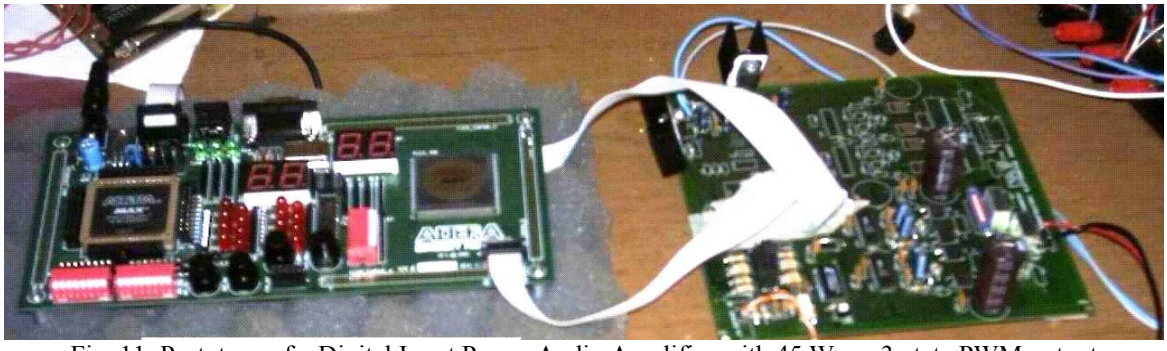

Fig. 11: Prototype of a Digital Input Power Audio Amplifier with 45 Wrms 3-state PWM output