A Fast-Lock Mixed-Mode DLL with Wide-Range Operation and Multiphase Outputs

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Abstract

This paper describes a fast-lock mixed-mode delay-locked loop (MMDLL) for wide-range operation and multiphase outputs. The architecture of the proposed DLL uses the mixed-mode time-to-digital converter (TDC) scheme for frequency range selector, a start-up circuit and coarse tune circuit to offer the faster lock time. And the multi-controlled delay cell for voltage-controlled delay line (VCDL) was used to provide the wide locked range and low-jitter performance. The charge pump circuit is implemented by digital controlled scheme to reach bandwidth tracking. The chip has been fabricated using the TSMC 0.25-μm single-poly five-metal CMOS process with a 2.5 V power supply voltage. From the measurement results, this DLL can operate correctly when the input clock frequency is changed from 32 to 320 MHz and generate ten-phase clocks within just one clock cycle. Moreover, the proposed DLL can solve the problem of the false locking associated with conventional DLL's and wide-range operation. At 320 MHz, the measured peak-to-peak jitter and root-mean-squared jitter are 37.2 ps and 2.492 ps, respectively. Furthermore, the locking time is less than 22 clock cycles based on the HSPICE simulation results. The DLL occupies smaller area (0.32×0.22 mm^2) and dissipates less power (15 mW) than other wide-range DLL's [1] ─[7].

1. Introduction

For high-speed and high-integration density VLSI systems, the phase-locked loops (PLL's) and delay-locked loops (DLL's) have been widely adopted to solve clock signal skew and jitter in microprocessors, memory interfaces and communication IC's. Generally, if there is no need for frequency multiplication, DLL's would be more attractive than PLL's because they are more stable and easier to implement together with digital circuits and exhibit better jitter accumulation characteristics than PLL's. Therefore, the DLL's offer better jitter performance than PLL's [1] [2]. In many DLL applications, such as high speed clock/data recovery (CDR), DDR [7] and multiphase clock generation, the multiphase VCDL output is usually used to implement the circuit function.

Conventional DLL's may suffer from harmonic locking over wide operating range. Therefore, various wide-range DLL's architectures [1]─[7] are proposed to overcome the problem of false locking. However, such DLL's resulted in complex architectures that faced such problems as increased area, added power consumption and degradation of jitter performance. According to the previous works, a mixed-mode architecture, which increases the lock range having no degradation of jitter performance with a relatively small overhead in area and power, is proposed in this paper.

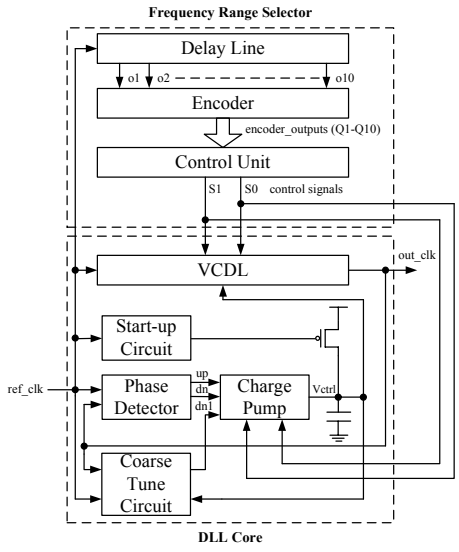


Figure 1: Block diagram of the proposed DLL.

2. Architecture

2.1 Architecture and Operating Principle of Proposed DLL

The architecture of the proposed DLL is shown Fig. 1. It has two major blocks, the frequency range selector and DLL core. The frequency range selector can detect the input frequency range and generate digital control signals (S1, S0) to switch the delay time range of the multi-controlled VCDL and charge pump for tuning the loop bandwidth. The digital-mode control scheme for range selector and the flat gain of the VCDL not only offer the faster lock time and wide locked range but also provide a low-jitter performance for various frequency application. The other block is DLL core that consists of PD, CP, LF, start-up circuit, coarse tune circuit and the multi-controlled delay line for VCDL. The start-up circuit sets the initial control voltage of the loop filter to VDD. On the same time, the coarse tune circuit is activated to generate a large discharge current until the output clock (out_clk) of the delay line is close to the input reference clock (ref_clk). Therefore, the coarse-tuning scheme can offer the faster lock time in this DLL.

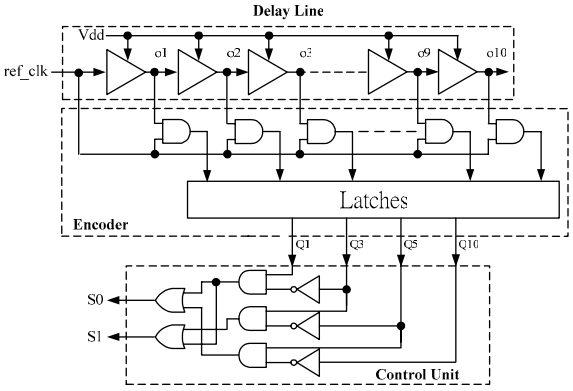


Figure 2: Circuit diagram of the frequency range selector.

2.2 Circuits Description

2.2.1 Frequency Range Selector

A time-to-digital converter (TDC) is a unit able to perform a time interval measurement and convert the result with a digital readout. In this DLL, the mixed-mode TDC scheme was applied as the frequency range selector. It generates 2-bit control signals (S1, S0) and thus switch the delay time range of the multi-controlled delay cell and the current of the charge pump to achieve adaptive bandwidth as shown in Fig. 2. The frequency range selector can choose the delay time range in the VCDL, according to the various input reference clock. The architecture consists of a ten-stage delay line, an encoder and a control unit. The circuit of the ten-stage delay line is similar to the multi-controlled delay cell which is used to avoid the process variation. The encoder and the control unit are composed of only latches and simple logic gates.

While the DLL is activated, the ref_clk will be propagated in the delay cell of the ten-stage delay line. The outputs (o1－o10) of the delay line will be AND with the ref_clk. The outputs (Q1,Q3,Q5,Q10) of the encoder are the digital value to describe the time interval in which the ref_clk is high, therefore, the frequency range of the input reference clock is determined. Four different operating ranges of this DLL are selected by the 2-bit control signals (S1, S0). For example, when the reference clock is 100 MHz, the outputs of the encoder are bit streams of "1110" and the 2-bit control signals (S1, S0) is (0, 1). When the input reference clock is 250 MHz, the outputs of the encoder are bit streams of "1000". Then the 2-bit control signals (S1, S0) is (1, 1). Based on the operating of frequency range selector, a wide operating range of this DLL is achieved.

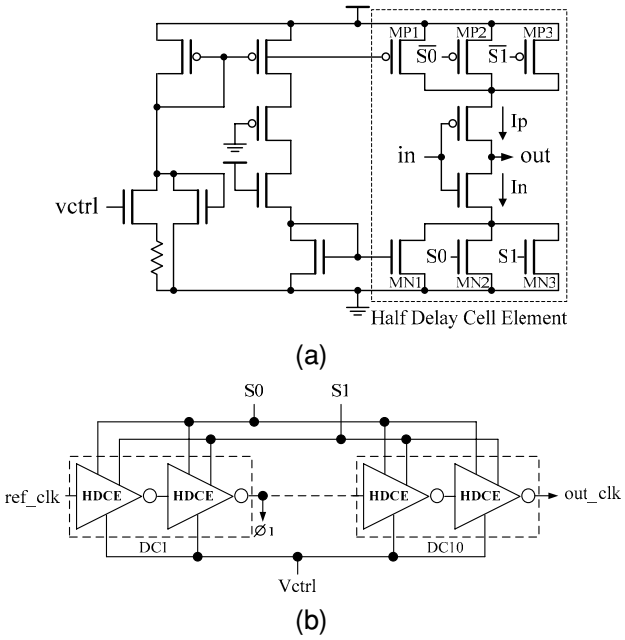


Figure 3: The multi-controlled delay cell (a) circuit diagram of HDEC and (b) configuration of ten-stage delay cell.

2.2.2 Multi-Controlled Delay Cell

In PLL's, a voltage-controlled oscillator (VCO) with a larger gain (K_{VCO}) is more prone to high spurs and phase

noise. One means of achieving simultaneously a large tuning range and small K_{VCO} is to divide a single wide-range tuning curve into several narrow-range sections with sufficiently frequency. In this DLL, a multi-controlled delay cell is proposed for the flat gain of the VCDL, to provide a wide operating frequency range and low-jitter performance. The multi-controlled delay cell is employed as the basic half delay cell element (HDCE) and two HDCE's compose a delay cell (DC), as shown in Fig. 3.

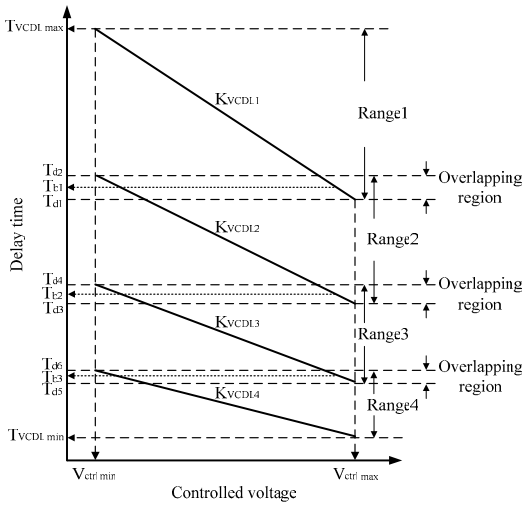


Figure 4: The principle of operating range of the proposed DLL.

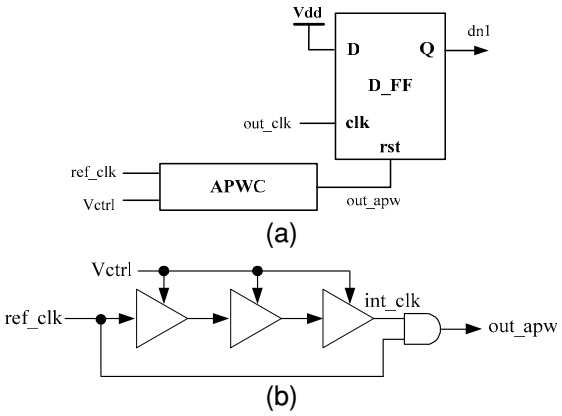


Figure 5: The schematic of (a) coarse tune circuit and (b) adjustable pulse width circuit.

The multi-controlled delay cell comprises four operating frequency ranges. Figure 4 shows the principle of operating range of the proposed DLL. The delay time ($T_{VCDL.max}$, $T_{VCDL.min}$ and T_d) of the multi-controlled delay cell is determined by three control signals V_{ctrl}, S0 and S1. In range1, the control signals (S1, S0) are (0,0), the operating range is between $T_{VCDL.max}$ and T_{d1}. In range2, the S0 is high and the S1 is 0; the operating range is between T_{d2} and T_{d3}, and so on. The mixed-mode wide-range DLL must design the boundary (T_b) of the delay line to determine various frequency ranges. To avoid the false locking with process, voltage supply, temperature, and loading (PVTL) variations, the operating range will overlap for each other. If the overlapping region is too small so the points T_{b1}, T_{b2} and T_{b3} disappear, then the gain of VCDL can be increased to make these points appear. From simulation results of VCDL transfer function reveal that $K_{VCDL1} > K_{VCDL2} > K_{VCDL3} > K_{VCDL4}$. Where the gain ($K_{VCDL}$) of VCDL in range1 is K_{VCDL1}; K_{VCDL} is in range2 is K_{VCDL2}, and so on.

2.2.3 Coarse Tune Circuit

In this DLL, the coarse tune circuit is proposed to offer faster locking time and provide better jitter performance as shown in Fig. 5. When the input reference clock is activated, the output pulse of start-up circuit is used to set the initial control voltage of the loop filter to VDD. The out_clk of the delay line leads before the ref_clk. The dn and dn1 signals are activated and the Vctrl greatly decreases. When the out_clk is close to the ref_clk, the dn1 signals will disappear. The PD up and dn signals are then used to fine-tune this DLL.

The coarse tune circuit consists of a D-type flip-flop (D_FF) and an adjustable pulse width circuit. The adjustable pulse width circuit output (out_apw) is generated to reset the out_clk, when the out_clk leads before the ref_clk. A schematic of the adjustable pulse width circuit is shown in Fig. 5(b). The adjustable pulse width is controlled by the ref_clk and control voltage (Vctrl) of filter. The adjustable pulse width circuit consists of three stages VCDL and a AND gate. The delay between ref_clk and int_clk of the three stages VCDL is controlled by Vctrl. When the Vctrl increases that cause the delay between ref_clk and int_clk of the three stages VCDL decreasing. After the AND gate, the narrow pulse width is generated.

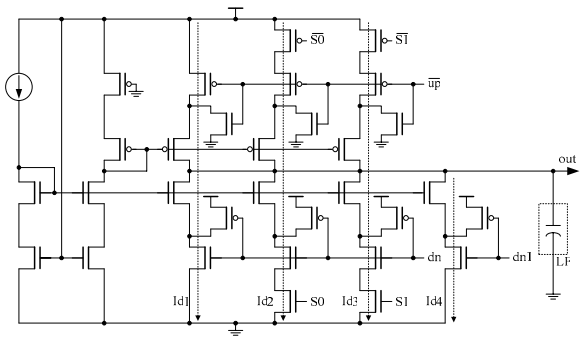


Figure 6: The schematic of the digital controlled charge pump and loop filter.

Table 1: The charge pump currents versus the K_{VCDL}.

Region	Control Signals	Condition	Current (Ich)	Gain (K_{VCDL})
Range 1	S0=0, S0=0	$T_{VCDL,max} < 2\times T_{d1}$	Ich1=Id1	K_{VCDL1}
Range 2	S0=0, S0=1	$T_{d2} < 2\times T_{d3}$	Ich2=Id1+Id2	K_{VCDL2}
Range 3	S0=1, S0=0	$T_{d4} < 2\times T_{d5}$	Ich3=Id1+Id3	K_{VCDL3}
Range 4	S0=1, S0=1	$T_{d6} < 2\times T_{VCDL,min}$	Ich4=Id1+Id2+Id3	K_{VCDL4}

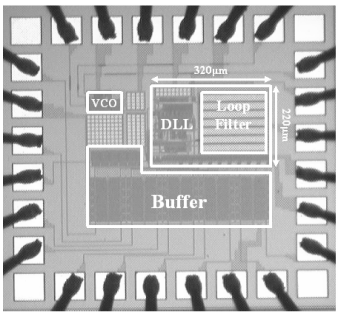


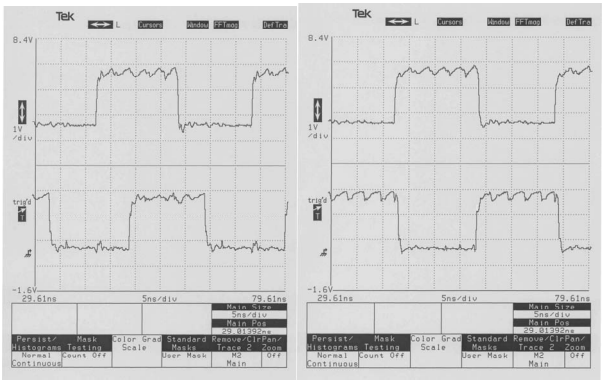
Figure 7: Microphotograph of the proposed DLL.

2.2.4 Digital Controlled Charge Pump

To design of a suitable DLL depends on various considerations, such as bandwidth requirement, jitter performance and lock time. From the analysis of the DLL small-signal AC model indicates that the fast acquisition time in the initial state and the jitter performance in the locked state are two important concerns. The wide-range operation DLL has various gains (K_{VCDL}) of VCDL, and the loop bandwidth changes with different K_{VCDL}. Furthermore, the current of the charge pump also influences the loop bandwidth. If the loop bandwidth is wide, then the lock time is short, but the input noise is larger. However, when the loop bandwidth is narrow, then the lock time is longer, but the input noise is smaller. Therefore, the loop bandwidth of DLL must be chosen carefully. Equation 1 shows the ratio of the loop bandwidth to the input operating frequency is [8]

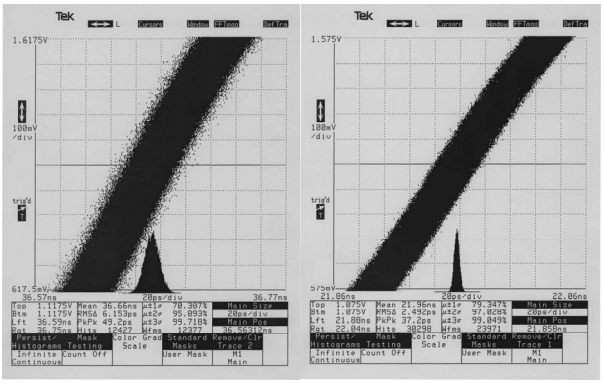
$$\frac{\omega_n}{\omega_{REF}} = \frac{I_{CH} \cdot K_{VCDL}}{2\pi \cdot C} \quad (1)$$

In this DLL, the charge pump circuit is implemented by a digital control scheme to enable bandwidth tracking, as shown in Fig. 6. The current of the charge pump is determined by the control signals (S1, S0) from the frequency range selector. The charge pump has various current combinations that correspond to various K_{VCDL} values, as shown in Table I. For example, in the range1, the control signals (S1, S0) are 0 and the current Id1 is the minimum current. However, in the range1, the gain (K_{VCDL1}) of VCDL is the maximum. On the other hand, in the range4, the S1 and S0 are high and the current Id4 is the maximum current. However, the gain (K_{VCDL4}) of VCDL is the minimum. Therefore, the ratio of the loop bandwidth to the input operating frequency will remain constant that has satisfied the equation (1).



(a) (b)

Figure 8: Clock waveforms at 32 MHz. (a) Output clock and phase 2. (b) Output clock and phase 5.



(a) (b)

Figure 9: The jitter histogram. (a) When operation frequency at 32 MHz and (b) at 320 MHz.

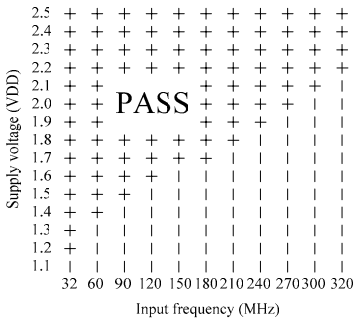


Figure 10: Shmoo plot of input frequency versus supply voltage.

3. Experiment and Comparison Results

The proposed DLL has been realized in a 0.25-μm standard CMOS technology and the chip area is 0.823×0.823 mm^2; this area includes the areas of the input and output digital buffers and I/O pads. The active area of DLL is 0.32×0.22 mm^2 and the loop filter consumes ~50% of the total active area. A microphotograph of this DLL is shown in Fig. 7. Figure 8 (a) shows the waveforms of output clock and phase 2 at 32MHz, respectively, and have a 72° phase difference. Figure 8 (b) shows the waveforms of output clock and phase 5, which are an inversion of each other with a 180° phase difference. Figure 9 (a) shows the measured jitter histogram for the DLL output clock at 32 MHz. The peak-to-peak jitter is 49.2 ps and the rms jitter is 6.153 ps. Figure 9 (b) shows the measured peak-to-peak and rms jitters for the 320 MHz output clock, at 37.2 ps and 2.492 ps, respectively. From the simulation results, the maximum locking time is 22 clock cycles at 160 MHz.

The Shmoo plot of the proposed DLL is obtained to investigate the dependence, as shown in Fig. 10. The y-axis represents the supply voltage VDD from 1.1 to 2.5 V, and the x-axis represents the input frequency from 32 to 320 MHz. Even in the low supply voltage condition, the proposed DLL can still remain in the locked state. The measurements show that the proposed DLL has low power and a wide operating frequency range.

Table 2: Performance comparison.

Performance Parameter	ADL DLL [1]	AAAM DLL [3]	AWR DLL [5]	ALJ DLL [7]	This work
Process	0.25-μm 5M CMOS	0.35-μm 3M CMOS	0.35-μm 1P3M CMOS	0.16-μm DRAM	0.25-μm 1P5M CMOS
Supply Voltage	2.5 V	3.3 V	3.3 V	2.3 V	2.5 V
Operating Range	150 ~ 600MHz	62.5 ~ 250MHz	6 ~ 130MHz	42 ~ 400MHz	32 ~ 320MHz
Lock Time	NA	NA	~1130 clock cycles	NA	22 clock cycles (Max.)
RMS Jitter	6.683ps with quiet supply	4ps with quiet supply	24.77ps @ 6MHz 3.297ps @ 130MHz	4.77ps with quiet supply	6.153ps @ 32MHz 2.492ps @ 320MHz
Peak-to-Peak Jitter	54ps with quiet supply	29ps with quiet supply	210ps @ 6MHz 24.3ps @ 130MHz	43ps with quiet supply	49.2ps @ 32MHz 37.2ps @ 320MHz
Power Dissipation	60mW @ 400MHz	12.6 mA@ 250MHz	132 mW @ 130MHz	52mW @ 400MHz	15 mW @ 320MHz
Active Area	0.13 mm^2	0.08 mm^2	0.45 mm^2	0.27 mm^2	0.07 mm^2

The comparison results are according to various wide-range DLL architectures, as shown in Table 2. The parameters are captured from the references [1], [3], [5] and [7], where the ADL DLL is reference [1], the DLL of the reference [3] is AAAM DLL, the AWR DLL is reference [5], the ALJ DLL is reference [7]. From the comparison results, the proposed DLL can achieve wide operating frequency than the the ADL DLL [1], AAAM DLL [3] and the ALJ DLL [7], and has faster lock time than the AWR DLL [5]. Furthermore, the area cost and power consumption of the prototype chip are much smaller than those of other wide-range DLL's [1]－[7].

4. Conclusions

In this paper, a fast-lock mixed-mode delay-locked loop for wide-range operation and multiphase outputs with a single clock cycle is proposed. The mixed-mode TDC architecture for the frequency range selector can automatically choose one of the delay lines in the VCDL according to various frequencies. The multi-controlled delay cell element for VCDL was switched by the frequency range selector, providing a wide operating frequency range and low-jitter performance. The coarse tune circuit is proposed to reduce the lock time and keep a better jitter performance in this DLL. The charge pump circuit is implemented by the digital control scheme to achieve adaptive bandwidth. Consequently, this DLL can operate correctly when the input clock frequency is changed from 32 to 320 MHz and generate ten-phase clocks.

Acknowledgment

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