A Complete and Fully Qualified Design Flow for Verification of Mixed-Signal SoC with Embedded Flash Memories

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Abstract

Today almost all the people in the industry are talking widely about full chip mixed-signal simulation, both in pre-layout and post-layout conditions, basically for two main reasons: a large range of applications is moving from fully digital to mixed-signal and full chip simulation with parasitic components, together with IR drop analysis, is becoming strictly mandatory before going to silicon. In fact, the cost of a mask set for a 90nm or a 65nm technology is growing in an exponential way, passing the million dollar for any single mask set. For these reasons, it is strategic to set up a very complete mixed-signal design flow allowing designers to go to the silicon in a safe way with the minimum risk of failure. Nowadays, various approaches to the same problem are pursued by different organizations, sometimes privileging the fully digital modeling of the mixed-signal system and some other times setting the digital part in VHDL and keeping the analog part at transistor level, simulating the whole chip with a mixed-signal simulator. Which is the right approach ? Which are the status and the reliability of the tools on the market ? Which is the acceptable trade-off among simulation speed, code coverage and precision of simulation results ? This paper tries to answer to these questions proposing a fully qualified and complete mixed-signal flow for SoC verification, implemented to design applications also containing embedded flash memories.

1. Introduction

When you think about designing a first silicon success complex mixed-signal application with an embedded flash memory, containing a significant analog part, you cannot forget to take into account some principal design steps:

- Full chip mixed-signal simulation (VHDL/Verilog and transistor level) to verify the circuit functionalities
- Full chip transistor level simulation with both digital and analog portions at transistor level to check whether the A/D and D/A interfaces work properly
- Flash core cell model availability as a built-in function of your fast spice simulator to be able to simulate large parts or the whole flash cell matrix
- Nominal optimization and statistical design analysis to optimize analog critical blocks and to increase the yield on silicon (DFY and DFM)
- Post-layout simulation and IR drop analysis with parasitic components for the final verification of the application before going to manufacturing.

An exhaustive and fully qualified mixed-signal design flow is shown in the flowchart of figure 1. The flow is divided into different blocks according to different levels of abstraction of the circuit simulation. Therefore, you can find system verification at mathematical level, functional simulation, analog sub-flow to design specific analog devices like bandgaps, opamps, sense amplifiers and oscillators, nominal optimization and statistical design analysis to increase the yield of critical analog circuits, mixed-signal simulation and, finally, post-layout and IR drop analysis stages.

In the following paragraphs, we will examine all the different levels of simulation stages exploiting their benefits in the process of designing a complex mixed-signal application with an embedded flash memory.

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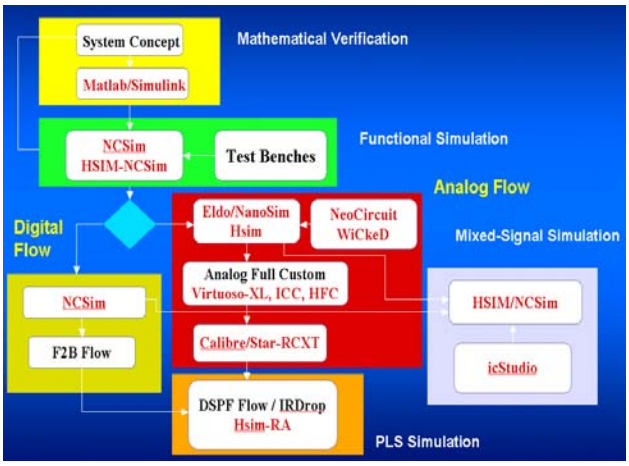

Figure 1. A complete and fully qualified mixed-signal design flow for SoC verification with simulation blocks at different levels of abstraction.

2. Simulation and Verification

Mathematical functional verification is performed at a very early stage of the design. In our flow, it is based on Matlab and Simulink, commercial tools allowing designers to describe the circuit behaviour using mathematical functions and to simulate it in a very fast way. The simulation environment also supplies complementary libraries containing standard analog and digital blocks with different functionalities. After mathematical simulation, designers switch to functional simulation mainly using a VHDL approach. All the blocks of the circuit, both digital and analog, are described at VHDL level and simulated with NCSim. At this point, during the designing phase, analog blocks start to be substituted with transistor level description replacing VHDL models. This is the most interesting step as regards circuit simulation because you can set all the digital part in VHDL/Verilog and the whole analog part at transistor level using a co-simulation engine. In our design flow, best performances are reached by HSIM-NCSim. The circuit is split in two parts so that digital portion is processed by NCSim (master simulator) while analog portion is processed by HSIM (slave simulator). This approach is very effective; in fact you can decide time by time which trade off between speed and accuracy to select. Basically it is like having a trimmer moving from full VHDL simulation to full transistor level simulation like shown in figure 2.

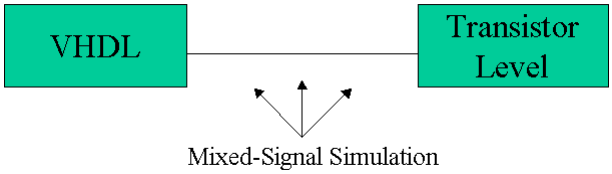

Figure 2. Mixed-signal simulation is like a trimmer from pure VHDL to transistor level description of an IC design. Moving this trimmer, you can choose the right trade off between speed and accuracy.

In our flow, we recommend to use HSIM-NCSim because it is very flexible and even though it is conceived to process digital-on-top applications, it allows with few easy tricks also to simulate an analog-on-top design. Furthermore, the HSIM simulator supports a built-in flash core cell model both for NOR and NAND flash cells so that you can exploit those features to simulate your full chip with an embedded flash memory. In fact, you can use the built-in flash cell model to include the whole flash cell matrix in the simulation. In this way, digital part will be simulated by NCSim and analog part plus flash cell matrix by HSIM.

In figure 3, you can see two program pulses and the corresponding read-verify cycles related to a full chip mixed-signal simulation using HSIM-NCSim of an application with an embedded NOR flash memory. Both digital and analog output waveforms are displayed in the same window. You can notice, for example, that the rising signal on the word line v(wl[5]), generated converting the digital signal DQPAD[0:31] into an analog ramp, leads to a shift in the threshold voltage lv9(mcell). On the bit line v(bl[0]), you can also notice two voltage pulses corresponding to the cell threshold voltage increasing ramps. The possibility to plot cell threshold voltage and drain current is given by the built-in flash cell model availability in the simulator. Using standard MOS transistors to model flash cells will not allow you to print those quantities and will slow down the circuit simulation.

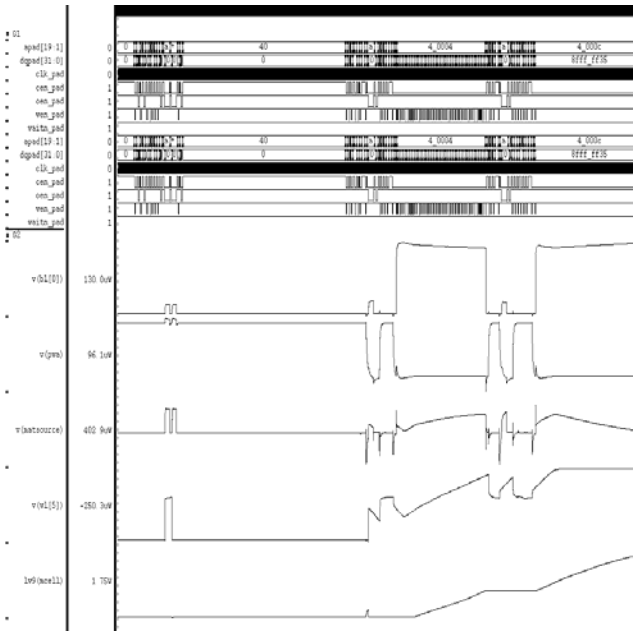

Figure 3. Output signals from a mixed-signal simulation of a SoC design with an embedded flash.

4. Nominal Optimization and Statistical Design Analysis

When designing with the most advanced technologies at 130nm, 90nm and 65nm, it is very important to perform the nominal optimization of critical analog blocks and, above all, to try to improve at the maximum the circuit yield on the silicon. Often, due to the low yield of a small but critical analog block, yield of the entire product is dramatically reduced. For this reason, in our design flow, we do not miss to propose to designers the usage of state-of-the-art tools for DFY (Design For Yield) and DFM (Design For Manufacturability) that allow designers to better know their circuits and, consequently, to fit component sizes and choose the right topology. We think that the usage of this kind of tools will become more and more important as designers are moving to 90nm and 65nm technologies, when DFM will grow as a constraint both at designing and at layout phases. WiCkeD is a commercial tool supporting a large number of different analyses like feasibility analysis, monte-carlo analysis, worst-case distance analysis, yield analysis and yield optimization that really help designers to improve their analog devices. In figure 4, you can see a scatter plot and a performance star diagram from the analysis of a bandgap voltage reference from the IC with the embedded flash carried out with WiCkeD.

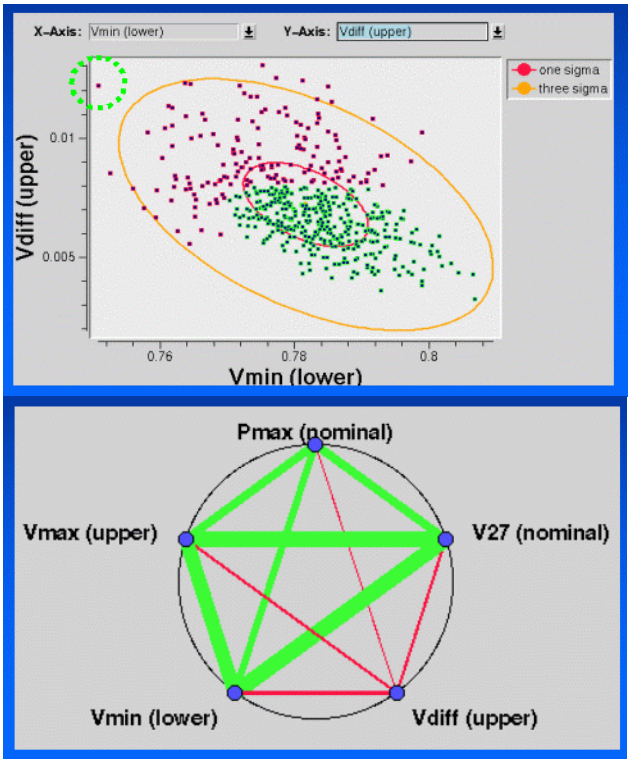

Figure 4. Scatter plot and performance dependency star diagrams from a WiCkeD working session related to a bandgap voltage reference.

The scatter plot visualization allows back annotating and simulating, inside the analog design environment, the performance behaviour of each sample point from a monte-carlo analysis. Moreover, the performance dependency star diagram illustrates the relationships among different performances of the circuit under test. The tool also provides a full datasheet with all the statistical parameter values for the chosen sample in *html* format. Using this approach, yield has been considerably improved by a 30% factor.

5. Back-End Flow for Mixed-Signal SoC

Another important issue in mixed-signal applications is the layout of the analog portion together with the management of the floor planning, when you have analog on top. As regards these topics, we propose a solution based on the Cadence Virtuoso-XL and Virtuoso Custom Router tools integrated with an

internally developed tool box called as *HFC* (Hierarchical Full Custom) which implements some layout functionalities not supported by commercial tools. Interoperability of HFC and Cadence tools is assured by the fact that they both operate on the same layout window and on the same database. Instead, as specifically regards the mixed-signal floor planning, it is still an open issue where a real good and satisfying tool is missing on the market, but we are already looking at some interesting proposals like Analog Virtual Prototyping (AVP). In figure 5, you can see a layout snapshot of the analog portion of a mixed-signal application with an embedded flash memory routed with the help of HFC. Layout engineer productivity is incremented by 20%-25% by the usage of HFC.

6. Post-Layout Simulation and Verification with Parasitic Components

Today, it is clear in the designer community that post-layout simulation with parasitic components on flat netlists coming out from parasitic extractors is becoming no more possible for several reasons. In fact, netlists are too large with too many parasitics and there are also difficulties in mapping and recognizing the net names between the hierarchical pre-layout and the flat post-layout netlists. Therefore, there is the incontrovertible need to move to a hierarchical approach for the post-layout simulation so that it is mandatory to use a DPF/DSPF flow or a newly developed approach to overcome size problems and netlist management by hand. In this approach, the hierarchical pre-layout CDL netlist (CDL is the preferred netlist format because it is used for DRC and LVS checks) with DPF and DSPF files back-annotated (DSPF flow) simulated with a fast SPICE simulator. On our side, we chose to work with HSIM fast post-layout functionality (PLX option) to perform post-layout simulation on large netlists in non-volatile memories technologies with the flash matrix included.

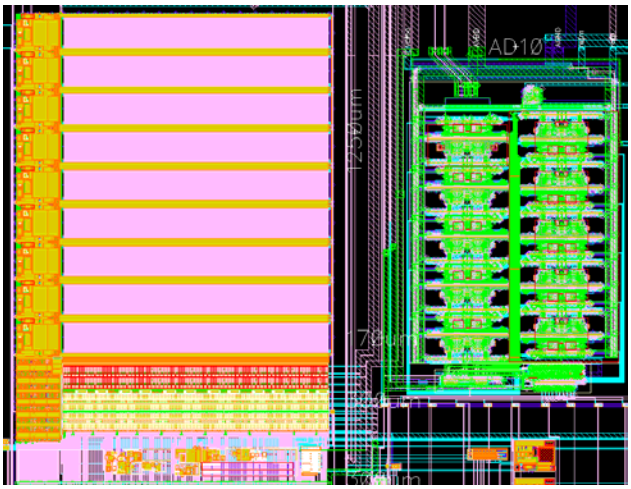

Figure 5. Layout of the analog portion of a SoC with an embedded flash macrocell routed with the help of internally developed tool HFC.

Another approach we are currently investigating is the capability to generate a fully hierarchical post-layout netlist from the pre-layout hierarchical one and the DSPF parasitic file. This last approach has been implemented by means of an internally developed tool, called as *icSim*, allowing to recreate, starting from a pre-layout CDL netlist and a DSPF file, a fully hierarchical post-layout netlist with back-annotated parasitics [1]. In figure 6, you can see one sample of the icSim interface, showing the management of sub-circuit hierarchical connections.

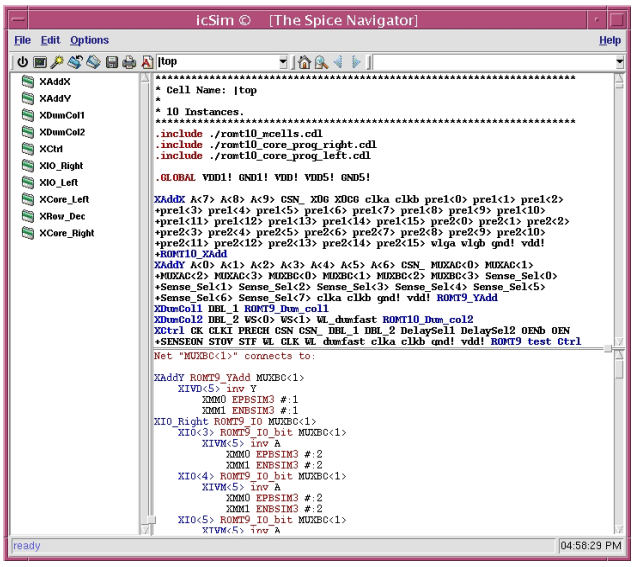

Figure 6. One sample of icSim. Pre-layout CDL netlist is loaded and parasitics are added at sub-circuit level generating a fully hierarchical netlist including parasitic components.

7. IR Drop and Substrate Noise Analyses

Finally, before going to the factory, you need to run IR drop and substrate noise analyses to check not to have power distribution problems in the chip and noise problems in the substrate. In fact, often standard cell digital libraries are quite noisy injecting such a noise in the substrate so that it is amplified in the analog part generating a bad working of the entire application. In our flow, we propose the usage of HSIM-RA for IR drop analysis and SubstrateStorm for substrate noise analysis. This kind of tools is becoming, day-by-day, more and more important as a key point for reliability of mixed-signal designs. In figure 7, you can see an example of IR drop analysis output map. Orange and red portions in the map indicate potential power distribution problems in the highlighted areas of the chip.

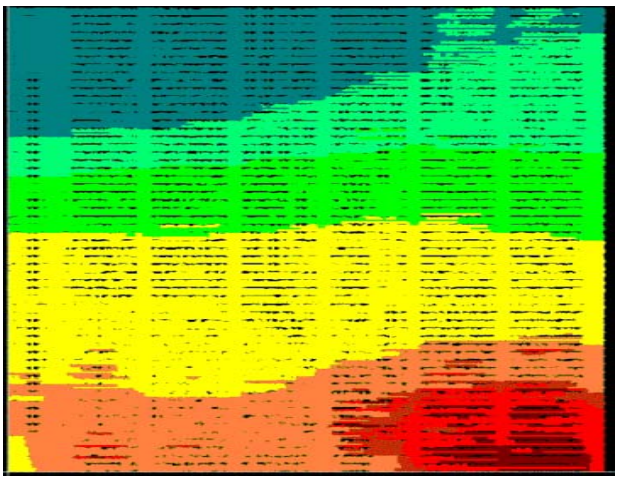

Figure 7. Example of IR drop analysis output results. Orange and red portions of the map indicate power distribution problems in the chip.

8. Quality and Reliability of the Design

Major benefits to the design quality derive from the usage of advanced tools for mixed-signal simulation that enable both to simulate very large circuits by means of behavioural languages and to really check undesired effects at the interfaces between analog and digital portions of the chip, where problems are often found when silicon is already out. Designers can simulate the whole circuit at different mixed-signal levels (mathematical, behavioural, digital VHDL together with transistor level schematics and post-layout) always providing a good trade-off between accuracy and speed. In this way, designers can privilege either speed (mathematical and behavioural simulations) when they need to check system consistency or accuracy when they need to check critical functionalities. Reliability is assured by the usage of state-of-the-art tools for yield analysis and improvement together with a DFM approach to the layout construction. Forcing robustness to critical analog blocks is a key factor for the first silicon success that is mandatory when designing with the newest technologies. Moreover, the systematic usage of IR drop and substrate noise analysis tools is becoming more and more inevitable to increase the percentage of applications working properly at the first silicon. IR drop analysis is performed with HSIM-RA capabilities, allowing to generate detailed maps of voltage drop in the different areas of your chip.

Conclusions

An exhaustive presentation of a complete and fully qualified A/M-S design flow for the verification of complex SoC with embedded flash memories has been described in this paper. From the presented analysis, it is clear that when designing with 130nm, 90nm and 65nm technologies you need to put in your design flow advanced A/M-S tools available on the market and sometimes to develop your own point tools to implement functionalities not supported in commercial tools. The aim is to avoid re-spins that are nowadays very expensive due to the incredibly increasing cost of the mask sets and, at the same time, make you miss time-to-market windows. DFM and yield improvement are the new keys to profit and, in that sense, such kind of tools must be integrated in a modern design flow. Another important point, when we talk about non-volatile memories, is the usage of built-in flash cell models in advanced simulators allowing to include millions of cells in the circuit simulation. NAND flash market is growing very fast so that it is strategic to be able to reach the market with reliable products at the right time. Moreover, when speaking of new technologies, analyses like IR drop and substrate noise that previously were not always performed by designers are overbearingly coming into play and soon will be strictly mandatory.

The philosophy we followed to formalize the flow is to integrate commercial very advanced solutions,

when available, trying to standardize the flow at the most. Internally developed tools and sets of script files have been conceived to link the various commercial tools and to replace missing features when necessary. Major benefits related to our flow are the standardization of the methodology, the possibility to verify the whole circuit responses at any design stage and the enhancement in terms of speed brought about to the overall design cycle avoiding unpleasant surprises at the first silicon out.
Another important consideration we can certainly do is that tool and simulator benchmarking is a mandatory and strategic activity to keep our users updated on the latest tool evolution. The design flow is so flexible to allow an easy replacement of obsolete tools with more effective ones and to be able to insert new state-of-the-art tools without big efforts. Strategic, in this sense, is the tool interoperability that should be assured operating on the same shared database.

Acknowledgments

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