A Mixed-Signal Verification Kit for Verification of Analogue-Digital Circuits

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Abstract

This paper presents an innovative approach for analogue and mixed-signal verification. It consists in a "verification kit" that makes use of concepts used in state-of-art digital verification, such as automatic results collection, coverage elaboration, data checking capability, pseudo-random and constrained stimuli generation. Using a Bandgap cell as case study, the paper shows as the presented approach allows a precise definition of the verification space and a saving of more than 50% of the total verification effort respect traditional verification methodologies. The paper shows also how the approach can be extended to more complex mixed-signal systems.

1 Introduction

If verification of digital sub-systems is based on advanced techniques such as constraints capture, randomised or pseudo-randomised stimulus-generation, result collection with coverage analysis, on the other side the verification of analogue sub-systems mainly depends on the designer's expertise. This is proven by the fact that, in analogue verification domain, in many cases different designers verify the same set of parameters with different test-benches and sometimes the verification responses are different. Moreover, even if mixed signal simulation tools are already available in the market and make it possible to link and simulate analogue and digital block in the same test-bench [1], nowadays the majority of the analogue designers simulates various mixed subsystems in order to verify a specific function of the whole device (i.e. reset and start-up conditions, power down/up signals polarity, functionality of analogue block selected and/or driven by digital part, test-mode etc. etc.). This approach provides a set of information about the functionality of the whole system that depends on the stimuli used by the designer and on the way in which the designer has collected the simulation results.

Some solutions exist to overcome these problems and to better integrate digital and analogue verification (e.g. from [2] to [7]) but so far they require a considerable effort in terms of building the environment and the concepts of randomisation and coverage are not extensively used.

In this paper, an innovative analogue and mixed-signal verification approach is presented, that extends and completes some previous works [8, 9, 10]. It consists in a "verification kit" mainly composed by elements to inject and collect results from an analogue or mixed-signal DUT, in a way that the techniques used in state-of-art digital verification (such as automatic results collection, coverage elaboration, data checking capability, pseudo-random and constrained stimuli generation) can be extensively reused.

As proof-of-concept example, the proposed verification kit is used to verify a Bandgap cell, a common circuit able to generate a temperature independent output voltage level equivalent to the band gap level of the silicon [11, 12]. Even if this device is not considered a complex case study, however its verification requires several simulations and much effort to collect the results. Therefore, it is possible to use this example to show how the proposed novel approach can extend digital verification methodology to the analog domain and which the improvements are in terms of data collection, coverage analysis and simulation run time. The paper shows also how to extend this novel approach to more complex mixed-Signal systems.

The Bandgap used as case study in the following verification process is designed using BJT technology and the pin out is shown in Figure 1.

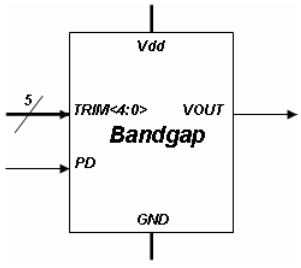

Figure 1: the pinout of the Bandgap used in the example

2. Specification of the Bandgap

The main features of a Bandgap cell are summarized in the following Table 1.

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Parameters	Min	Typ	max	Unit
Power supply (Vdd)	3	3.3	3.6	V
Temperature	-40	27	150	°C
Output voltage * (VOUT)	1,22-1%	1,22	1,22+1%	V
Settling time	50		230	µs

*** +/- error of 1% is referred to 1.22 V.**

Table 1: Main specification of the Bandgap

Since it has been assumed the availability of a 5-b Trimmer word, the verification process has to answer the following basic requests (see also Table 1):
"For each process variation at least one 5-b Trimmer configuration that guarantees absolute maximum error of 1 % for all temperature range (from -40 °C to 150 °C) has to exist"

Fig.2 shows the well-known temperature-insensitive Bandgap output that has to occur for each process variation.

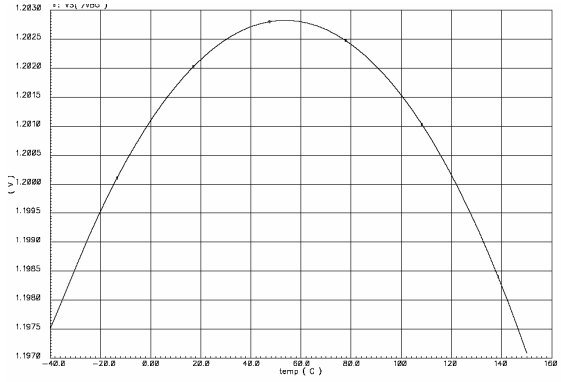

Figure 2: Typical acceptable output curve of a Bandgap

In order to verify the previously discussed item, the following method is taken into consideration:

1. only BJTs and resistors process variations are considered (9 different model cards)
2. for each process variation all the 5-b configuration trimmers have to be investigated in terms of temperature response (5 temperature values are considered)
3. other parameters are considered in typical conditions (i.e. Vdd = 3.3 V)

The restriction of the process variations range reported in point 1 is due to the fact that for this preliminary check (DC response of Bandgap based on BJT technology) it is possible to assume that the contribution of MOSFET process variations is negligible if compared with the BJT and resistor ones.

In the following, the standard verification approach is compared with the one proposed in this paper.

2. Standard approach

Using a standard approach, the previously discussed method can be translated in 9 different parameter simulations (each one with a different model card) with temperature sweep (from -40 °C to 150 °C using 5 values) in which the variable is the trimmer code (from 0 to 31). For example, using *Cadence Affirma Analog Artist* and setting the parameter simulation in the proper way with a fixed model card (all typical conditions), the results are the ones shown in Fig.3. The figure shows 32 curves, each one related to a different trimmer code in temperature sweep.

The best curves in terms of temperature response are placed in the middle, thus it has to be verified (for example by *Calculator* tool) which curves are in compliance with the specification (VOUT in Table 1). In this case the trimmer codes 0, 1 and 2 respect the specification (absolute error < 1%). This kind of simulation has still to be run for 8 times in order to cover all model cards. This procedure does not allow automatic data collection and the results analysis has to be done from time to time by the designer.

Other procedures can be used (i.e. *Corner* tool) in order to run all the simulations (included model card variations) only once, but in any case results collection and analysis can not be automated. It is worth noting that whatever procedure is used, the simulation run time (*Sim_time*) can be calculated as follows:

$$Sim\_Time = 9 * 32 * Sim\_Trim \qquad (1)$$

where 9 is the number of the possible process variations (BJT and resistor), 32 is the number of possible trimmer code variations and Sim_trim is the simulation run time of one of the 32 simulations included in a single parameter simulation. For this case study it is possible to assume *5 s* as *Sim_trim*, thus:

$$\text{Sim\_time} \approx 25\ min \qquad (2)$$

In addition, it is important to highlight that in (2) the time that the designer spends to collect and analyze the results is not taken into account and it is considerably high.

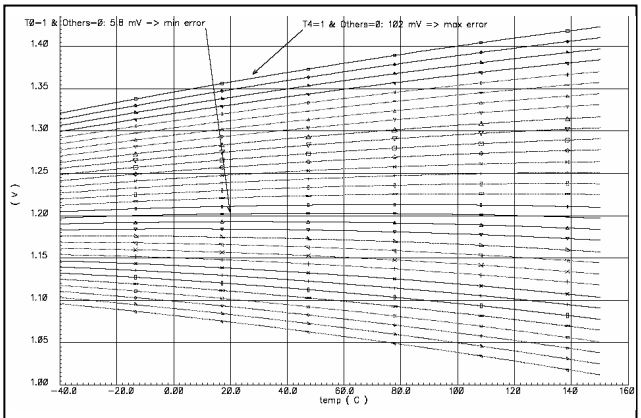

Figure 3: Results in typical condition

3. The Mixed-Signal Verification Kit

The proposed mixed-signal verification kit is represented in Figure 4. In this paper, the kit is applied to the Specman Elite® environment [13] a tool for automating the process of functional verification. Specman includes a verification language, called "*e*" (under standardization with the IEEE initiative P1647 [14]), that allows the verification engineer to capture the rules from specifications as well as to generate tests automatically.

The core of the kit is a library of fully controllable and configurable verification terminals suitable to stimulate and monitor analogue signals: vProbes and vSource. The *vSources* blocks represent "verification Sources" which are the models of a signal source to bridge between verification domain, in which the stimuli are produced as digital word, and analogue domain that is able to process only continuous time stimuli.. Examples of vSources are: signal generators, noise injectors, parameters spread emulator, etc. *vProbes*, "verification Probes" are models of a signal probe to bridge analogue domain in which continuous time output are obtained and the digital Verification environment that is able to process only digitalized signal.. Examples of vProbes are: voltage/current/time detectors, min/max functions etc. vSources and vProbes, as shown in the next paragraph, are implemented partially in "e" and partially in AHDL Analogue HDL, such the VerilogAMS [15].

Drivers are procedures written in "e" that generate the proper set of stimuli, either directly driving the digital part or driving the analogue part through the vSources. *Monitors* receive the outputs directly or through the vProbes. In addition, the detection of the failures occurring in the analogue or digital DUT is done through the use of a *scoreboard* that contains all the data needed to compare the expected responses with the real ones. The *Checker* controls the data coming from the monitors, to check for rules compliance for instance. A *sequence generator* is provided to handle and schedule the whole verification environment. Therefore, using all the information coming from monitors and scoreboard related to the covered input space, it is possible to elaborate a coverage function representing the compliance of the mixed system with its specifications.

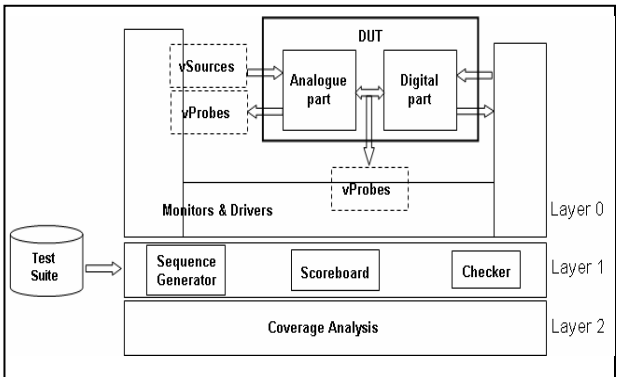

Figure 4: The Mixed-Signal Verification Kit

4. The vSource and vProbe concepts

The schematic diagram of a generic vSource is shown in Fig.5. It is composed by an "e" description part and an AHDL one. The "e" part transfers the three following kinds of information into the AHDL domain.

Signal parameters: in the integrated mixed-signal verification environment, the stimuli coming from "e" domain are transformed in the parameters of a function generator. For example, in order to produce a sine-wave, the following parameters are needed: frequency, amplitude, phase, delay etc. It is worth noting that the vSource output signals could represent also a parameter spread of an analogue DUT sub-system (i.e. input voltage offset values of an operational amplifier due to input pair area mismatch).

Configuration signals: a configurable DACs layer converts the digital stimuli in analogue ones in a specific range and with a certain resolution (see Configurable DAC blocks in Fig.5);

Time Manager signals: it is necessary to optimise verification/simulation time, e.g. by decoupling the digital simulator events with mixed-signal ones, or providing special time function impossible to be reproduced in the digital verification environment.

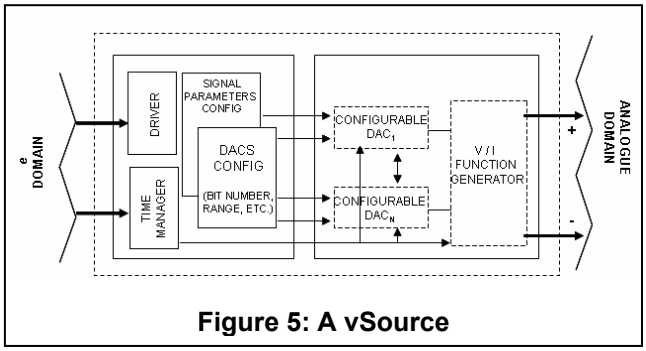

Figure 5: A vSource

The schematic diagram of a generic vProbe is shown in Fig.6 A generic vProbe acts in the opposite way than a generic vSource: the selected analogue output signals coming from analogue DUT are transferred into the "e" domain in order to collect them in a proper way (see Monitor in Fig.6) and elaborate dynamic coverage analysis. In addition, since it is not worthwhile to manage complex mathematical function

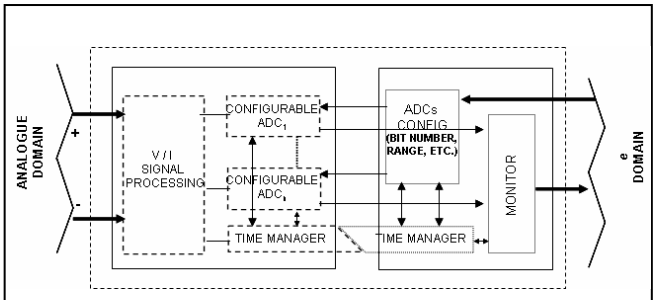

Figure 6: A vProbe

with "e" language, some vProbes include a signal processing unit in the AHDL domain (see V/I Signal Processing block in Fig.6).

5. The use of Mixed-Signal Verification Kit for the Bandgap Verification

Fig.7 shows the schematic representation of the simplified integrated environment used for the Bandgap. The environment shown in Fig.7 is mainly composed by:

- BandGap: Description of the BandGap cell (transistor level or HDL model);
- vS_vdc: vSource with configurable parameters vmin-vmax as allowable voltage range that drives Vdd (power supply);
- vP_ivalue: vProbe to measure the current consumption of the BandGap when rise edge of Trigger signal occurs;
- vP_vsettling: vProbe that measures the BandGap settling time due to the Power Down/Up signal (PDN);
- vP_value: vProbe to sample the output value when rise edge of Trigger signal occurs and to establish right or wrong BandGap behaviour for each temperature, process variation and trimmer condition.
- IE: interface elements that allow transfer Trimmer word and PDN signal from digital environment to the BandGap. These blocks are used to take into account the effect on the transferred signal due to the variations of the digital/analogue power supply signals

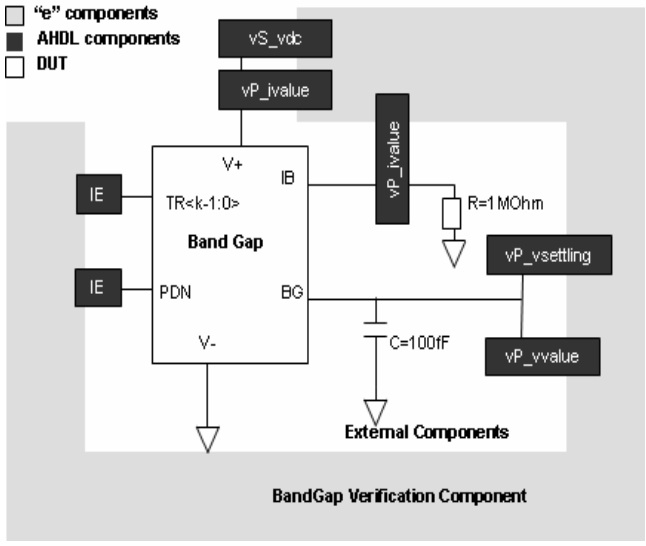

Figure 7: Use of Mixed-Signal Verification Kit for the Bandgap

When *Trigger* signal occurs (see Fig.8) the vP_value acts as a simple Scoreboard, thus checking if the output of the BandGap is in the area between low and high thresholds (decided by the user).

The signals *TRIM* and *Trigger* (that are included in the environment) are generated in "e" part in order to change trimmer conditions, to synchronize *TRIM* signal (based on the internal timing signal named *Sync*) and to provide trigger signal for vP_value block. The period and duty-cycle of the *Trigger* signal can be changed by the user in order to take into account settling time of the band gap (in this case could be directly the one specified in Table 1). Fig.9 shows the timing of the signals involved in the verification process.

Note, period and duty cycle of internal *Sync* signal is defined by the user.

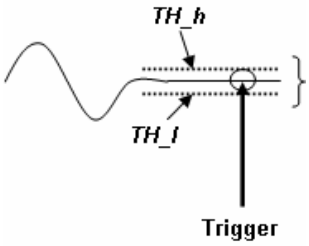

Figure 8: How to implement a check on the bandgap output

It is worth noting that automatic multiple simulations (regression) involving temperature and process variations are now possible: the user has to decide the temperature range (min&max), the temperature step and the model card that need to be investigated.

The verification environment depicted in Fig.7 includes some configuration files the user can modify/extend. An *ENV file*, with environment definition including instances; a *Config file*: information about parameters used in the verification process (e.g. temperature step, Temp_min, Temp_max, low and high threshold etc. etc.); an *"AMS" command file*: information related to the simulator parameters and model cards; a *TEST Suite*: database of pre-defined test according to the verification plan; a *Regression File*: script to set up multiple simulations.

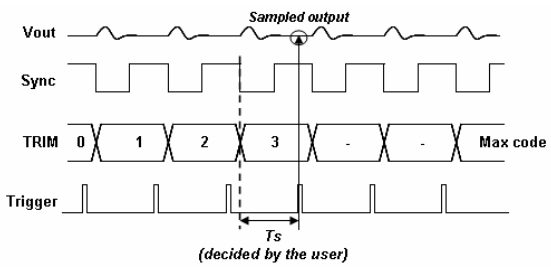

Figure 9: Timing of the signals involved in the verification process

6. Results

Thanks to the regression ability (multiple simulations), using this novel approach it is possible to act in the following way: each model card is simulated for 5 temperature values;each couple model card/temperature value is simulated for all trimmer code.

It is worth noting that Specman tool allows to introduce a control loop between probed outputs and stimuli: an output result obtained at the time "n" can produce an effect on a stimulus generated at the time "n+1". Thus in the presented environment this is translated in the following item:

"When the output corresponding to a certain model card-temperature pair presents an error (Voltage Value) higher than 1% for a certain trimmer code, this pair will not be used for other simulations that involve the same trimmer code"

Simulation run time result shows that the *Sim_time* in this case is about *10 min*, thus, if compared with the result shown in *2*, more than a 50% improvement has been gained. Moreover, the time for the engineer to setup the environment is drastically reduced.

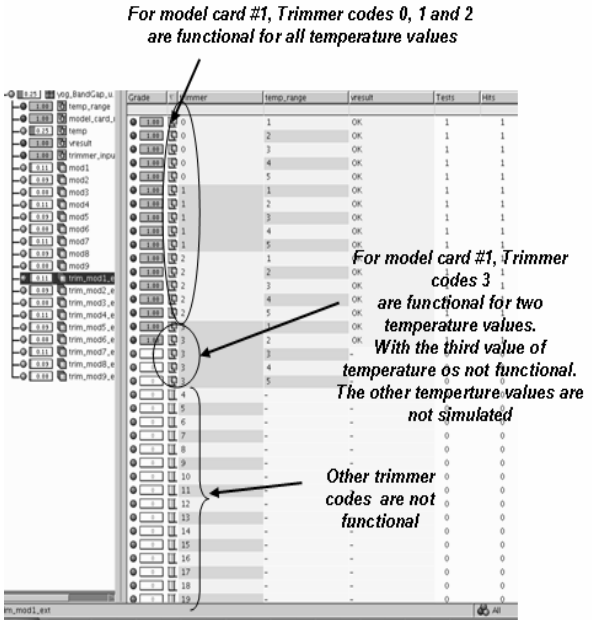

Figure 10: results collection and coverage elaboration

The main coverage items used to elaborate the results are, for output coverage:

- For each model card, is there (at least) one trimmer code that guarantees an error less than 1% for all temperature values?
- For each trimmer code, which are the model cards that guarantee a maximum error less than 1% for all temperature values?

For input coverage:

- Have all the trimmer codes been used?
- Have all the model cards been used?
- Have all the temperature values been used?
- For each model card, have all the trimmer codes been used?

Fig.10 is an example of coverage elaboration and data collection results. It is worth to note that the obtained results match the ones related to standard simulation (see section 2) and also that results are collected in a comprehensive way, i.e. in detailed reports and they not rely on the interpretation of waveforms by the verification engineer as happens in the standard approach.

7. Conclusions

The presented approach is valid also for more complex mixed-signal systems: the mixed-signal verification kit includes an extensible, easy configurable and ready to use set of components to drive, monitor and process current and voltage signals together with a significant set of coverage items, checks and test scenarios for most common analogue blocks such as DC-DC converters, amplifiers, buffers, comparators, band gap, voltage reference and power on reset blocks. The user can easily configure the verification environment through a graphical interface and build different test scenarios. In the same way, vSources and vProbes can be combined to generate and elaborate any kind of continuous signals.

The proposed approach offers a highly integrated and automated solution extending the most advanced techniques for functional dynamic verification to analogue circuits. Concepts like stimuli pseudo-randomization, coverage analysis, scoreboards and regressions are applied to mixed signal design drastically reducing verification time and increasing verification quality.

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