

Striking a New Balance in the Nanometer Era: First-Time-Right and Time-to-Market Demands Versus Technology Challenges

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Abstract: Today's semiconductor marketplace demands nanometer designs of unprecedented complexity and performance, with uncompromising time-to-market requirements. This drives a focus on predictable, high-quality design results despite the challenges associated with these next-generation technologies.

This scenario is complicated even further by the need to address these challenges across a wide spectrum of products, ranging from high-frequency processor designs to extremely complex ASIC designs. In the nanometer era, the common factor for ensuring market leadership across this broad variety of products is achieving single-pass design success to avoid costly re-spins and the loss of market opportunities: design turnaround time must be minimized without compromising design efficiency and first-time-right requirements.

Design automation tools must balance both requirements, while providing designers with information that enables them to "design around" potential trouble spots in both today's and tomorrow's environment to ensure an exceptional level of built-in quality. This discussion highlights some of the innovations IBM is developing, such as variation-aware and statistical timing, faster serial and parallel processing, more highly integrated data models and tools, and concurrent chip and package design, which optimise the competing requirements of simultaneously reducing design turnaround time and achieving single-pass design success, while effectively managing the technical challenges associated with nanometer designs.