

Reduction of CMOS Power Consumption and Signal Integrity Issues by Routing Optimization

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Abstract—This paper suggests a methodology to decrease the power of a static CMOS standard cell design at layout level by focusing on switched capacitance. The term *switched* is the key: if a capacitance is not switched often, it may be high. If it is frequently switched, it should be minimized in order to reduce power consumption. This can be done by an algorithm based on forces that automatically optimizes the position and length of every single wire segment in a routed design. The forces are proportional to the toggle activities derived from a gate level simulation. The novelty is that this allows to iteratively find a new topology for the wire segments. Our algorithm takes as input an already given, grid routed layout.

I. INTRODUCTION

Dynamic power, more precisely the switching net capacitances, still causes the highest part of the power consumed in integrated systems. If most of a system is designed, an optimization late in the development flow can avoid long re-design iteration cycles.

A. Related Work

Some ideas in the proposed methodology are inspired by force driven placement strategies as in [2]. The minimization of these forces yields a power optimized placement. The wire lengths of highly active nodes are kept low.

Using the switching activity as a steering factor while optimizing C is a well-known general strategy in literature. This has been suggested in [3] and [1].

An actual application on layout level is given in [6]. Similar to our method, it is shown that non-uniform space between wires can minimize power. However, only bus interconnects are considered, rather than logic signal nets in general. Also, a change in topology is not in the scope of [6].

[8] describes how the properties of metal layers can be exploited to achieve a low total net switching power. This is done by assigning long and highly active wires to upper routing layers carrying the least coupling capacity per unit length. Our methodology optimizes the topology of wire segments *after* routing *within* the layers.

B. CMOS Basics

1) *Capacity*: Two important trends in the physics of wires justify to focus their topology for power minimization. First, wire capacitances increase over the years when compared to the average gate capacitances [7][5]. Second, the side-to-side capacitances make up an ever growing amount of the total capacitance [8].

2) *Power*: We try to reduce the capacitive power. Its formula is well known in the literature as $P_C = C\alpha_{01}fV_{dd}^2$. $\alpha_{01}fV_{dd}^2$ is the product of switching frequency and the square of the supply voltage of the node and is invariant after logic synthesis. We can therefore introduce a proportionality constant κ that includes this product and express the power as:

$$P_{net} = \sum_i \kappa_i l_i \left(\frac{1}{d_{li}} + \frac{1}{d_{ri}} \right), \quad (1)$$

if we only consider the sidewall capacitances, l_i is length of the i^{th} wire segment, and d_{li} and d_{ri} are the left and right distances to the next metal objects, respectively.

II. OPTIMIZING THE WEIGHTED CAPACITANCE

A power optimized routing can be obtained by surrounding each single wire with more space. Of course, this is undesirable due to limitations in area. However, we can exploit the remaining space after routing, especially grid-based routing, such that highly active wire segments become more isolated than segments with low switching activities. Section I derived the wire length as a second parameter to be optimized regarding the capacity. We propose to shorten high- κ nets accepting an increase in low- κ net's coupling wire segment lengths.

Both optimization goals described above can only be useful if they respect each other. It is not very helpful to isolate a high- κ wire segment if it is very short. On the other hand, shortening a high- κ wire that is not in the proximity of another net might be less effective than shortening a low- κ net that is very close to another one.

Wire segments that are already physically routed can not just be placed somewhere else. There could be other not movable objects in the way like clock or power lines or vias. Moreover, we must consider wire segments in one metal layer that have one or more branch segments in a layer above or below. Then, a change in position of such a segment would cause these branch segments to change their coupling lengths and thus their power.

III. THE PROPOSED METHOD

The idea of how to separate higher- κ wires relies on a force model between wire segments. The force between two wires is proportional to the sum of their κ -factors. The force decreases with $1/d$ to reflect Formula (1). Iteratively, the segments

traverse into a balanced state by following the directions of their force fields.

Since the branch lines must be taken into account (cf. Section II), this step may be taken only if we gain a total minus on our objective function. This can be mapped to a second model: the longer a segment gets, the more a counter force must prevent this. This can be thought of as a repulsive spring. The proximity of the considered branch segment influences the spring constant. It should be high, if a reduction in length would save a lot of switched capacitance. This is the case if the branch segment is close to a high- κ object and/or carries a high- κ value itself.

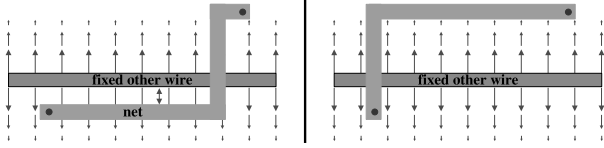


Fig. 1: Topology before (left) and after (right) optimization.

Fig. 1 shows the most simple example, where we optimize a topology as in the left side. The optimized position for the horizontal segment of the net connecting the two end nodes is above the fixed other horizontal wire (cf. right side). Using the field forces only, the horizontal bar would move further to the south. With the repulsive springs introduced, the lower horizontal segment receives a high contraction, because of the presence of a high field. The contraction gets transmitted across the vertical segment to the upper horizontal segment. Because the spring force of the upper segment is smaller, the balance will cause the lower bar to get shorter, and the upper bar longer. After a sufficient amount of time steps, the optimized layout results.

IV. EXPECTED BENEFITS

This section derives a comparison between the net switching powers before and after optimization. The expected optimization potential is high.

The design model produced by a commercial tool consists of N parallel wire segments routed on $M > N$ tracks. Two additional fixed wires with $\kappa = 0$ model the border of the scenario. This shall represent the result of a grid-based router as used in the industry under chip size constraints. The assumed wire width to minimum spacing ratio is 1:1. A $1/x$ distribution of toggle activities reflects the typical situation for industrial ASIC designs.

The task to optimize the $N + 1$ distances $d_0, d_1, \dots, d_N$ between $N + 2$ wires such that the power is minimal can be formulated as:

$$P_{segs} \propto \sum_{n=0}^{N+1} \frac{(\kappa_n + \kappa_{n-1})}{d_n} = \min!$$

$$d_n \geq d_{min} \quad \forall n = 0 \dots N$$

$$\sum_{n=0}^{N+1} d_n \leq (M + 1)d_{min} \quad (2)$$

This is a geometric program, where the first line is the objective function. We recorded the value of P_{segs} with the

generated κ_i s and the initial d_i s for comparison. The second line reflects the minimum spacing rule. Together with the chip size constraint in the third line, the complete system was passed to a public domain geometric program solver [4]. The solver returns both the optimized value for the objective function P_{segs} and the new constraint values d_n .

Tab. 1: Average net power reductions for $M=N+1$

N	4	8	16	32	64	128
$-P_{net}$ [%]	29.9	26.7	26.2	24.1	17.7	14.1

Tab. 1 displays the resulting average net switching power savings of random designs as a function of N , the parameter M is set to $N + 1$. Multiple passes with different sets of random seeds were run to obtain average numbers. The savings displayed in the table are promising: For example, for a bus with $N = 64$ wires running on $M = 65$ different tracks, optimal wire spacing can reduce the net switching power by about 17%. This is a significant change. It further increases for higher numbers of M , ie. with more space.

There are a couple of factors that will cause loss in optimization potential, cf. Section II. Considering this, we are in the range of the power savings at layout level as expected in [6] for buses.

V. FUTURE REMARKS

The optimization engine is intended to work together with standard ASIC design flow tools. It reads real layout data and toggle activities from them and performs the optimization methods described. The result is a modified layout which is written back to the tool's database.

The method does not yet support Miller capacitances. However, if the variable *toggle rate* is replaced by the possible overlapping transition time frame of two adjacent nets, the same algorithm can be used to minimize the risk of failure due to crosstalk disrupted signal integrity. The algorithm can further be optimized to react on the two forces at the two sides of a wire segment with an optimal wire width. This can repair timing violations late in the flow. Ordering the nets in a very specific way can further improve the effectiveness of wire spacing [9]. A mechanism to split the wire segment into pieces is beneficial if only part of it is movable.

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