Optimising Test Sets for a Low Noise Amplifier with a Defect-Oriented Approach

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Abstract

This paper is aimed at studying defect-oriented test techniques for RF components in order to optimize production test sets. This study is mandatory for the definition of an efficient test flow strategy. We have carried out a fault simulation campaign for a Low-Noise Amplifier (LNA) for reducing a test set while maintaining high fault coverage. The set of production test measurements should include low-cost structural tests such as simple current consumption and only a few more sophisticated tests dedicated to functional specifications such as S parameters, Noise Figure (NF) or IP3.

1. Introduction

The integration on the same System-on-Chip (SoC) of digital, mixed-signal and Radio-Frequency (RF) cores is one of the main challenges in the development of wireless systems for telecommunications and mobile Internet. Apart from the design challenge, the cost of testing these devices is a major concern given the costs of RF testers and the length of test times.

Production testing of RF components generally targets the validation of the functional specifications. Often, market pressures and reduced testing time limit the number of functional specifications that are actually verified during production.

This work is aimed at studying defect-oriented test techniques for RF front-end components with the intention of optimizing production test sets, in a similar way as it has been done in the past for analogue and mixed-signal circuits. Defect-oriented test techniques have been considered in[1][2]. In [1], industrial results of a quiescent current testing technique are presented. The operational method is based on selecting multiple power supply levels and observing the corresponding quiescent current signatures. The main difference with respect to our work is the measurement parameters that are used in order to detect the faults.

In [2], a novel defect testing technique is presented for non-linear RF front end circuits using input impedance matching. A low overhead Built-In-Self-Test solution is presented. However, in our work, a BIST solution is not targeted. Signature testing based on deriving device specifications from generated signatures is studied in [3]. It is based on reducing test cost by using a low frequency Automated Test Equipment (ATE).

Therefore, we have carried out a fault simulation campaign for a Low-Noise Amplifier (LNA) in order to verify the suitability of applying just simple current consumption tests rather than more sophisticated tests directed to measure functional specifications such as S parameters and Noise Figure (NF).

This circuit corresponds to a 0.25 µm BiCMOS Low Noise Amplifier (LNA) that is currently in production at ST Microelectronics. The LNA uses a voltage and a current supply for biasing. The simulations are then performed in a frequency band from 400MHz to 4 GHz.

2. Fault modeling

The fault models that have been considered for the circuit components and their interconnection include catastrophic faults resulting from circuit shorts and opens as it has been done in the past for analogue circuits.

Circuit components include bipolar transistors, capacitors and resistors. For each transistor, short-circuits between the terminals (base-collector, base-emitter, collector-emitter) and opens in each terminal have been considered. For capacitors and resistors, component shorts and opens have been included. Opens have been modeled with a resistance value of 1 MΩ and shorts with a resistor of 1 Ω. With these fault models, and after fault collapsing, a total of 54 faults have been considered in the results of this study. Each fault has been simulated independently from each other.

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3. Fault simulation results

This section presents the results of different fault simulations that have been carried out.

The first results show us that all transistor shorts can be detected by current consumption. It is the most pertinent test in this case. In fact, the fault coverage is 100 %. An explanation is that a transistor can be seen as direct junction and a indirect junction. So when one of these junctions is shorted the transistor effect disappears.

Furthermore, in case of transistor opens, the conclusions are the same as in case of shorts. Thus, current consumption allows the detection of 100 % of the faults for transistor opens and shorts.

In the case of capacitor short faults, it can be noted that all S parameters have the same fault coverage. Some faults can not be detected. For example, one capacitor fault can not be detected by NF parameter. In fact NF depends on the type of input stage of the RF part. So, the capacitor has no impact on the NF parameters.

Concerning capacitor open faults, the results are less relevant than for the other faults. S-parameters and NF have the maximal coverage whereas the current consumption can not detect any of these faults. In fact, at low frequency, a capacitor is equivalent to an open circuit. So, adding an open node will not change its static behavior. Open faults for one decoupling capacitor can not be detected by any of these parameters. This capacitor does not influence the RF part of the circuit. It is used to prevent the RF signal interfering with the power supply.

All resistors in the circuit are used for biasing. For resistor short faults, all S parameters have a fault coverage of 100 %. For each S parameter test, the testing time is exactly the same. So, it can be chosen one of the four S parameters in order to detect short faults in any of the resistors. Some of the short faults in some resistors can be detected by all parameters. Of course current consumption will be chosen, because of its low cost.

So by gathering all these results, it was interesting to study the fault coverage of each parameter and in particular the fault coverage of all combinations of two parameters. These results are next described.

Figure 1 shows the fault coverage for each test parameter. The S11 parameter has the highest fault coverage (89 %). The combined fault coverage of all parameters is about 96 %, which in our case constitutes the highest fault coverage that can be obtained.

Figure 2 presents the fault coverage results for all combinations of two measurement parameters. In fact, the combination of any S-parameter with current consumption (Icc) gives the same coverage than all parameters combined, that is about 96 %. So, in conclusion, a simple measure of one S-parameter with Icc will give the highest fault coverage in theory.

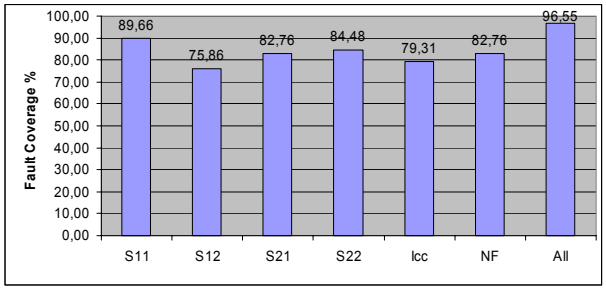

Figure 1. Fault coverage for each of the test parameters.

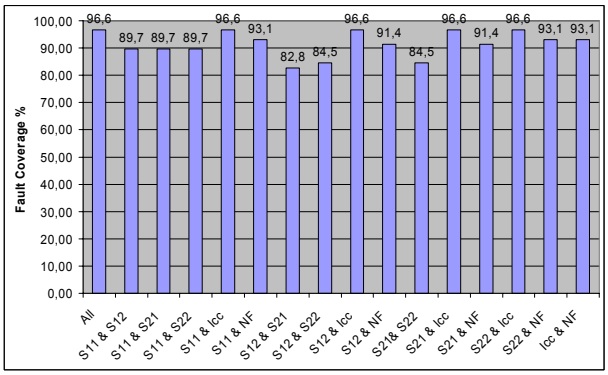

Figure 2. Fault coverage versus different combinations of test parameters.

4. Conclusions

In this paper, we have shown that S parameters have the higher fault coverage. Results of this study indicate that fault coverage of 89.6 % is obtained using only parameter S11. The most important information is that we need essentially the measure of one S parameter and of the current consumption in order to achieve the highest fault coverage (96 %). The measurement of the NF parameter does not seem to be relevant for the detection of catastrophic faults.

5. References

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