Low Power Analogue 90 Degree Phase Shifter

Peter H. Saul, Saul Research
peter@saulresearch.com

Abstract

This paper describes a re-useable circuit module for a 90^0 phase shifter, sometimes called a "Hilbert Transformer", which has been demonstrated on a 0.35-micron CMOS process. The 10-pole circuit is entirely analogue in operation, and achieves measured amplitude and phase accuracy compatible with >50dB sideband suppression. Statistical design techniques assure good functional yields. Total current consumption is 236microamps at 3.3V, and chip area is 1.42 square mm, excluding bond pads. Applications include low power, low cost SSB receivers, more advanced communications architectures in GSM, DCS and G3, and sonar.

1 Introduction

There are many signal processing applications which require accurate phase shifting through 90 degrees, including both analogue and digital radio transmissions. Reference [1] contains a description of several of the architectures which may be used. Potentially one of the most interesting will be Single Sideband (SSB) reception. International agreements provide for the cessation of amplitude modulation (AM) broadcasts by 2010. There are digital replacements such as Digital Audio Broadcasting (DAB), Digital Radio Mondiale (DRM), and satellite-borne FM/digital modulation. However, conventional single sideband, either with reduced carrier (SSB-RC) or suppressed carrier (SSB-SC) is a viable, low cost approach suited to low-technology infrastructures. The 90-degree phase shifter may also be modified to produce any relative phase angle between the two outputs.

Currently, filtering in communications systems uses a wide range of techniques, including ADC/DSP approaches, [2, 3]. These tend to be chip area and power intensive. Analogue structures such as gm-C filters and MOSFET-C filters also work well, but have control issues, and in some cases dynamic range problems [4, 5]. The alternative, described here, is to design an analogue circuit which allows for process variation by spreading errors across many components, and then accept if necessary a test stage drop-out. Modern process yields are such that this may be achieved at minimal cost. The positive benefits of the techniques described are in very low power consumption and small chip area; the area required by the phase shifter to be described is approximately that of a single 8 bit ADC.
The chip photograph is shown in Figure 9, which has been placed after the text. The process used was austriamicrosystems C35. This is a 0.35-micron minimum feature size "analogue" process, i.e. it offers high value resistors, polysilicon capacitors and active devices with high output impedance.

This latter point is important in that faster and smaller geometry processes are available, but are only "digital". In principle, the differences are small, but a key issue is that low active device output impedance, typical of a digital process, compromises analogue stage gain. In precision analogue circuits, the provision of near-ideal operational amplifiers is essential for predictable and repeatable operation. True analogue processes can be used for the design of two-stage op-amps with open-loop gains in excess of 70dB, while digital processes limit similar circuits to 50dB or less. It is also very useful to have accurate resistors and capacitors which can be realised in acceptable chip areas.

2 Operational Amplifier Design

Where the new process is significantly better than older generations of analogue process is in the active device operational speed. The opamps used in this circuit operate at 7MHz unity gain bandwidth and 22 microamps current, at 3.3V supply. Opamps on the same process run have been simulated at up to 1GHz unity gain bandwidth.

The core circuit of the opamp is shown in Figure 8, also located after the text. The circuit consists of a P-channel input pair, M9-M10, with N-channel current mirror loads and P-channel tail. The level shift stage, M4-M5-M11-M12 drives the gate of the output P-channel M13, while the output N-channel, M6, is driven directly by M10. This circuit will operate down to a supply voltage of 2.5V or less quite satisfactorily, depending on the threshold voltages. Not shown on the circuit above are the output phase compensation blocks and the input stage bias block. The former provides >60 degree phase margin when operated into modest loads, e.g. 5pF. It is thus capable of driving off-chip if required. Higher current versions can

1530-1591/04 $20.00 (c) 2004 IEEE

stably drive 30pF loads. The bias block provides threshold and temperature tracking of the bias currents, and a switch-off feature which powers down the op-amp to sub-5nA level. Although not fundamental to the operation here, this feature is included in many recent opamp designs.

3 Measured Opamp Performance

The bandwidth performance of the opamps was >6MHz at 22 microamps total current, including bias. The opamp was configured as a x10 gain block to assess noise and offset voltages; true open loop gain proved difficult to measure, but was shown on higher current versions to be very close to the designed 90dB.

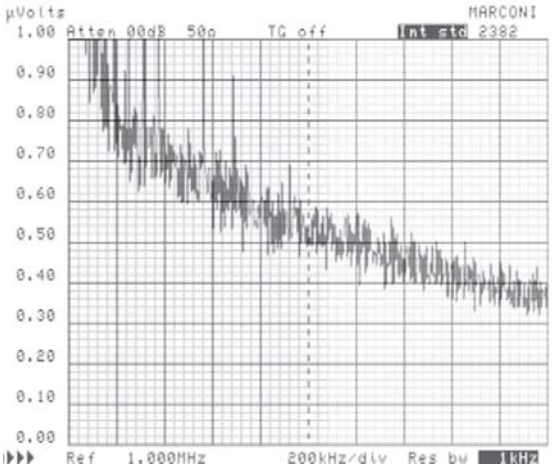

Figure 1, Noise performance of Opamp.

Noise in the individual opamps was comparable with "discrete" CMOS opamps. Figure 1 shows the noise output, follower connected, in a 700Hz video bandwidth. Although the right side of the plot is not quite at the flat noise condition, it corresponds to 0.4 microvolts in 700Hz, i.e. 15nV per root-Hz. Most samples from a group of 10 units were similar, although one device was much worse.

Offsets in the opamps were minimised by layout design. Mean value from 10 samples was 0.74mV, with 4.38mV standard deviation. Such a small sample should not be over-interpreted, but it does appear to show that there is not more than a small systematic offset, and an acceptable random variation. In a complex circuit, post-process trimming is unlikely to be available, so it was essential to maintain offset variations within manageable proportions to allow circuits to operate without external intervention, and on a production basis. In the circuit described in this paper, small DC offsets are not important.

4 Hilbert Transformer Design Concepts

The conventional frequency range for communications audio is 300Hz to 3kHz. However, to minimise phase and amplitude errors while allowing for process variation, it was determined that a wider range, 150Hz to 8500Hz, should be used. Nominal design parameters were:-

Phase error <+/-0.1degree
Amplitude error <+/-0.1dB.

This requires a 10-pole filter design. An attraction of this approach is that *random* component errors represent a relatively small overall error, while *systematic* component errors, e.g. resistor or capacitors all off-norm, represent a filter centre shift. Since each band edge provided was at least an octave beyond that necessary, no additional amplitude or phase errors will be incurred by process changes within the specified limits.

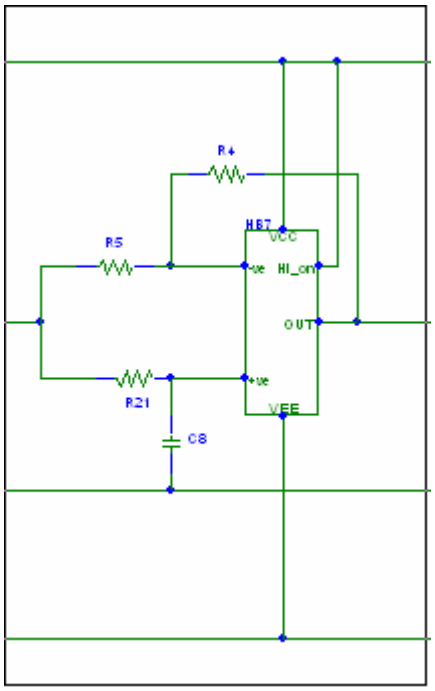

Figure 2, Filter, Single pole.

Each filter pole was determined by a resistor-capacitor-opamp configuration as shown above. The box in the diagram is the opamp as in Figure 8. The switch-off facility ("Hi-on" on the diagram) was provided by a single control line to all opamps. Resistors R4 and R5 determined the stage gain, nominally x1, and were typically 100kohms. This value was a compromise between chip area, additional current in the dynamic state, and stage bandwidth. The latter is important in that additional phase delay must be avoided. The ten poles are arranged in two groups of five, such that the phase shifts

from finite opamp bandwidths were equalised as far as possible.

The most critical components after the opamps were the resistors and capacitors equivalent to R21 and C8 in Figure 2. Since the pole frequencies must go down to 250Hz, large values were required. Each stage had a nominal 50pF main capacitor, while the lowest frequency stages had two or four such capacitors in order to limit the resistor value to less than 20 megohms. The layout is shown in Figure 9. The cellular structure is evident; each section of the filter used an identical core, with variations for the resistor value, and in the case of the lowest frequency sections, the addition of capacitors. It is clear that alternative poles for the design could be easily arranged, and indeed more sections could be added. This latter possibility is attractive if a wider passband is required, or if greater accuracy in the passband is needed. This would be achieved using a higher order filter which in effect would spread errors over a greater number of components.

5 Monte Carlo Analysis

In practice, all processes have parameter variations, and it was essential to take these into account if a design core was to be suitable for repeated use. In addition, high resistivity components, usually in low-doped polysilicon, tend to have relatively high, usually negative, temperature coefficients. Typical values for resistors in SPICE format are:-

TC1=-1.2E-3
C Lot=10%
C Dev=0.01%
R Lot= 10%
R Dev=0.3%

Over the frequency range of interest, the simulated amplitude error was always small, at 1 milli-dB. The phase error remained within a 200 milli-degree band. The simulated result is shown below, for a 100-pass Monte-Carlo simulation of all variables. Calculations at the design stage showed that the sideband suppression should be -54dB. This is a good, although not excellent, figure.

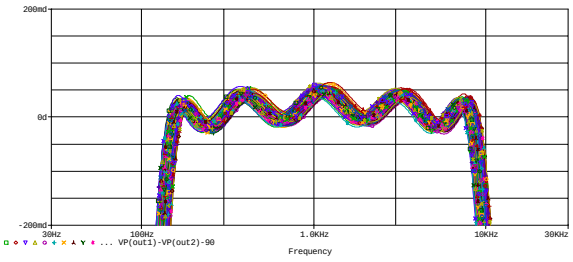

Figure 3, Simulated phase variation

6 Layout Considerations

Layout of the opamps was based on known successful configurations at 0.8 microns; these were reduced to 0.35 micron dimension devices with minimal changes.

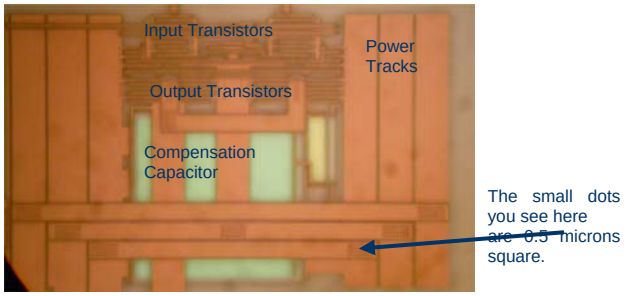

Figure 4, Single opamp, including power tracks and compensation capacitor.

The opamp layout above shows that the opamp area is dominated by the compensation capacitance. In addition, tracks suitable for power provision in an opamp array take up significant area too. At the scale shown, the contact holes, 0.5 microns square, are just visible on the power tracks. For convenience of filter design, the supplies were +V, 0V, -V, where V was 1.2V to 1.8V. Most measurements were made at +/-1.65V, i.e. suitable for operation on a 3.3V supply.

The filter capacitors, which are visible in Figure 9, consisted of parallel plates of POLY1 and POLY2. The long-thin aspect ratio meant that connection to the capacitance included less than 1 square of POLY1 and POLY2 series resistance. In addition, all capacitors were identical in layout, using a single cell. It was not practical to add “dummy” cells for each capacitor.

The resistors were more variable and potentially subject to greater errors.
Possible error terms were from:-

1) End errors. These were similar for all resistors.
2) Contact resistance. This was taken care of by the resistor array techniques described above.
3) Effective width variation.
4) The temperature coefficient, -1.2e-3/degree C, was acceptable for many applications.

The design was clearly a multi-dimensioned compromise in respect of resistor design in particular.

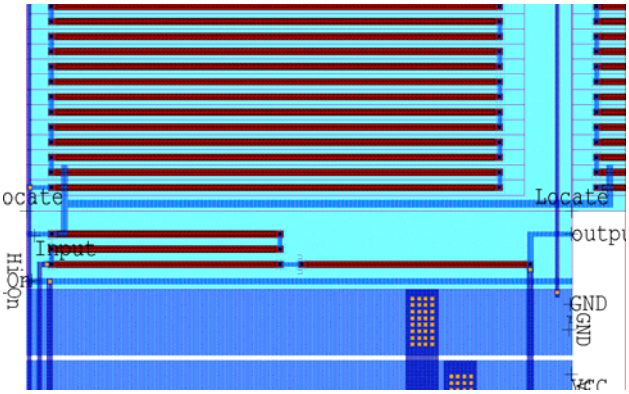

Figure 5, Resistor Examples

The compromise values are in part illustrated in Figure 5. The lower part of the main array of resistors for this cell are in the centre. The unit resistor size was nominally 100kohms. Just below this group are the feedback gain setting resistors for this cell, 2x100kohms, realised as 2x50kohms each. All resistors were 1 micron in width. The "long-thin" resistors at least removed length as an effective variable, although width remained. No "dummy" cells were used.

7 Measured Results

Measurements were made using a Powertek 102 Gain-Phase Analyser. This had a frequency capability to 2MHz. Although specification error limits for the full frequency range were comparable with the measurements required, self-calibration of the equipment in situ suggested that the actual measurements were of adequate accuracy and repeatability at this low frequency end of the range, such that measurement error was not regarded as a problem.

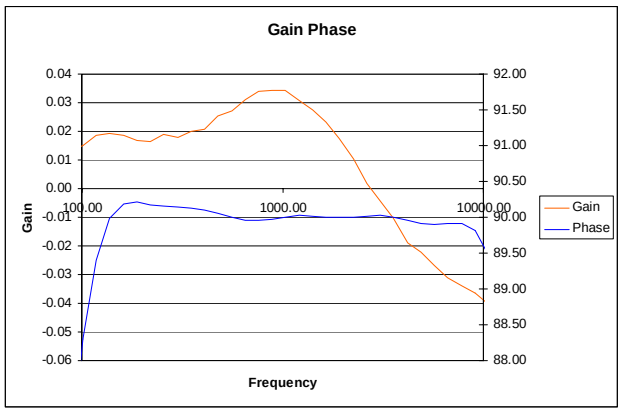

Figure 6, Measured Gain and Phase Response of full Hilbert Transformer.

A specific device response is shown above. This demonstrated a gain response error of 7 to 10 milli-dB over a wide frequency range. Phase error in this case was between -0.1 and +0.2 degrees. Other devices, from the sample of 10 measured, showed broadly similar results, although this was the best of the sample.

In the SSB receiver context, it is possible to determine, from phase and gain accuracy, a figure for projected suppression of opposite sideband, assuming an ideal mixer and accurate local oscillator phase shift.

The formula used was:-

$$S := 10 \cdot \log\left[\frac{\left(1 - 2 \cdot a \cdot \cos(p) + a^2\right)}{\left(1 + 2 \cdot a \cdot \cos(p) + a^2\right)}\right]$$

where a= amplitude voltage ratio
and p=phase imbalance in radians

The predicted SSB performance of the chips may be plotted for all the devices tested.

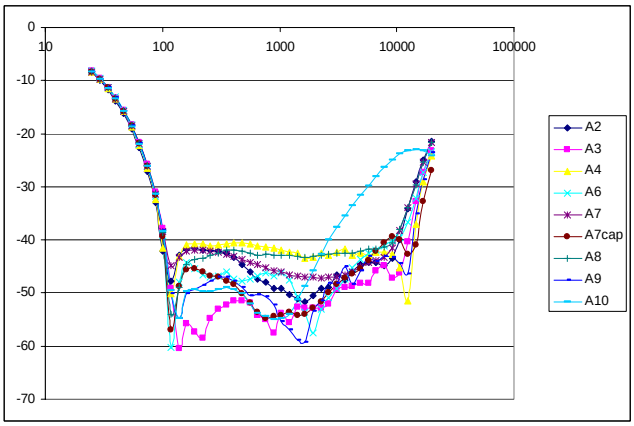

Figure 7, Sideband Suppression plot

Figure 7 above illustrates this data extraction. Of the sample of devices, all would meet a specification for opposite sideband of -42dB at all points, while the best met the design target of -54dB over most of the range.

A sideband suppression of -40dB is useable in a single sideband receiver, but not so in a transmitter. Potentially, minor errors can be corrected externally, but this is undesirable. The source of the errors was thought to be primarily opamp variation. Discrete versions of the opamp showed variations in current and hence gain-bandwidth product for this low-current variant. Higher current versions were much more uniform in characteristics, so that a revised version of the circuit would operate at two or three times the current of the present circuit, but with SSB suppression of >54dB for most or all of the production.

8 Conclusions

This paper has presented the first results on a fully integrated analogue Hilbert transformer. Statistical analysis of the circuit was largely supported by the measurements, although it was shown that the first pass design should be slightly revised to further improve performance and repeatability for quantity production.

Novel aspects of the design included the use of an analogue 0.35 micron CMOS process, with no post-process trimming to achieve the desired results. Integration of very high values of capacitors and especially resistors on-chip has been shown to be fully reproducible; the errors noted are very small in absolute terms. The circuit offers simplicity of function, low noise, low power operation and small chip area, especially when compared with an ADC/DSP equivalent.

The 90-degree phase shifter can also produce arbitrary phase differences between two outputs. This has applications where controllable, usually variable, phase is required, e.g. in sonar.

The phase shifter is available as a design cell for the austriamicrosystems C35 process. Individual opamps are also available, as is an audio-frequency 4-pole band-pass filter covering the same frequency range. A second version for the similar X-Fab process is under consideration.

9 References

[1] Abidi, A.A.; "Direct-conversion radio transceivers for digital communications" Solid-State Circuits, IEEE Journal of , Volume: 30 Issue: 12 , Dec. 1995 Page(s): 1399 -1410

[2] Chang, P.J.; Rofougaran, A.; Abidi, A.A.; A "CMOS channel-select filter for a direct-conversion wireless receiver" Solid-State Circuits, IEEE Journal of , Volume: 32 Issue: 5 , May 1997 Page(s): 722 -729

[3] Ryynanen, J.; Kivekas, K.; Jussila, J.; Sumanen, L.; Parssinen, A.; Halonen, K.A.I.; "A single-chip multimode receiver for GSM900, DCS1800, PCS1900, and WCDMA" Solid-State Circuits, IEEE Journal of , Volume: 38 Issue: 4 , April 2003 Page(s): 594 -602

[4] Porret, A.-S.; Melly, T.; Python, D.; Enz, C.C.; Vittoz, E.A.; "An ultralow-power UHF transceiver integrated in a standard digital CMOS process: architecture and receiver" Solid-State Circuits, IEEE Journal of , Volume: 36 Issue: 3 , March 2001 Page(s): 452 -466

[5] Yoshizawa, A.; Tsividis, Y.P.; "Anti-blocker design techniques for MOSFET-C filters for direct conversion receivers" Solid-State Circuits, IEEE Journal of , Volume: 37 Issue: 3 , March 2002 Page(s): 357 -364

[6] RF and Microwave Handbook, ed. M. Golio, ISBN 0-8493-8592-X, p. B-19.

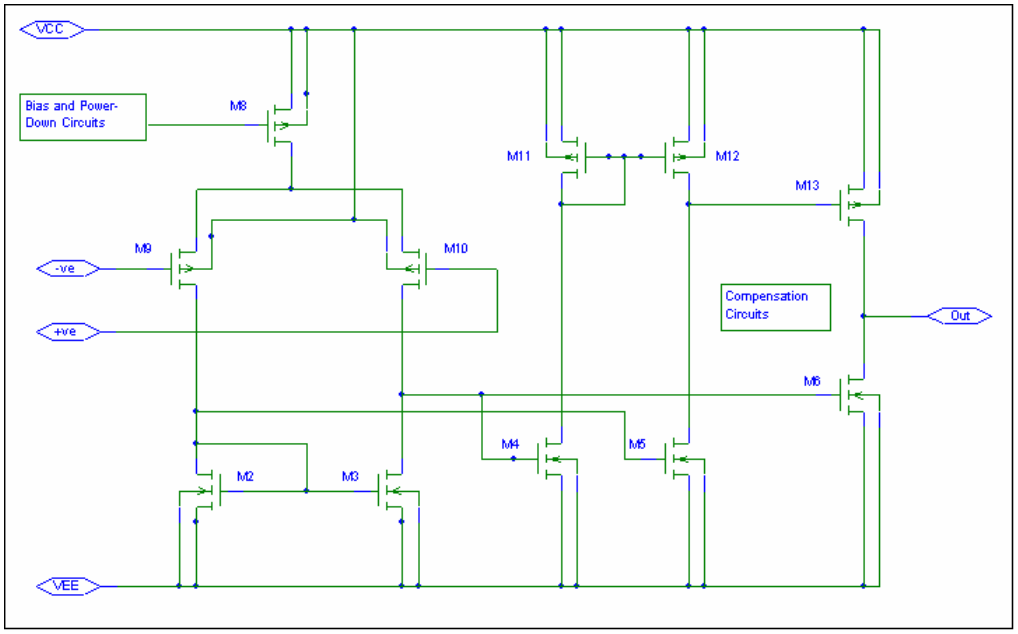

Figure 8, Opamp core circuit.

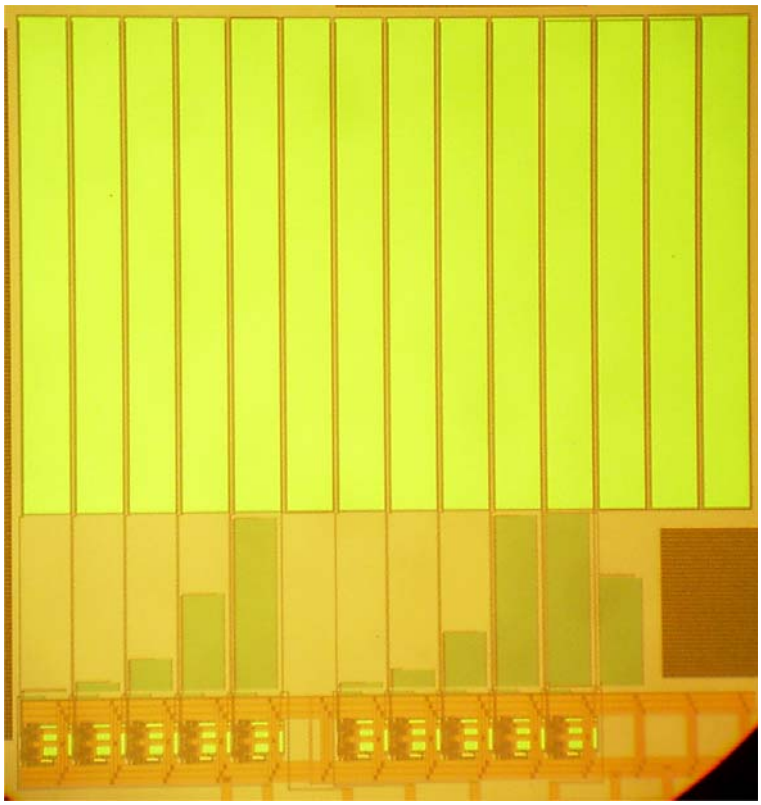

Figure 9, Chip Photograph. 1.2mm x 1.2mm module, excluding bond pads.