Demonstration of a SiGe RF LNA Design using IBM Design Kits in 0.18um SiGe BiCMOS Technology

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Abstract

A 1.5GHz-2.0GHz Low Noise Amplifier (LNA) is designed in IBM 0.18um BiCMOS technology using IBM design kits in Cadence Design Flow. The fabricated LNA chip is packaged and tested. The measured results (gain, noise figure, and IIP3) correlate with the simulation very well. The results demonstrate that IBM SiGe technology, Modeling, Design Kits and the Cadence design flow are solid and accurate for RFIC design.

Introduction

A cascode low noise amplifier (LNA) at 2V power supply has been implemented in 0.18um IBM SiGe BiCMOS technology. The circuit is highly integrated with ESD protection circuits. The die is packaged and mounted on the test board. The measured data show that power consumption is less than 12mW. It provides a forward gain (S21) of 20dB with a noise figure (NF) of only 1.2dB at 1.6GHz and also provides S21 of 15dB with a NF of 2.2 dB at 2 GHz with off-chip re-matching.

This paper also shows the design method for LNA design with low breakdown high F_T bipolar devices. It briefly describe a way to pick the device and select the suitable size for general LNA design. In this work, the cascode LNA circuit design is targeted at 2GHz. After the fabrication the die was packaged in QFN16 and mounted on a FR4 - 4 layer test board. Because the room size of the package we have is much bigger than the die size, the final operating frequency is shifted to 1.6GHz due to the huge parasitics of the package. However, it is possible to the shift the operating frequency back to 2GHz by adding additional shunt capacitor and resistor on input and output terminals respectively. For both 1.6GHz and 2GHz case, the test results show a good agreement between the measurements and the simulations, which validate both the non-linear models of the active devices and the method used by the commercial software.

Sige HBT device parameters

Low base resistance, high gain and high Early voltage make the SiGe HBTs ideal for analog and mixed-signal applications [1]. The offering high F_T, low base resistance bipolar device in 0.18um SiGe BiCMOS technology makes it feasible to design a cascode bipolar LNA by 1.8V or 2V power supplies. For that device, both the vertical scaling and lateral scaling are used to reduce the base width and the base resistance, which made a significant noise improvement of the device performance.

It has been found out in [2] that the NF_{min} is a weak function of device size but primarily a function of the bias current density . When biasing at the minimum noise figure point, the available gain from the transistor is a function of the device size. The relationship of NF_{min} to key transistor parameters can be shown by equation [3]:

$$NF_{\min} = 1 + \frac{n}{\beta_{dc}} + \sqrt{\frac{2I_c}{V_T}(r_e + r_b)\left(\frac{f^2}{f_T^2} + \frac{1}{\beta_{dc}}\right) + \frac{n^2}{\beta_{dc}}} \qquad (1)$$

Obviously, from the equation, the NF_{min} can be improved by increasing β_{DC}, f_T, or decreasing the r_b. Because the base resistance will decrease as the bias current increases, the NF_{min} will first decrease as the biasing current increases in the low current region and will increase when the shot noises from the bias currents start to dominate the noise figure. With the high speed, low-noise and low-power capabilities (trading off excess speed for reduced DC current), the minimum emitter width SiGe HBT transistors have low NF_{min}, making them suitable for LNA design.

The IBM SiGe HBT transistors are close to optimum design for simultaneous noise and input return loss matching around 2 GHz[2]. When an appropriate value of

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emitter degeneration inductor is used, the simultaneous noise and input return loss matching can be achieved. In this work, 0.55nH-emitter degeneration is chosen for the noise and impedance matching. And the 0.20µm emitter width, high performance HBT devices are using for the cascode LNA. This device features 2V BVceo and 120 GHz f_T, based on the 0.18um SiGe BiCMOS process of IBM technology.

Fig. 1 shows the NF_{min} of minimum emitter width, 0.20um width, 10 multiplicity HBT in 0.18um SiGe technology versus base current density with Vce 1 volt. When biasing at fixed current base density, the available gain from transistor is a function of the device size. Moreover, the available gain is also associated with the current density. Fig.2 shows the associated gain as a function of emitter length for the transistors when biasing at the different current density. From Fig. 1 and Fig. 2, it can been seen that there exists trade off between minimum noise figure and maximum gain for device size and bias point.

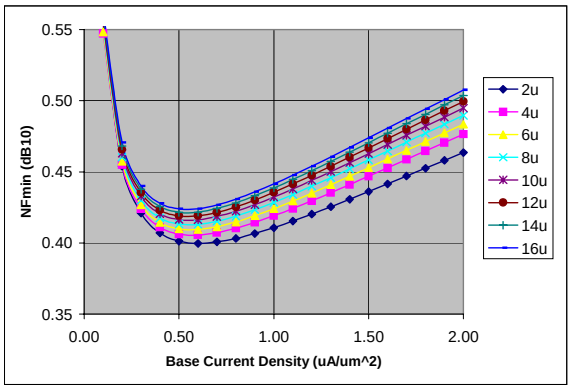


Figure 1. IBM SiGe 7HP HBT n2bv0p2: NF_{min} versus base current density with emitter length parameter (Vce=1V, m=10)

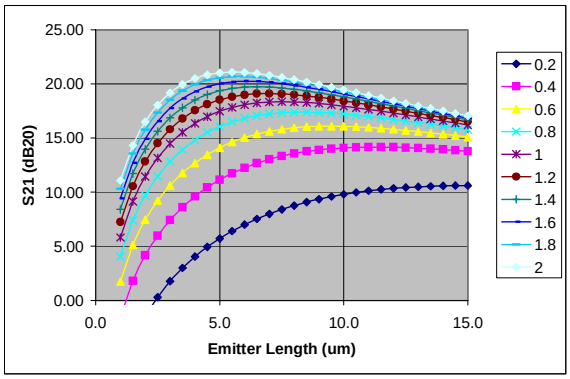


Figure 2. Associated gain versus emitter length for the transistors with base current density in figure 1.

LNA design

The major specs of the LNA are input/output source impedance matching, noise figure, and forward transconductance gain. Furthermore, the IIP3 of the LNA should be maximized. Fig. 3 shows the schematic of the LNA. The LNA circuit used is a cascode configuration that reaches high unilateral levels. Surround the circuit there are bondpads and ESD devices. All signal and supply pins are protected against ESD. Especially, the Input and Output ESD are using DoubleDiode_RF_5GHz ESD devices that are offered by IBM Design kit. The parasitic of the ESD are also counted into the design. To implement 0.55nH-emitter degeneration, double bond pad/wire are used on the emitter terminal.

Cascode configuration has the advantage of high gain, low noise and is a very stable circuit providing large isolation and large frequency bandwidth. The cascode transistor Q1 provides the gain and the Q2 drastically reduces Miller effect, significantly lowering the input capacitance seen at the input node and output nodes, which provides a large isolation. For the 2V power supply design, the DC point between Q1 and Q2 is biased at 1V, which benefits the maxim dynamic range from the 2V breakdown devices. Referring to the Figure 1 and 2, we chose a device with size of 10x0.2µmx8µm as the low noise device and bias it at ib = 1.2µAx10x0.2x8 = 19.2µA. At that base bias point, the collect current is about 5mA. At that size, the device Nfmin is about 0.45dBm and Gain is about 18dB.

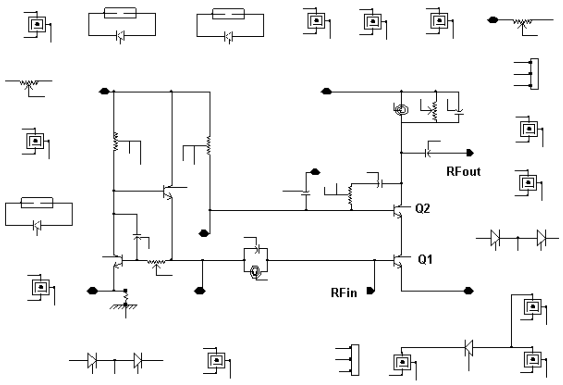


Figure 3. The schematic of a cascode LNA configuration with bond pads and ESD devices.

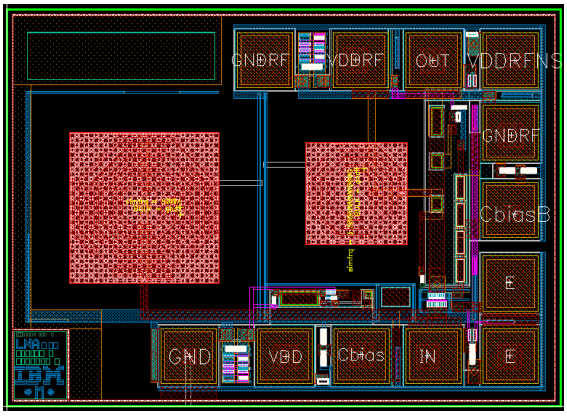
The inductor connecting the base of Q1 and the bias circuit is used for RF blocking. This inductor blocking will provide noise and linearity advantage comparing to resistor blocking [4]. The linearity is enhanced because the inter module frequency will get a low impedance at

the base point. However, the on-chip inductor feed bias circuit has an area consumptive as a trade off.

Because the Q of the on-chip components would result in unacceptable NF degradation, so off-chip external matching components are needed in the RF input. A series off-chip inductor of 5 nH and a series 10p capacitor are used.

The whole design has been done using IBM analog and mixed signal (AMS) design kits in Cadence Design Systems. The design cycle flow including parasitic extraction and re-simulation. The parasitic extraction of IBM AMS design kits are only related to the interconnect parasitics, and not device parasitics. In general, device parasitics associated with design-kit-supported devices are modeled within the supplied device models. The critical RF path has been designed widely enough to minimize the effected of the parasitical resistance. Moreover, to get better noise isolation, NS back plane are chosen for mim cap, bondpad, and the RF path. So there has huge parasitic capacitance existing in this circuit. The design was calibrated by the Diva Coeffgen with Rp parasitic extraction resimulation. Actually the Rp effect can be totally ignored for this design and the comparison results will be shown later.

The circuit has been fabricated on a multi project wafer at IBM Microelectronics. The layout and photo snap of the circuit is presented in Fig 4. The Die size is about 1.15x0.85 mm^2. The chip is packaged mounted on 1"x2" FR4 4 layer board. The package used is QFN16 with 3mm x 3mm body room. Since the distance between 2 facing pads of QFN16 is about 4mm, comparing the distance of 0.8mm between chip input and output pads, the bound wire inductance is much bigger and shifts the LNA operating frequency dramatically.



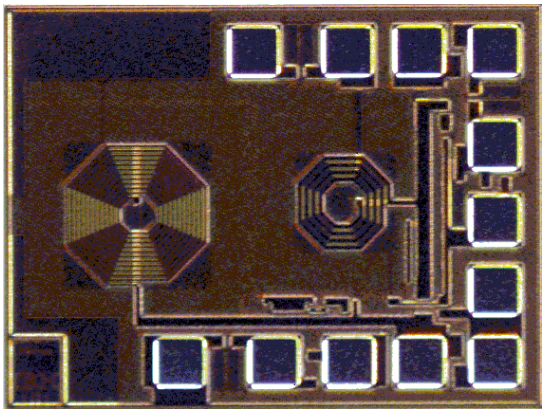


Fig. 4 Layout and die photo of the LNA

Result and measurement

The LNA was targeted at 2Ghz operating frequency with voltage supply of 2V. Total current consumption is less than 6mA including biasing circuit. As it mentioned before, due to the large parasitic of the package, the operation frequency will shift to 1.6GHz. However, nevertheless, with equivalent model circuits of the package and the external components, the testing result still shows a good agreement between data and the simulation. The Equivalent SPICE model circuit of the package is shown in Figure 5 and the external component model is shown in Fig 6.

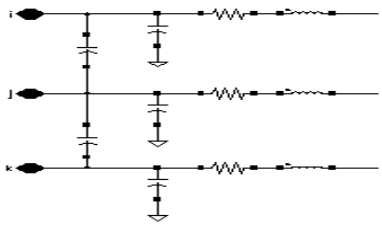


Figure 5. The Equivalent SPICE model circuit of package

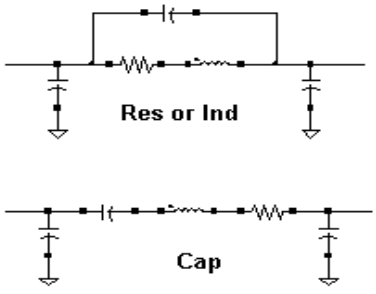


Figure 6. The equivalent model circuit of external off-chip resistor, inductor and capacitor components

The Figure 7 shows a comparison between the measured and simulated S-parameters from 1 to 3 GHz for the LNA. The testing result shows the operating frequency is at 1.6GHz. The gain of LNA at 1.6GHz is 21 dB, the input return loss is 9.3dB and the output return loss is 17.4 dB. The input/output isolation is better than 35dB. The measurement data fit the simulation curves well, however, the S22 and S21 data doesn't agree accurately. The reason of the shift is due to a lag of the load inductor in layout, which is shown in figure 8. The RF power bus go through under the inductor that increase the inductance and parasitics that decrease the resonant frequency. Hence the S22 is shifted to low frequency due to the low resonant frequency.

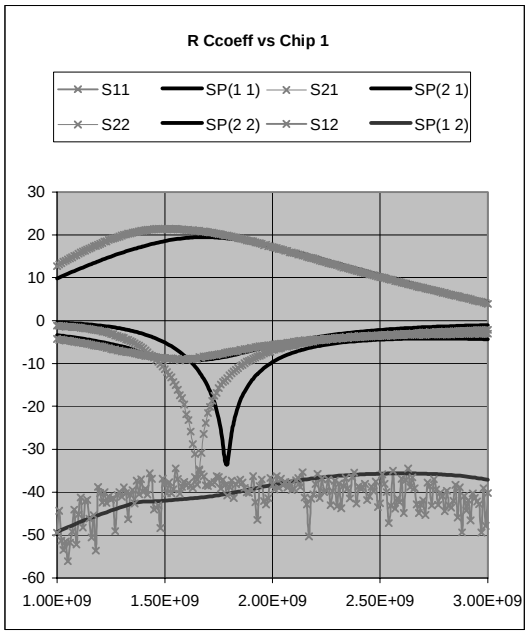


Figure 7 The simulated and the measured S parameter for the low noise amplifier from 1 to 3 GHz

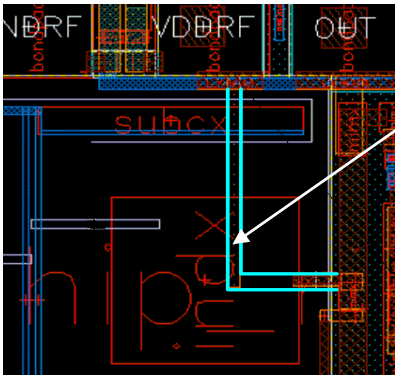


Figure 8 The RF power bus under the inductor increases the inductance and parasitics and decreases the resonant frequency.

It can be added about 0.55nH to the load to represent the extra effect of the extract lag of the inductor. With this correction to simulation, a very accurate simulation vas measurement result can get in the Fig 9.

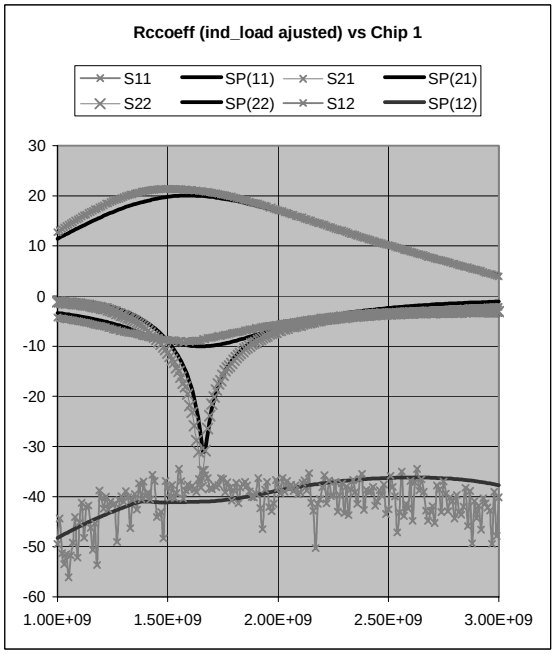


Figure 9 The simulated and the measured S parameter for the LNA from 1 to 3 GHz. The load inductance has been adjusted due to the case in layout shown in Fig. 8.

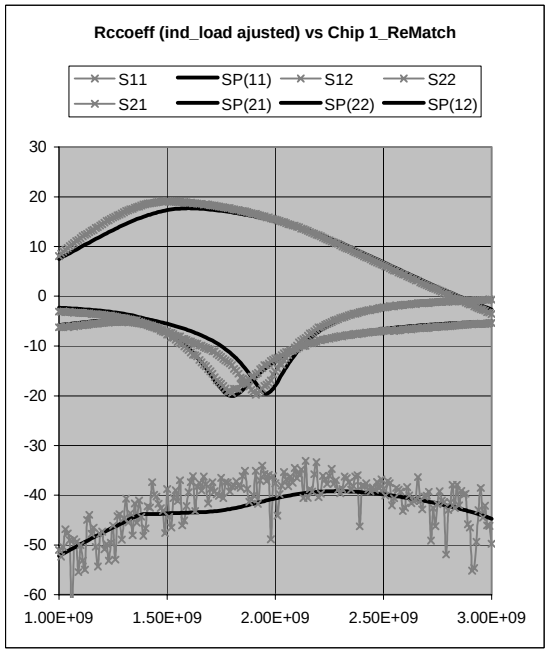


Figure 10 The simulated S parameter for the amplifier from 1 to 3 GHz for the tuned LNA.

This LNA can also be tuned to high frequency after adding a 1p shunt cap and 100Ω shunt resistor at input and output respectively, Figure 10 shows the operation frequency can be shifted back and can cover 2GHz. Again, the testing result agrees and the simulation result very well. It validates the non linear model of the active devices as well as the method of design cycle flow.

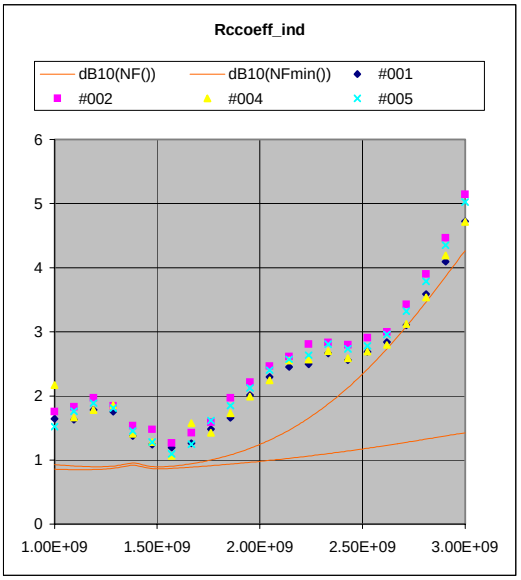


Figure 11. The measured noise figure vas simulations results. Multi chips have been measured.

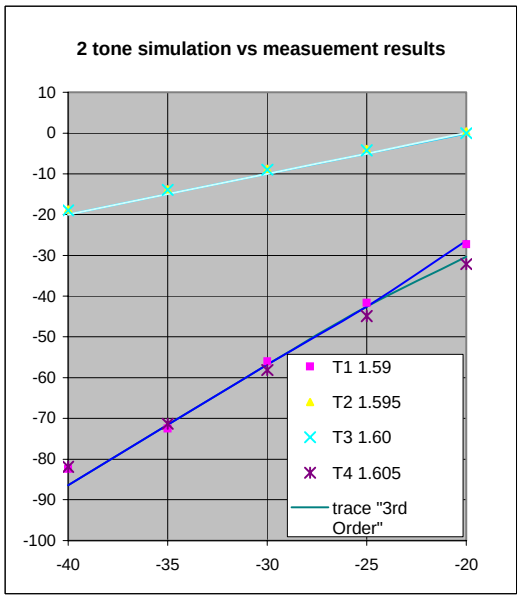


Figure 12. The two carrier third order inter-mods at the output port

Figure 11 shows the measured and simulated noise figure for this design. The measured NF is 1.2dB at 1.6GHz and 2.2dB at 2GHz. Which is closely matched to the simulation results. Figure 12 shows two-carrier third-order inter-modulation measurement and simulation results. The measured IIp3 is –6dBm at 1.6 GHz. The linearity data also has great correlation between the hardware and simulation.

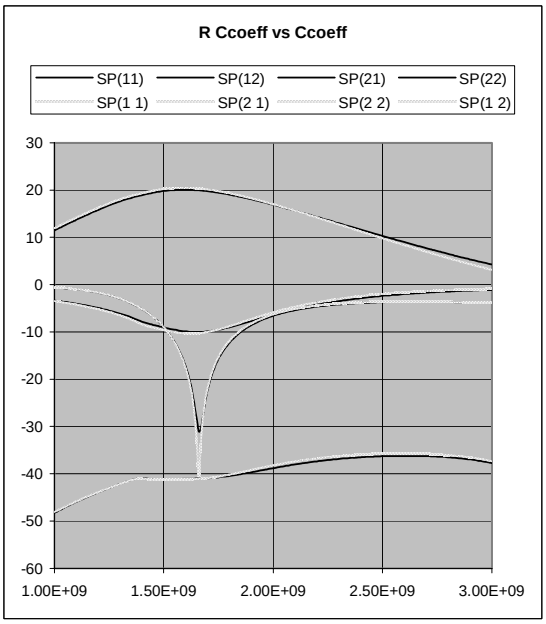


Figure 13. The comparison results for using Rp and Ccoeff parasitic extraction view and using Ccoeff extraction only.

Finally, as we mentioned before, the simulation results we used for above comparison is based on the layout with both R and C parasitic extraction. Since the critical RF path have been deigned wide enough and the NS back plane are used for the paths, mim caps and pandpads, so the parasitic capacitors dominate the parasitic effect. Actually the Rp can be totally ingnored for this LNA simulation. The comparison results for using Rp extraction and without using Rp are shown in Figure 13.

Conclusion

This work demonstrates a cascode low voltage low noise LNA design with the device selection method with IBM 0.18um BiCMOS technology. This paper presents the design and the characterization of a low noise

amplifier for 1.5G and 2GHz range with 2V-voltage supply. It also outlines the good agreement between the measurement and the simulations, which validate both the device modeling and the method used by commercial software and IBM Design Kit.

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