Hot topic session:
RF Design Technology for Highly Integrated Communication Systems

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Abstract

The characteristics of highly integrated High-Speed Data-Transmission-Systems for near future communication standards are high mobility, low power, reliability, high performance, low cost and short development time. Recent available RF development tools do not allow the efficient design of tailored, well partitioned, highly integrated, high datarate communication systems targeting up to 6 GHz carrier frequency. Reasons for this are the missing flexibility and accuracy in the hierarchical design process from system down to physical level. In this session representatives of system houses, a leading EDA provider and a silicon foundry will introduce and discuss the challenges related to the specific areas. Considering the market relevance of high data rate wireless communication systems the missing overall design technology today is a real hot topic.
Suggestions on how to improve the existing situation addressing the design technology as a whole will be discussed. Depending on the representatives perspective converging requirements will be worked out and non-converging requirements will be debated in a controversial manner.

1. Motivation and Context

For future wideband telecommunication systems with integrated RF-front-ends we need higher abstraction levels and more precise behavioural models considering process and package physics at the same time.

Therefore, existing methodologies, flows, tools, modeling and process interfaces have to be improved. These are not separated domains, since they are influencing each other. The practice to collect best tools and to define a flow on top of it (state-of-the-art) becomes very risky for the development of future communication systems since bottom up verification becomes extremely difficult and the top-down design process may be unable to reach the physical implementation level. Reasons are the non-optimized interfaces between system, circuit and device physics level. This reduces reliability and, therefore, increases the probability for a required redesign, limits reuse and increases the development time. Not less important is the fact that system developers have no chance to address the full capability of modern processes.

Therefore, three different perspectives (system house, EDA provider, technology vendor) will be presented in order to reflect the interface problem and also to discuss existing solutions controversy. In the first presentation an overview of todays challenges in the design of highly integrated mobile transceiver systems with focus on WLAN from System House perspective will be given. Bottlenecks in existing work flows using various tools will be pointed out. Demands for improvements of the design technology for near future high data rate wireless Communication Systems will be discussed. A new design flow solution from a leading EDA provider shown in the second presentation addresses the existing design challenges. A new, verified design flow for WLAN applications considering system architectures provided by several system houses will be introduced. In this flow a new testbench approach speeds up the design process in presence of higher modeling accuracy and increasing system complexity. The role of the silicon foundry in improving the existing design technology by providing an enhanced interface to modern process technologies is addressed in the third presentation. A more flexible and more accurate utilization of modern BiCMOS and Bipolar processes (e.g. SiGe2/ATMEL) has become available by using a special implementation concept for introducing the geometry-scalable bipolar compact model HICUM to a conventional design kit.

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2. Demands on RF Design Technology for Near Future High Data Rate Wireless Communication Systems from System House Perspective (R. Wittmann, G. Tränkle)

In this section, an overview of today's challenges in the design of highly integrated mobile transceiver systems with focus on WLAN (IEEE802.11a, Hiperlan2) will be given. Especially the design of an embedded RF-Front-End (Fig. 1) is a demanding task of special relevance. Bottlenecks in state-of-the-art RF-system design work flows using various high quality tools will be pointed out. Demands for improvements for the development of near future high data rate wireless communication systems will be discussed.

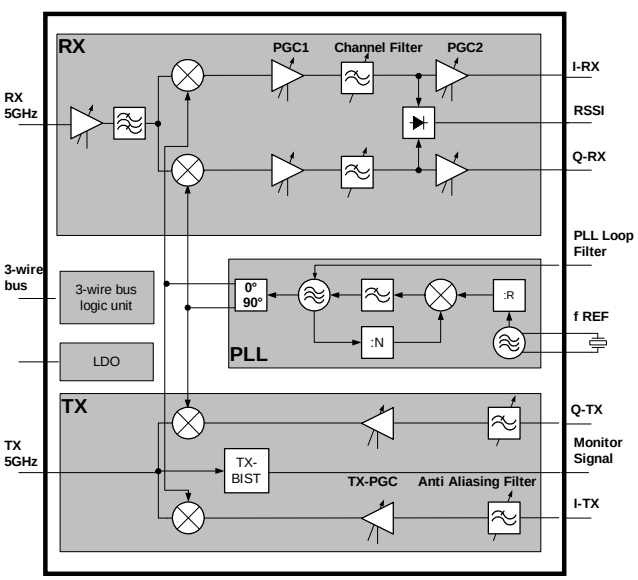

Figure 1: *Block Diagram of an integrated WLAN Transceiver Front-End (Source: Infineon Technologies AG)*

The major demands address the seamless integration of following aspects into an application oriented design flow:

- the interactive semi-automated design assistance using advanced testbenches
- an improvement of modeling precision on all levels of design in spite of increasing system complexity
- RF-oriented interfaces to CMOS and BiCMOS process technologies (Design-Kits)

One of the biggest challenges to be successful with future product developments will be the accurate scheduling of the design milestones. If a market analysis figures out the required performance profile for a planned product, then besides fulfilling the specification conformity, the on-time introduction to the small market window is of high relevance. Current technology platforms and commercially available design tools enable in principle the design of monolithic integrated solutions of complex wireless transceivers. But the actual challenge is to do it faster and with a higher design security and time security than today.

New tools should clearly support the above targets of a reliable, highly determined IC-development. As a evaluation platform the 5GHz ISM-WLAN covering IEEE802.11a and Hiperlan2 is utilized within the HGDAT project [1]-[4]. Within this platform parameterizable formalized simulation instructions (testbenchnes), which are executable, have been defined for system refinement and verification. These modeling testbenches offer a seamless Top-Down/Bottom-Up simulation environment, using different abstraction levels [5]. With this scenario most of the design steps, beginning with system level specification, can be covered with the desired accuracy. Nevertheless, one missing step is the verification of the system specification conformity on hardware level with the appropriate physical interfaces. This aspect has to be investigated more in the future. The idea is to combine all available information from active and passive elements (including parasitics) within the simulation testbench and add the hardware verification results. This yields a lot of additional information during the design cycle. With this information the lack of critical design parameters can be calculated. In a next step it should be possible to center the design by using Built-in-Self-Test (BIST) and Built-in-Self-Correction (BISC) functionalities (e.g. [6]). The result is a faster, highly determinable design flow. Fig. 2 shows the interaction of the simulation and verification cycle.

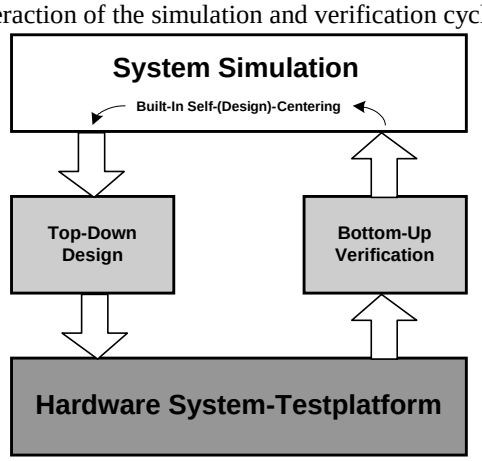

Figure 2 : *Interaction of the Simulation- and Verification Cycle*

In order to ensure that the new proposed design flow works out the sophisticated vision, some assumptions have to be considered:

- all relevant parameters of the system specifications must be expressible by appropriate stimuli
- a seamless simulation and verification testbench of all analog and digital functions must be available for the transmit- and receive chain
- all influence-taking interfaces and environment parameters must be included
- Models for technology variations must be available

A design flow tailored like this does not only enable faster and more secure developments, it could also be a key element in future multi-mode solutions, e.g. UMTS with IEEE802.11b-WLAN, or different WLAN standards sharing one RX/TX chain. This is because of the merged BISC function which could work as a design centering as well as a design adaptive element.
In general, the reuse of function blocks within a design or from one system/technology platform to another must be improved. A higher degree of RF design automation is urgently needed since the design process of high-performance integrated transceiver solutions requires productivity acceleration. General design methodologies supporting RF analog design automation from system to component level are rare. New high level RF-suited design description languages like VHDL-AMS and the discussed AMS extension for SystemC enable the research on efficient approaches in this area. Today, design automation is entering the traditional RF full custom section. Modern C-level design languages allow to introduce parameterizability and process portability also to the RF-design. One example of such an approach can be found in [7], [8]. This new mixed-signal/RF IP design approach focuses on flexibility of design and process parameters in mixed-signal and RF designs within a customized conventional design framework. Special features are the flexible degree of automation and the compatibility to handcrafted designs.

The real benefits of such a proposed design platform with discussed aspects are cost and resource savings and increased flexibility and competitiveness.

3. Complete RFIC Front-to-Back Implementation starting from RF Architecture Selection with Verification at Mixed-Signal & System-Level for a WLAN application

(J. Hartung)

Besides advanced process technologies and circuit designs, a complete design flow is the key to enable the efficient design of modern wireless communication systems targeting up to 6 GHz carrier frequency, where our main focus is the design of an optimal RF-subsystem [10].
What is the IDEAL RFIC design flow?
Already in paragraph 2 several major demands are given. Typical requirements a complete design flow needs to support are:

- Enabling Top-Down & Bottom-Up design
- Fast architectural exploration for optimized RF spec.
- Complete application-specific testbenches
- Complete RFIC implementation environment
- Comprehensive consideration of parasitic effects
- Verification at system-level during each stage

A proposed RFIC design flow is given in Figure 3. The main stages during the flow will be described in more detail within the next sections. Three main parts are identified within the proposed solution:

1. RF Architecture Selection & Optimization
2. Verification & Exploration at System Level
3. RFIC Implementation

To select an appropriate architecture of a RF Transceiver for a specific wireless standard like W-CDMA, WLAN, Bluetooth and enabling comprehensive parameter studies and optimizations, a complete set of testbenches for the RF and the System-related measurements to perform all conformance tests is necessary.
The capability to verify, explore and optimize the entire analogue front-end of an RF IC in a Mixed-Signal & DSP design environment is one of the main challenges, but very crucial, in todays wireless standards.
Based on the selected RF architecture described at behavioral level, the major task is the complete implementation from transistor-level realization, layout and parasitic extraction.

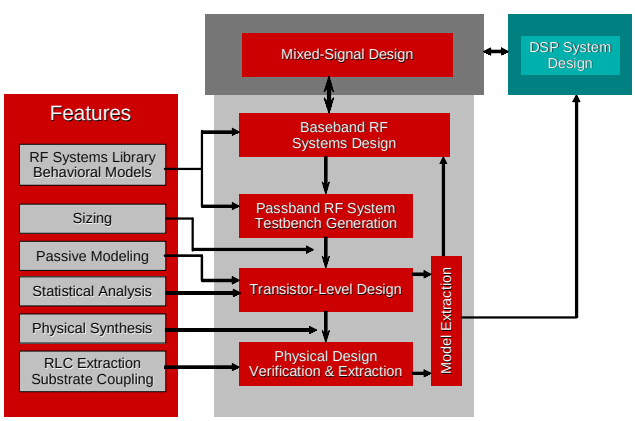

Figure 3: *Proposed RFIC Design Flow.*

To design, verify, explore and optimize an candidate RF architecture, a wide range of measurements need to be performed against the standard specification. In principle we can distinguish between RF and System measurements. Besides the measurements specified within the standard several other measurements needs to be performed to investigate the impact of the non-ideal effects on the modulated signal, like IQ imbalance, phase and bias error.
Standard design environments only provide limited support to perform these measurements within a single setup. New 'measurement-focused' approaches were necessary to enable a complete testbench built from stimuli's, analysis, post-processing and further application-specific parameters.
Beside the testbench setup another important point for enabling top-down design and architecture exploration at behavioral level are the models themselves. To perform a careful high-level architectural design before proceeding with the detailed block-level design, a complete set of RF behavioural building blocks need to be available. As long as typical RF measurements like Gain, Noise Figure, or Intermodulation need to be done under single and multi-tone excitation, where the available RF analysis could be used, these models are sufficient to analyse a given RF architecture. But when alternative RF architectures needs to be compared and also system-level measurements needs to be done with a digitally modulated signal applied, the performance of simulations at passband level are too slow.
Based on a complex lowpass signal representation [9], baseband models for RF function blocks that simulate what happens to the baseband representation of a signal as it passes through the block have been introduced.

In todays wireless standards it is very important to verify, explore and optimize the entire analogue front-end of an RF IC in a Mixed-Signal & DSP design environment.
Since the RF/Analog blocks are a subset of the mixed-signal circuitry they are directly available within the mixed-signal environment, therefore RF blocks could be easily extended with analog/mixed-signal/digital blocks (e.g. A/D converter) to do further studies.
Also for system designer several approaches exist to consider RF/analog non-ideal effects during their studies in a DSP design environment [1], [3]:

- Complex lowpass equivalent RF models in C
- Co-simulation techniques
- Extracted model techniques

A library implemented in C (also based on [9]) with similar blocks and parameters as the one within the IC flow implemented in a analog behavioral language allows you to realize the architecture in both "worlds" and just update the corresponding parameters.

Besides cycle-based, event-driven and analog circuit simulations, where the latter one offer several advanced RF simulation capabilities like envelope analysis [11], co-simulation techniques as a combination of the different choices offer new approaches to address the necessary trade-offs between accuracy and simulation speed and to combine different types of models and different levels of abstraction.
Further on, different extraction techniques are supported that creates an equivalent representative of the RF/analog circuit within the DSP design environment without sacrificing much simulation performance. This approach would still allow BER studies by taking into account non-ideal RF effects.

After the architecture optimization and its conversion into passband models and a corresponding testbench setup, the implementation of the transistor-level circuits and later on the physical realization starts. These passband testbench will be used during the complete implementation process and allows a combination of different levels of abstraction for each block and subsystem. We'll only highlight some of the implementation stages with its requisite features given in Figure 3 here.
The first stage is to realize transistor-level circuits for the blocks of the actual architecture at the passband representation. Based on the block specification, a topology and ranges for independent variables (size of devices, currents, voltages, etc.), multiple simulations are done during the sizing process, and later on the designer can analyze trade-offs between goals and sensitivities to design variables.
Due to higher frequencies and a higher integration, passive components (package, transmission line, spiral on-chip inductors, etc.) become more and more important for todays RFIC's. There are various ways to model/characterize these components (modeling tools based on formulas or look-up tables, electromagnetic field simulations, and/or measurements). The results are always RLC lumped-element models and/or simulated/measured S-parameter data that could be used within the circuit simulation.
Similar as passive component modeling, a comprehensive consideration of parasitic effects is absolutely mandatory. Especially substrate coupling and the inductive nature of interconnects are of vital importance in todays designs. As important as a fast and accurate extraction technology, is a seamless integration into the flow enabling parasitic re-simulations at different levels of abstraction.

The presentation will highlight the above mentioned aspects of the proposed design flow realized within the Cadence tool environment.

4. SiGe Design Kit with geometry scalable Compact Model integration introduces new degrees of flexibility to the RF design process (H.-J. Wassener, M. Schröter)

The accuracy of a simulation is dependent on three factors, the accuracy of the models, the error caused by the simulator algorithms, and the circuit set-up itself. Unreliable and erroneous results will thus be obtained if poor model parameters are being used or if the models do not accurately reflect physical effects that are important for the circuit behavior.
Atmel has to deal with all the topics mentioned above. As a foundry with internal and external design activities a fast feedback is required if problems arise with the supported design kits and differences between simulated and measured results. Continuous improvements have to be made in order to improve the overall design flow.

A long-term partnership with Prof. Schröter led to the introduction of the HICUM transistor model [12] in Atmel's RF design kits. This transistor model, geometry scalable and generated from TRADICA [18], is an improvement compared to the Gummel-Poon model. But designers are difficult to convince as there are some more factors influencing the simulation results.

Starting with the previous project HF-Frontends and continued with the project HGDAT a partnership with Cadence started, addressing the topic package modeling. Other topics were and are parasitic extraction and substrate coupling.

In order to cross-check the results of a parasitic extraction and to get broad band models of structures like packages, bond wires or integrated coils a 3D-EM simulator has to be used. CST is an associated partner within the project HGDAT and gives support for this task.

Back to the core devices namely the HICUM transistors, where several tasks were or are in the queue.
With its around 80 parameters, the HICUM transistor model is more complicated compared to the Gummel-Poon with its about 50 parameters. Overall, there are more than 200 NPN models, both simultaneously generated by TRADICA, included in the existing design kit. HICUM's capability to also simulate self-heating can create possible convergence problems during the simulation, depending on how the model is implemented in a circuit simulator. It turned out that SpectreRF is very robust regarding such problems.
One of the main applications for SiGe technologies are power amplifiers. All topics addressed later are especially important for PAs. Additionally reliable parasitic extraction is important as most of the transistor area is metal interconnection.
The first set of models being available in a bipolar design-kit describes typical values. As a first step towards statistical simulations corner models were introduced using the advanced knowledge base of TRADICA. Though using corners is not very common for bipolar RF technologies this was the only available possibility to enhance Atmel's design kits.
A reliable prediction of circuit yield is not possible when using corners. Though several tools are available for statistical simulations they depend on scalable models. So at the moment there is a gap between those tools and TRADICA which is presently employed to generate a large variety of fixed (discrete) models in a library. The methodology and program though are capable of generating continuously geometry scalable models and to allow geometry sweeps. To close this gap will be one of the major topics in the near future. Besides implementing statistical tools into the Cadence design flow the key will be TRADICA which has to generate a/o the statistical HICUM bipolar models.

The first part described more or less the view of creators or users of Atmels's SiGe design kits. The second part below will present the view of Prof. Schröter.

An advanced physics-based compact bipolar transistor model, HICUM (HIgh-CUrrent Model) [12], has been developed particularly for high-speed/high-frequency circuit applications, fabricated in modern Si/SiGe BiCMOS process technologies. Compared to the standard SPICE Gummel-Poon model, HICUM has been demonstrated to be significantly more accurate over both a wider operating and temperature range.

Transistor sizing is mandatory for circuit design and optimization (e.g. [13]), thus requiring a *geometry scalable* transistor model. Further benefits of such a model are the capability of, e.g., matching and statistical simulation. Geometry scaling means that *every* element in a model equivalent circuit has to be described as a function of device dimensions. While this is fairly simple for some elements it can become *very complicated* for other elements in a given process (s. below). For instance, geometry effects may not only depend on the device dimensions but also, for given dimensions, on bias and frequency. Also, sometimes certain vertical dimensions are allowed to be changed if requested by a customer, adding another degree of required model flexibility.

In addition to "general" geometry effects occurring at lower frequencies, there are a number of effects that become important at high frequencies but have not yet achieved the appropriate attention. The presently most

important geometry scaling issues from a (h.f.) circuit design point of view are:

- Collector-base breakdown caused by the lateral pinch-in effect [14];
- Thermal coupling caused by self-heating under adjacent emitter fingers or transistor cells [15];
- High-frequency noise from distributed injection and current flow under the emitter [16];
- Substrate coupling (intra and inter device).

In all cases, a spatially distributed representation of certain transistor regions is necessary for accurately predicting the circuit behavior. The associated distributed compact models can only be generated efficiently from a physics-based scalable model parameter set. Thus, it is easily imaginable, that a flexible model and parameter generation methodology for practically relevant device topologies, spanning from minimum size single-base to multi-finger transistors and including all important effects, requires a physics-based scalable approach with partially fairly complex equations, and significant coding effort .

As a possible solution for offering geometry scalable models, sometimes a *simplified* set of equations is implemented into the model subcircuit (e.g. [17]), using a simulator's specific scripting language. However, since this has a number of serious drawbacks, besides the large variety of bipolar transistor processes and device designs, a sophisticated set of scaling equations have been implemented into a stand-alone program called TRADICA [18].

Using the synergy between the modeling capabilities at CEDIC (TU Dresden), Atmel's foundry service with the feedback of its internal and external users (designers), and the EDA provider Cadence, TRADICA has been integrated into the Cadence Design Framework. The achievement of this new milestone in the field of bipolar transistor modeling, design kit support as well as tool and flow integration allows to use accurate geometry-scalable bipolar transistor models for modern Bipolar/BiCMOS processes. The approach is also more flexible compared to selecting models from a library with limited discrete transistor sizes. This facilitates a flexible path towards automated circuit design and optimization as well as parametric yield simulation. An important condition though for achieving this goal is the availability of a physics-based compact model, such as HICUM, which is supported by both TRADICA and SPECTRE-RF, within the Atmel's SiGe and SiGe-BiCMOS design kits.

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