

Hierarchical Simulation of Substrate Coupling in Mixed-Signal ICs Considering the Power Supply Network

Thomas Brandtner
Infineon Technologies
Development Center Graz, Austria
brandtner.external@infineon.com

Robert Weigel
University of Linz, Austria
weigel@mechatronik.uni-linz.ac.at

Abstract

This paper presents a novel substrate coupling simulation tool that is well suited to floorplanning of large mixed-signal IC designs. The IC layout may consist of several subcircuits, hence a hierarchical design flow, which is usually used for IC circuit design and layout, is supported. Coupling data modelling the substrate inside subcircuits are precalculated and subsequently used during floorplanning leading to shorter simulation time. In addition, the impedance model of the power grid is considered as well making it possible to provide estimation results of substrate coupling quickly after only one simulation step. The approach is verified by experimental results in 0.13 μm CMOS and 0.25 μm BiCMOS technologies.

1. Introduction

The ongoing trend to smaller feature sizes in IC technology offers the opportunity to implement RF-circuits operating at frequencies of up to several GHz in CMOS or BiCMOS ICs. Hence analogue and digital subcircuits may be integrated together in large mixed-signal designs. This enables digital interference to couple to sensitive analogue nodes through the substrate [1].

Traditional approaches to decrease this substrate coupling are, for instance, spatial separation, guard rings and less sensitive differential circuit designs [2]. Usually these measures are implemented using the circuit designer's experience, although a few substrate coupling simulation tools are available [3, 4]. Most of these tools simply perform a resistance extraction of a given flattened IC layout. This approach does not fit very well into the traditional hierarchical design flow, in which subcircuits are designed and layouted first. Subsequently, these subcircuits are placed during the process of floorplanning. Another important aspect of this design step is the power supply network. Since most of the substrate noise is coupled via low-ohmic substrate contacts

and connections of power supply nets [5], a properly designed power grid has a significant impact on the quality of substrate coupling countermeasures.

Therefore, a simple-to-use substrate coupling estimation tool for floorplanning would help the designer to create less sensitive mixed-signal ICs. In Section 2 a substrate model based on the boundary element method (BEM) [6] is presented which is well suited to large layouts that are usually considered during floorplanning. An optimal tool would provide coupling results immediately by itself without necessary further simulation steps. This may be achieved by cosimulation of the substrate and the impedance model of the power grid as proposed in Section 3. The data structure shown in Section 4 enables a hierarchical layout to be processed. In addition it supports fast recalculation if the placement of subcircuits (macros) is changed like being done in floorplanning. Simulation and measurement results are presented in Section 5 for two state-of-the-art technologies listed in Table 1.

Technology	ρ_{well} / depth of well	ρ_{bulk}
BiCMOS 0.25 μm	0.12 Ωcm / 1.25 μm	8 Ωcm
CMOS 0.13 μm	0.06 Ωcm / 1.2 μm	1.5 Ωcm

Table 1. Technologies with simplified substrate model data.

2. Modelling of the substrate

2.1. Boundary element description

Using a simplified point of view, the substrate of a CMOS or bipolar technology may be seen as a semi-indefinite halfspace of silicon with different layers of resistivity depending on the doping density, like epitaxial layers, wells and the bulk. In most cases time-variant magnetic fields and displacement currents can be neglected for frequencies below 10GHz leading to a simple electrostatic

description of the problem:

$$\nabla \left(\frac{1}{\rho(\vec{r})} \nabla \phi(\vec{r}) \right) = -J(\vec{r}) \quad (1)$$

where $\rho(\vec{r})$ denotes the resistivity of a certain point \vec{r} , ϕ is the potential and $J(\vec{r})$ describes the current density injected at point \vec{r} . The substrate is assumed to be free of space charge. In order to compute substrate coupling, two contacts i and j are considered first. For the sake of simplicity both are assumed to lie in the same substrate layer Ω . Only minor modifications have to be applied to the following equations in order to accommodate the more general scenario where the contacts are placed in different layers. The resistivity $\rho(\vec{r})$ is constant within Ω , therefore Equation 1 reduces to the Poisson equation. If a unit current is injected into contact j and if constant current density is assumed, the potential ϕ at a point \vec{r} inside Ω may be calculated as

$$\phi(\vec{r}) = \int_{\Omega} G(\vec{r}, \vec{r}_0) J(\vec{r}_0) d\vec{r}_0 = \frac{1}{A_j} \int_{\Gamma_j} G(\vec{r}, \vec{r}_0) d\vec{r}_0 \quad (2)$$

with Γ_j equals to the surface of contact j with an area A_j . $G(\vec{r}, \vec{r}_0)$ is the modified Green's function which accommodates the special problem of a semi-indefinite layered half-space. It satisfies

$$\Delta G(\vec{r}, \vec{r}_0) = -\rho \delta(\vec{r} - \vec{r}_0) \quad (3)$$

within volume Ω . G simply expresses the potential at a certain point \vec{r} , if a unit current is sourced into an indefinitely small point \vec{r}_0 . It also holds the homogeneous Neumann condition at the surface of the substrate. G and the normal component of current density should be continuous at all boundaries between two substrate layers. Only contacts need to be considered in Equation 2 which is a main advantage of any boundary element description. On the other hand, the whole substrate has to be discretised when using finite element methods [2] leading to a large number of variables that may not be feasible in large mixed-signal designs.

2.2. Green's function for layered media

Due to radial invariance of the semi-indefinite layered halfspace, separation of variables in cylindrical coordinates may be used to simplify Equation 3 to

$$G(r, z, z_0) = \frac{1}{2\pi} \int_0^{\infty} Z(k, z, z_0) J_0(kr) dk \quad (4)$$

where $J_0()$ is the Bessel function of the first kind of order 0. The integration variable k acts like a spatial frequency since the depth function $Z(k, z, z_0)$ has to satisfy the propagation equation with the well known solution

$$Z(k, z, z_0) = A_i(k, z_0) e^{kz} + B_i(k, z_0) e^{-kz} \quad (5)$$

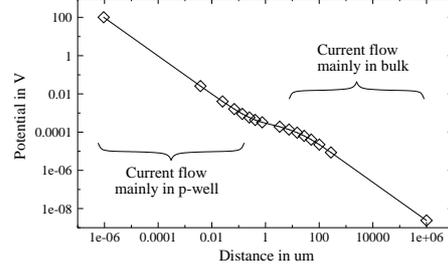


Figure 1. Green's function of CMOS process

This result is similar to the solution of a transmission line, therefore A_i and B_i may be interpreted as amplitudes of propagating waves [7]. The depth function Z has to meet several boundary conditions that can be used to determine A_i and B_i

- Homogeneous Neumann boundary at $z = 0$
- $Z(k, z, z_0)$ and $\frac{1}{\rho} \frac{\partial Z(k, z, z_0)}{\partial z}$ continuous at layer interfaces
- $\lim_{z \rightarrow \infty} Z(k, z, z_0) = 0$
- At injection point z_0 :
 $\frac{\partial Z(k, z, z_0)}{\partial z} \Big|_{z \rightarrow z_0+} - \frac{\partial Z(k, z, z_0)}{\partial z} \Big|_{z \rightarrow z_0-} = -\rho k$

Now Equation 4 may be used to calculate the space domain Green's function G . It is a one-dimensional Hankel transform, which is computationally expensive. Fortunately the depth function Z is smooth in k -domain making it possible to exploit a Fast Hankel Transform algorithm [8]. After a change of the integration variable $k' = kr$ and a transform into log-domain $r = e^x$, $k' = e^y$, Equation 4 may be rewritten as

$$G(r, z, z_0) = \frac{1}{2\pi r} \int_0^{\infty} Z(e^{y-x}, z, z_0) J_0(e^y) e^y dy \quad (6)$$

which is a convolution-type integral of two functions $f_1(x-y)$ and $f_2(y)$. It may be discretised and evaluated by a digital filter with an appropriate set of weights.

Figure 1 shows the Green's function of the 0.13 μm CMOS process mentioned in Table 1. Although a retrograded p-well is implanted down to a depth of about 1.5 μm , it is sufficient to model it as a single additional layer. Usually the doping profile of the p-well is known. For the calculation of the average resistivity one has to take into account that the carrier mobility depends on doping concentration due to additional scattering at ionised impurities [9]. Simulations show that using several layers to describe the changing doping concentration leads to the same result.

It can be seen in Figure 1 that the electric field near the injection point has a simple $1/r$ -relationship which is similar to a field of a single layer halfspace with $\rho = \rho_{\text{well}}$. If the distance gets bigger than the depth of the low ohmic p-well, more and more of the injected current flows into the high ohmic bulk leading to a bend in the Green's function.

If distance is increased further, $1/r$ -relationship returns with $\rho = \rho_{bulk}$ since the major part of the current now flows in the bulk only. This shows that guard rings are quite effective in this technology since the resistivity between adjacent substrate contacts is low, whereas the coupling between distant ones is small due to the less doped bulk.

The Green's function is calculated once. It is possible to compress this data in log-domain since the $1/r$ -relationship transforms to a simple linear one. Hence only a few points have to be stored in the so-called technology file. This pre-calculation of G increases the speed of many subsequent computations.

2.3. Resistance calculation

The next step in substrate modelling is the assembly of an impedance matrix Z which elements are $Z_{ij} = \phi_i/I_j$ where ϕ_i is the potential of contact i due to a current I_j injected into contact j . Equation 2 only provides the potential at a certain point. The potential across a contact is constant. This condition does not fit into the assumption of a constant current density. Hence each substrate contact has to be divided into smaller rectangles in order to keep the error small. Galerkin's method may be applied in order to estimate the voltage ϕ_i leading to

$$Z_{ij} = Z(R_i, R_j) = \frac{1}{A_i A_j} \int_{\Gamma_i} \int_{\Gamma_j} G(\vec{r}_i, \vec{r}_j) d\vec{r}_j d\vec{r}_i \quad (7)$$

Contacts i and j are assumed to be rectangles R_i and R_j . Γ_i is the surface of R_i with area A_i and Γ_j denotes R_j with area A_j .

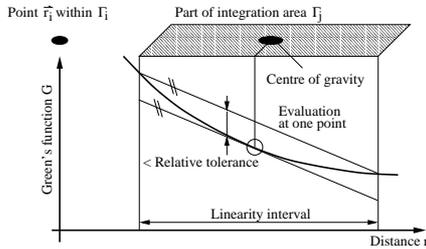


Figure 2. Linear approximation for integration

Two two-dimensional integrations of G have to be performed for the calculation of Z_{ij} . Hence a linear approximation of G within a reasonable interval is used for a fast evaluation of the inner integral (Figure 2). An appropriate maximum value for the linearity interval with respect to distance r is determined so that the approximation error is limited to a given relative tolerance. If G were linear, an evaluation of G at the centre of gravity would cause no integration error at all. Assuming $1/r$ -relationship of G , which is usually the case, a relative tolerance of 0.1 leads

to an integration error of 0.017. This value turned out to be sufficient for substrate coupling estimation with reasonable accuracy, hence it was used for all simulations in Section 5. The value of this linearity interval with respect to distance is also precalculated and stored in the technology file mentioned above.

These considerations lead to a recursive algorithm for computing the integral of Equation 7. Assume that R_i is smaller than R_j and let C_i and C_j be the centre of gravity of R_i and R_j , respectively. If R_i and R_j together are smaller than the precalculated linearity interval for the distance between C_i and C_j , Z_{ij} is estimated to be $G(C_i, C_j)$. Otherwise, R_j is divided into two parts R_{j1} and R_{j2} . The problem $Z(R_i, R_j)$ itself is recursively computed with $Z(R_i, R_{j1}) + Z(R_i, R_{j2})$.

The substrate is passive and reciprocal, therefore the impedance matrix Z is symmetric and positive definite. Hence its inverse $Y = Z^{-1}$ may be calculated by using a conjugate gradient (CG) algorithm [10]. Although matrix Z is dense, it is still the best choice to get a fast result since the coupling coefficients Z_{ij} decrease quickly for distant contacts. Starting with 500 rectangles it takes about 25 iterations to get a result with a residual error of 0.001.

3. Cosimulation of substrate coupling and power supply network

Substrate coupling simulation programs usually compute a circuit model describing the coupling between certain contacts. Such a model can be extracted from the elements of the admittance matrix Y . The CG algorithm calculates the result of a linear equation system, hence it must be restarted several times to get the whole inverse Y .

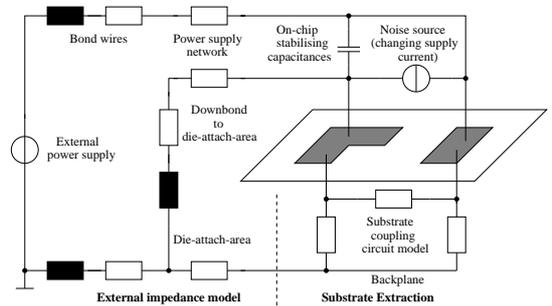


Figure 3. Substrate and external impedance model

Unfortunately, this substrate circuit model is not sufficient to estimate substrate coupling. The resistivity between substrate contacts and power or ground nodes also plays an important role as shown in Section 5. Hence an impedance model has to be provided defining the 'external world' like

the power supply network (Figure 3). In our approach the admittance matrix Y is never computed. The impedance model is used directly in our program to calculate the coupling between certain nets. Hence only one linear equation system has to be processed. This results in a significantly improved computation time.

An hierarchical SPICE netlist with subcircuits is used to define the impedance model. This netlist is read and the Y matrix is set up exploiting the nodal voltage approach. Rearrangement of nodes gives

$$\begin{pmatrix} I_{CS} \\ I_{NS} \end{pmatrix} - \begin{pmatrix} I_C \\ 0 \end{pmatrix} = \begin{pmatrix} Y_{CC} & Y_{CN} \\ Y_{CN}^T & Y_{NN} \end{pmatrix} \begin{pmatrix} V_C \\ V_N \end{pmatrix} \quad (8)$$

Nodes C are substrate ports, nodes N are internal ports. I_{CS} and I_{NS} are currents sourced to specific nodes inside the external impedance model. I_C is current flowing into the substrate. V_N and V_C denote the nodal voltages. Simplifying yields

$$V_C = Z_{ext}I_C + V_{ext} \quad (9)$$

$$Z_{ext} = (Y_{CN}Y_{NN}^{-1}Y_{CN}^T - Y_{CC})^{-1} \quad (10)$$

$$V_{ext} = Z_{ext}(Y_{CN}Y_{NN}^{-1}I_{NS} - I_{CS}) \quad (11)$$

Since the impedance matrix Z satisfies $V_C = ZI_C$, a cosimulation of substrate and impedance model may be carried out:

$$(Z - Z_{ext})I_C = V_{ext} \quad (12)$$

Again a CG algorithm is used to solve this modified linear equation system.

4. Data structures and algorithms

Our novel substrate simulation tool supports a hierarchical design strategy. Hence the internal data structure has to model the layout of an IC and its substrate contacts in a hierarchical way. A binary tree is well suited to such a problem. In addition the impedance matrix Z has to be stored in this tree in a way that an effective matrix multiplication can be performed. This led to the development of a 'Binary Coupling Tree (BCT)' shown in Figure 4.

The macro object represents the root of the BCT, cell objects implement the internal nodes. On the other hand a macro object may act as an internal node as well supporting macros being placed in macros and, therefore, a hierarchical design strategy. Rectangle objects are leaf nodes containing the detailed layout information divided in space. A cell object combines all substrate ports of its child nodes to one big simplified substrate contact.

The elements of the impedance matrix Z are stored in a single linked list. Each list element consists of a pointer to two nodes of the BCT and the dedicated coupling data.

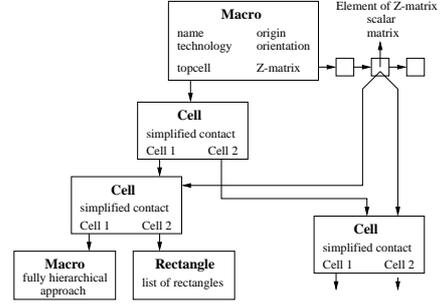


Figure 4. Binary Coupling Tree

This data may be a matrix containing all coupling coefficients Z_{ij} between all rectangles of two rectangle objects, or it models the coupling between the simplified contacts of two cell objects. The latter may happen if the two cells and its substrate contacts are placed far away from each other. The linearity interval of the Green's function is used to determine whether this simplification is justified.

A macro and its BCT can be precalculated and stored in a macro database. These precalculated macros may be load quickly during floorplanning. A calculation of the additional coupling coefficients between the macros is still necessary. However, this can be performed easily since macros are usually located far enough from each other being able to exploit the coupling simplifications mentioned above. If one macro is rotated or moved, only certain elements of Z need to be reevaluated.

Together with the cosimulation presented in the previous section these advantages will make our tool highly suitable for the estimation of substrate coupling while floorplanning an IC.

5. Simulation and measurement results

A testchip in each technology of Table 1 has been designed and manufactured. Both ICs contain various different guard ring structures like guard rings with different distance to the noise injection point or guard rings with different width and spacing to the dedicated measurement contact. Simple resistive substrate contacts with a size of $6 \times 6 \mu m^2$ act as noise injection points. In this paper only results of our DC test structures are presented since the present version of our simulation software does not consider any capacitive coupling between wells. This very important feature is currently under development.

Figure 5 illustrates the results of the CMOS testchip for guard rings placed with different distance to the injection point. All measurements were carried out with a frequency of 0Hz. An excellent matching of measurement and simulation data may be observed. However, one would expect a smooth increase of attenuation over distance. Actual variations are originated in different resistances R_{gr} between

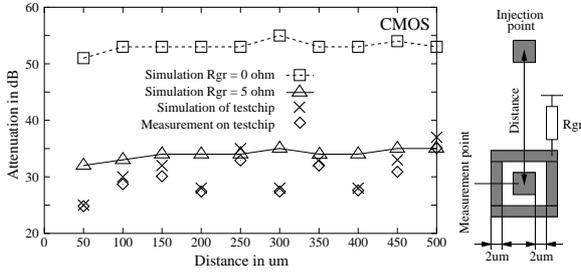


Figure 5. Guard rings at different distance

guard rings and the ground node. On the CMOS testchip R_{gr} ranges from about 5Ω to 15Ω due to difference in metal line length. R_{gr} is extracted from layout and its influence is directly simulated by the cosimulation procedure of Section 3. Simulation results for constant R_{gr} are provided in Figure 5 as well. A slight decrease in coupling over distance may be seen. Hence R_{gr} has a big impact on substrate noise decoupling as shown in Figure 6.

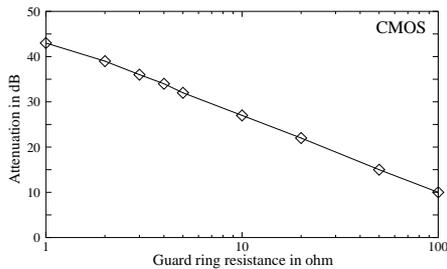


Figure 6. Influence of guard ring resistance to ground (Distance $50\mu\text{m}$)

The influence of spacing between guard rings and the measurement points, which they should stabilise, is presented in Figure 7. Again simulation and measurement provide almost equal results. Near guard rings offer only a small improvement due to the huge difference in resistivity of the p-well and the bulk beneath. A big R_{gr} may worsen the decoupling significantly. Hence the design of the internal power supply network is critical to the function of all guard rings that are usually connected to power or ground nodes. Results of the BiCMOS testchip are almost equal to its CMOS counterpart except a shift of 5 to 10dB in attenuation due to higher resistance of p-wells and bulk.

6. Conclusion

The traditional approach of substrate coupling estimation with resistance extraction in a flattened layout and subsequent network simulation is not feasible for large mixed-signal designs. In this paper a hierarchical substrate simulation tool has been presented. It offers the opportunity of

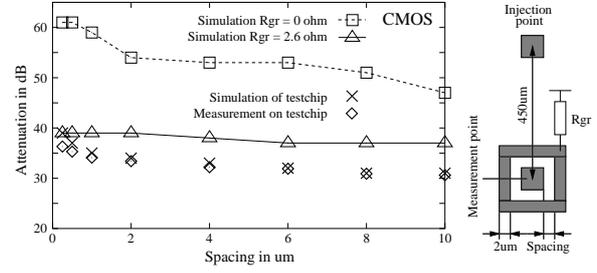


Figure 7. Guard rings with different spacing

substrate coupling estimation during the process of floor-planning. Fast recalculation is performed after typical operations like moving or rotating a subcircuit (macro) in the floorplan. The cosimulation of substrate coupling and the external impedance model of the power grid decreases both computation time and the necessary number of steps until a useful result for the designer is provided. The application to larger mixed-signal designs and the incorporation of wells will be part of investigations in the near future.

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