# Giant Spin Hall Effect (GSHE) Logic Design for Low Power Application

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***Abstract*—Conventional CMOS transistors will reach its power wall, a huge leakage power consumption limits the performance growth when technology scales down, especially beyond 45nm technology nodes. Spin based devices are one of the alternative computing technologies that aims to replace the current MOS based circuits by taking the advantage of their attractive characteristics, including non-volatility, high integration density and small cell area. The development of technologies such as spin-transfer torque random access memory (STT-RAM) and spin torque majority gate logic has become a story of great success. However, most of these technologies faces problems like, small operation margin, poor fan-out ability, etc. As the latest spin technology, Giant Spin Hall Effect (GSHE) Magnetic Tunneling Junction (MTJ) demonstrates a much better operation speed, switching probability and resistance margin. By leveraging the benefit of greater power efficiency and area density, GSHE MTJ elements become a suitable candidate for spintronic logic gates. Compare with traditional MOS transistors based logic gates , GSHE MTJ based logic can operate as a non-volatile memory and requires a much smaller number of elements to perform same logical operations (i.e., 'AND', 'OR', 'NAND' or 'NOR' gate.). And compare with other spin based logics, GSHE MTJ based logic also provides an better performance, excellent CMOS process compatibility and great fan-out ability.**

## I. Introduction

Conventional CMOS technology based design has been confronted by many technology challenges, such as localized variability [1], integration issues [2] and power dissipation issues [3]. As one of the solution to avoid an increase in dynamic power consumption, multicore processors have become a major application in modern microprocessors. However, with the technology continuously scaling down, multicore architectures reduced dynamic power consumption with an exponentially rises of leakage power. As CMOS scales beyond 45nm technology nodes, leakage power becomes one of the bottleneck that limited the performance of microprocessor. With billions of transistors integrated on a single process, high transistor leakage current leads to an tremendous increasing of the power consumption, which increases overall system cost, and at the same time, significantly degrades the reliability. The increases in transistor density cannot introduced linear savings in power consumption.

Researchers from both industry and academy are now looking for emerging technologies as the alternatives to traditional CMOS technologies. Following such a research, new developments of power efficient, scalable microprocessors based on emerging resistive memory technologies has been presented. As one example, spin-torque transfer RAM (STT-RAM) which leverages the magnetic device of magnetic tunneling junction (MTJ) shows a great potential in on-chip cache and memory for its zero standby power, high integration density, fast access time, and excellent CMOS compatiblity [4]. Such a technology has been developed since early 2000s [5], and commercialized by Everspin in 2013.

Except the application of on-chip storage, researchers also found out that there is also a possible to further implement combination logic using scalable, low leakage resistant memory device arrays constructed from non-volatile memory such as STT-RAM and spin torque majority gate. In conventional CMOS based structure, combination logic circuits cost even more power than memories. But with the implementation of non-volatile devices, this part of power consumption can also be saved. Even more, with such a technology, the design area can largely reduced without sacrifice much operation speed, and performance. It is expected that in the near future, a whole processor can be fully construct by these non-volatile device. With such a MOS free structure, the leakage power can be highly reduced even with continuously scaling down technologies.

Various researches has been studied under such a purpose. These purposed structure leverages the device non-volatility to reduce the static power consumption, however, most of them also experienced problems of their own. Nikonov et al. presented a spin torque majority gate, that a four terminal device is designed that the output is decided by the majority data among the three inputs. Since the output nodes number is always less then those of input nodes, such a structure could be not easy to control if it is extended to a more complicated structure. Guo, et al. proposed a STT-RAM Look Up Table (LUT) structures using a set of STT-RAM based LUTs to perform the logic function [6]. However, same concepts as FPGA, the number of transistors used in these LUTs could be even larger than it of a conventional CMOS based combination logic. In such a situation, the leakage power may even increase. And there are many other designs that build flip-flops based on STT-RAMs [7], [8]. While with a relatively high switching threshold of MTJ, process variation and intrinsic thermal randomness impacts largely reduce the reliability of these structures.

As the latest spin technology, Giant Spin Hall Effect (GSHE) MTJ demonstrates a much better operation speed,

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switching probability and resistance margin. By leveraging the benefit of greater power efficiency and area density, GSHE MTJ elements become a suitable candidate for spintronic logic gates. Thus, in this paper, we will provide a novel logic structure that leveraging GSHE MTJ devices. The simulation results shows that, compare with conventional CMOS based logic gates, our structure may reduce leakage and total power at 22nm technologies nodes by $3.1\times$ and $5\times$, respectively, while maintaining an almost same throughput with its non-volatility property.

The rest of paper is organized as follow: Section II presents the basics of GSHE MTJ; Section III introduces the basics concept of our proposed logic structure; Section IV gave a detail of the disadvantage of this structure and how the structure is improved; Section V shows a case study of two inputs ripple-carry full adder and Section VI concludes our work.

## II. GSHE-MTJ Basics

Fig. 1(a) illustrates a 3-D view of one aspect of Giant Spin Hall Effect (GSHE) MTJ device. As the cross-sectional view shows, GSHE MTJ constructs by a stack of various layers. More specifically it contains a free layer, an dielectric oxide layer, and a reference layer which are the three layers that a conventional MTJ is consisted of, a GSHE electrode strip, and a antiferromagnetic layer. The data store in the device is based on the different directions of magnetization in the free layer and the reference layer. When the magnetization orientation of the free layer is parallel to that of the reference layer. The MTJ resistance is in low resistance state ($R_L$) and representing logic '1'. On the contrary, a high resistance state ($R_H$) or logic '0' is presented by anti-parallel directions of the two ferromagnetic layers. The GSHE electrode strip is coupled to the free layer. It is formed from GSHE materials such as $\beta$-Tantalum, $\beta$-Titanium, Rubidium or Platinum [9]. When a charge current flow through the strip, it will produce a GSHE which converts the input charge current into a spin current. The spin current conversion can be described by:

$$J_c = \theta_{SH}(\sigma \times J_e) \tag{1}$$

where $\hbar J_c/2e$ is the spin current density, $J_e$ is the charge current density, $\sigma$ is the spin polarization unit vector, and $|\theta_{SH}| = |J_c/J_e|$ is the material-dependent spin hall angle.

The GSHE spin current will exert a spin torque on the free layer and change the free layer magnetization between parallel and anti-parallel states. When the applying programming current on the strip (from terminal A to B as shown in Fig. 1(a)) is larger than the switching threshold, the device will be written to '0', and it will switch to '1' if a current larger than the threshold is applied on the opposite direction. If the current from either direction is smaller than the threshold current, the device will not be written and remain its current data state. And the antiferromagnetic layer on the top is used to ensure that the magnetic orientation of the reference layer is always fixed.

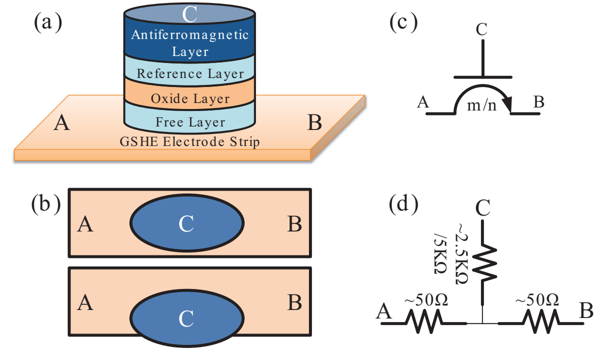


Fig. 1. GSHE MTJ structure (a) 3-D view, (b) Top-down view, (c) Device symbol, (d) Equivalent circuit.

Without considering thermal fluctuation, the critical current density $J_{c0}$ for GSHE-MTJ switching can be written approximately as: [10]

$$J_{c0} \approx \frac{2e}{\hbar}\mu_0 M_s t \alpha_0 (H_c + \frac{M_{eff}}{2})/\theta_{SH} \tag{2}$$

Where $M_s$, $M_{eff}$ is the saturated magnetization and effective demagnetization field, $\alpha_0$ is damping constant when input current is 0, $H_c$ is the coercive field of free layer, and $t$ is environment temperature. If the material is fixed, the threshold current density can be calculated by Eq. 2. Compare with conventional MTJ used in STT-RAM, the current density threshold of GSHE MTJ is times smaller. A lower energy barrier and smaller threshold makes GSHE MTJ a better candidate for combination logic design.

The relationship between switching current density and charging current density is fixed, however, the charging current can be adjusted by different connected area between free layer and GSHE strip as shown in fig. 1(b). Thus, the threshold current can also be changed by placing MTJ with a various position on top of the GSHE strip.

Fig. 1(c) and (d) represents GSHE MTJ device symbol and equivalent circuit. a, b, and c are the three terminal of GSHE MTJ. The arrow direction denotes the direction of writing '0'$\rightarrow$'1'. Since the device is driven by current, m and n here, shows the connect input current nodes and relative threshold, respectively. Fig. 1(d) also shows that the resistance of strip is much smaller than the MTJ resistance. Since the writing path only go through the metal strip it largely reduce the resistance on the writing path. Meanwhile, it is possible to increase the resistance of MTJ, and improve the operation margin.

## III. GSHE Spin Logic Structure

### A. Basic Logic Functions

Since the switching threshold of GSHE MTJ can be changed by manufacturing without using other material, it is possible to build device with various threshold. This property makes such a device possible to achieve basic logic functions, (such as 'AND', 'OR', 'NAND', and 'NOR'). Fig. 2 illustrates the circuit design of basic two inputs logic gates and corresponding truth table. The logical operation performed by each of these GSHE MTJ elements is determined by appropriate connecting direction of input nodes A and B, as well as

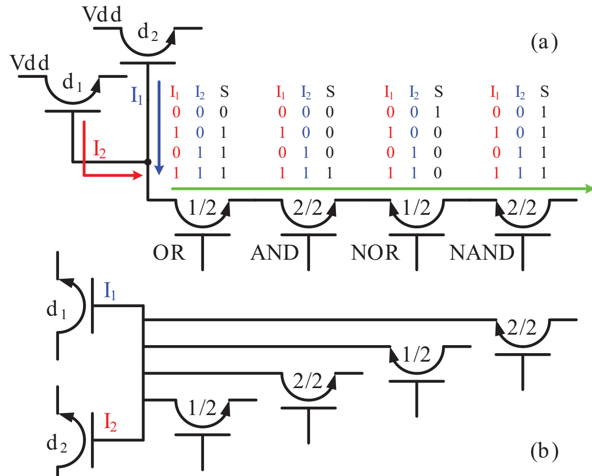


Fig. 2. Examples of Basic Logic Functions. (a) Serial Connection, (b) Parallel Connection.

selecting of input nodes (n) and switching threshold (m). The input currents of each device are determined by the output resistance states of upper level devices ($d_1$ and $d_2$). With different resistance states (either $R_H$ or $R_L$) of two input devices, the current $I_1+I_2$ will present approximately in three region: $R_H, R_H(0,0)$, $R_H, R_L(0,1)$, and $R_L, R_L(1,1)$ under the same supply voltage. Devices will be switched once the current is larger than the threshold. If the threshold is near $R_H, R_L$, the device will perform as an 'OR' gate. Otherwise, if the threshold is around $R_L, R_L$, the device will then perform as an 'AND' gate. 'NAND' and 'NOR' gates can be achieved by an opposite connection of 'AND' and 'OR' device. Truth tables of these four types of logic gates are shown in fig. 2 (a).

For more detail, although the resistance of GSHE strip is much smaller than that of MTJ, it still needs to be considered when calculating the required threshold. We assume that MTJ resistance is $R_L = \frac{1}{2}R_H = R$. Then the relationship between two resistance states and writing current $I_{XY} = I_1 + I_2$ can be as follow:

$$
\begin{aligned}
I_{00} &= \frac{4V}{4R+(4N+1)R_S} \\
I_{01} = I_{10} &= \frac{V(3R+R_S)}{(2R+\frac{R_S}{2})(R+\frac{R_S}{2})+NR_S(3R+R_S)} \\
I_{11} &= \frac{2V}{R+(2N+1)R_S}
\end{aligned}
\tag{3}
$$

Where $R_S$ is the equivalent resistance of GSHE strip, and N is the number of elements that connected on the output path. As aforementioned, the switching threshold for 'AND' gate and 'OR' gate should be placed between $I_{11}$, $I_{10}$, and $I_{10}$, $I_{00}$, respectively. In order to tolerate more process variation effect, the margin between the charging and threshold current should be both maximized. Therefore, the switching current threshold of 'AND' gate ($I_{AND}$) and 'OR' gate ($I_{OR}$), could be:

$$
\begin{aligned}
I_{OR} &= \frac{V[10R^2+(12N+6.5)RR_S+(4N+1)R_S^2]}{[4R+(4N+1)R_S][(2R+\frac{R_S}{2})(R+\frac{R_S}{2})+NR_S(3R+R_S)]} \\
I_{AND} &= \frac{V[3.5R^2+(3N+6.5)RR_S+(N+0.75)R_S^2]}{[R+(2N+1)R_S][(2R+\frac{R_S}{2})(R+\frac{R_S}{2})+NR_S(3R+R_S)]}
\end{aligned}
\tag{4}
$$

We assume that $R = 2.5k\Omega$, $R_S = 100\Omega$, and the fan-out number N is 4, thus, the switching threshold ratio between $I_{AND}$ and $I_{OR}$ is approximately: $\frac{I_{OR}}{I_{AND}} \approx 0.7745$. The ratio could be changed with a even large number of N, since the threshold is fixed after fabrication, it can not be changed based on different fan-out, thus, the number of fan-out is limited. However, the fan-out number is still much larger than the input elements number, with proper design, it is possible to achieve any combination logic based on the basic logic gates.

To further reduce the affect from fan-out device, a parallel structure is designed as shown in fig. 2 (b). As load resistance of writing devices is reduced by parallel structure, the current is mainly determined by MTJ resistance. However, such a structure will distribute charging current through each strip, the current will largely reduced depends on how many output elements there is. Thus to reduce the dynamic power consumption, the serial structure will mostly be adopted, the parallel structure will be a better candidate when a large enough power supply is provided.

### B. GSHE Logic Operation Scheme

In GSHE logic device, performing a logic function determined by what resistance state the input device stored, it requires that these input devices should be stable with its data. The devices in a path cannot be all written at the same time. To write one device, the data stored in both its upper and under level devices cannot be changed at the same time. It makes that, in a complex circuit structure, the devices cannot be written all together. Another issue is that each device could be both input device and writing target element, the supply voltage should be able to apply on each of these device in the circuit. To achieve such a writing scheme, a multi-step writing should be applied in GSHE logic device writing. On the other hand, since writing of these device depends on the direction of charging current, once a device has been written, it cannot perform the same function again. Once the device has been switching, it cannot be switched back under the same direction writing. Thus, a preset step is required before each operation, an opposite current is applied to ensure that every device is at the initial state before it can perform a correct function.

Therefore, an unique multi-stage structure is designed to

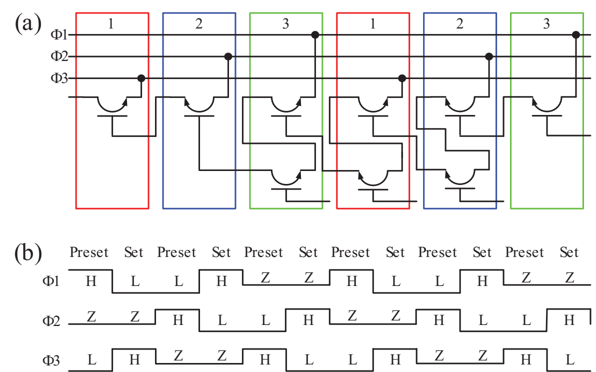


Fig. 3. (a) Circuit of Three-stage Operation Scheme, (b) Control Signal Diagram.

achieve GSHE logic functions. In the scheme, input devices and target devices are assigned into different stage to avoid writing conflict. As an example, a three-step structure is shown in fig. 3 (a). Three control lines (Φ1, Φ2, and Φ3) are applied to separate these three stages. Since GSHE device has three terminals, for each device, its input is connected with one or two outputs of upper stage devices depends on its corresponding function, the output is connected with inputs of several under stage devices, and its third terminal is connected with the control line of its own stage. Writing/control signal of such a circuit is shown as fig. 3 (b). For each writing stage, there are two steps: preset step and set step. In the preset step of stage $M$, control line $\Phi(M-1)$ is connected to supply power $2V_{dd}$, control line $\Phi M$ is grounded, and the rest lines are all floated. Therefore, the charging current will only apply through GSHE strip of the target devices and the power supply can be large enough to write all these devices back to their initial states. On the other hand, switching control line $\Phi M$ to $V_{dd}$ and grounding line $\Phi(M-1)$ will perform a writing in set step. During the writing step, the floating lines can isolate none used devices from input and target device, so that the performed functions will not be disturbed.

The proposed control line writing scheme is a sequenced writing. Under such a scheme, the timing performance of all these devices are all controlled by the control lines, no extra clocks are necessary in the design. At the same time, by leveraging the non-volatility property of GSHE MTJ, data can stored in these device, thus, the requirement of latches or flip-flops can also be reduced. Besides that, since the writing is divided to several steps, the same output data can be readout from the output in each step, when the logic devices haven't catch a new input. The accuracy of a circuit can be verified by comparing these output data, which largely increase the reliability of GSHE combination logic.

## IV. Diode-GSHE Structure

### A. Sneak Path Issues

Same as many other resistive device, sneak path could always be an issue that high-resistance cells being "short-circuited" by paths of devices in low-resistance state. Fig. 4 shows an example of a real case of current sneaks in GSHE logic. The current flows through some sneak paths (blue line) beside the desired one (red line). These paths contains uncontrolled parallel resistance, with various data stores in device A to H, the charging current of the desired path will be heavily impacted. The added resistance of sneak paths significantly narrows the operation current margin. To reduced the affects of sneak paths, a much larger number of writing stages is required to operation GSHE logic. As a matter of fact, to avoid overwriting these undesired devices, at least 7 stages are required in the writing scheme. More stages will leads to more non-used stages during each operation stage, and its throughput will also be largely reduced with these unoccupied stages.

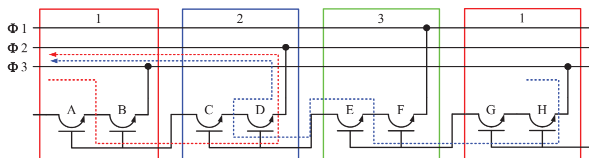


Fig. 4. An example of a real case where current sneaks through undesired paths.

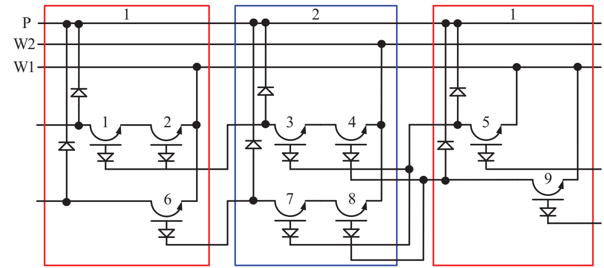


Fig. 5. Proposed Diode-GSHE Structure.

### B. Proposed Diode-GSHE Structure

The sneak path issue can be eliminated by the proposed diode-GSHE structure. By using a non-linear device as a function of diode [11], [12], the current flow would be limited only within desired direction. Fig. 5 shows our proposed design. With applying non-linear diode on the connection of each blocks, the current can only go through the direction from input device to target device, and undesired sneak current will be largely reduced. Since the writing stage can be blocked by the non-linear devices, no more then two stages are necessary in the desire. With a diode-GSHE structure, there are only two operation steps: when the first stage is used as inputs, the second stage will be programmed; on contrary, writing the first stage is based on the data stored in the second stage. During the whole process, devices in the circuit are always occupied. With the same logic structure, the throughput of Diode-GSHE structure can be further improved.

Since only two stages are used, two control lines are required. However, in Diode-GSHE structure, there are an extra control line which is used for preset step. Thus, in Diode-GSHE, the preset will go through a preset line, instead of going back through the writing path. Apparently, there are two mainly advantages as the preset control line is designed. First, since the preset path only go through a single GSHE strip, the supply voltage for preset can be very small to provide a large enough switching current. With a much lower preset voltage, power consumption of the whole system can also be reduced. More important, if the preset current doesn't go through the input device, the input device will not be disturbed by preset control. The preset line design, will also improve the reliability

TABLE I
Control Signal of Diode-GSHE Structure

| Control Lines | P | $W_1$ | $W_2$ |
|---|---|---|---|
| Preset1 | 0 | $V_{low}$ | Z |
| Set1 | Z | 0 | $V_{high}$ |
| Preset2 | 0 | Z | $V_{low}$ |
| Set2 | Z | $V_{high}$ | 0 |

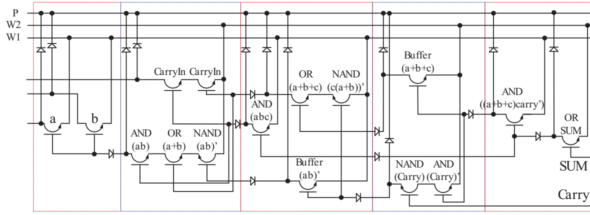

Fig. 6. Example of Diode-GSHE Based Full Adder.

of the whole system. To achieve a two step programming, the input signal will be designed as shown in TABLE I.

By leveraging non-linear devices, and extra preset line, such a scheme is able to limit the direction of each current flow, so that the sneak path in both preset stage and programming stage will be reduced. Meanwhile, both power consumption and programming throughput can be improved by such a structure.

## V. Case Study

### A. Full Adder Design

As an example, a full adder has been build based on Diode-GSHE logic structure. Fig 6 shows the structure of 1 bit full adder. Although it is possible to have any number of fan-outs, the design will be complicated if too many fan-outs are connected from one device. Since every GSHE strip comes with its intrinsic resistance, it is not easy to control the current flow compare with relatively precise switching threshold of each device. Thus, in Diode-GSHE design, the fan-out is limited in 1∼3. Another rule is that input devices can't be shared with multiple devices, they also can not be connect to a same output if they are in different stages. To follow this rule, a buffer has been introduced in the design, a buffer is an one input node GSHE device, that will pass the upper stage data to the under stages. Although it will cost some power and more design area, it makes a combination logic easier to design.

Leveraging the property of non-volatility and its self-sequential control, an N-bits adder can be achieve by one single-bit full adder that has a carry-out connected with carry-in (as shown in fig. 7). Since the higher bit shall always wait the carry-out signal from lower bit, such a structure doesn't need to sacrifice the operation latency. It is possible to design an N-bit adder by only one single-bit full adder without any extra overheads. Thus, the adder can largely reduce the design area and power consumption while maintain almost same throughput.

On the other hand, as shown in fig. 6, there are three circles from lower bit carry-in input to the outputs, thus, for each bits operation, there will be three same results provided to the output, these two more results that calculated by the same progress, can be used to verify the correction of first result. This scheme can largely increase the GSHE logic reliability which is one of the biggest issue in resistive devices.

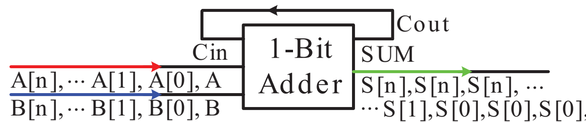


Fig. 7. N-bit Adder Structure basd on 1-bit Adder.

### B. Experimental Results

A verilog-A GSHE MTJ model was created for our proposed design. The single bit full adder has been built with such a verilog-A model. With the same function, CMOS based full adder has also been simulated with PTM 22nm, 32nm, and 45nm technology model [13]. All simulations were conducted under Cadence Spectre Analog environment.

The summary of GSHE MTJ performance has been provide in TABLE II [10]:

TABLE II
SUMMARY OF GSHE MTJ PARAMETERS

| Parameter | Values |
|---|---|
| Critical Current ($I_0$) | $50\mu A$ |
| Switching Latency ($t_0$) | $5ns$ |
| High Output Resistance ($R_{high}$) | $5000\Omega$ |
| Low Output Resistance ($R_{low}$) | $2500\Omega$ |
| GSHE Strip Resistance ($R_S$) | $100\Omega$ |
| Surface Area ($S_A$) | $110 \times 65nm^2$ |

In order to estimate the advantages of the present circuit, the comparison of evaluated performance has been given between CMOS based and Diode-GSHE based full adder. Fig. 8 compares the simulation results of total power consumptions of 16 bits full adder at 500MHz based on 1) 3-stage GSHE-logic structure, 2) Diode-GSHE logic structure, 3) conventional CMOS structure. GSHE based configurations reduce total power by $2.0\times$, and $3.16\times$ over CMOS, respectively, when maintains the same bit size. Compare with 3-stage structure, diode-GSHE has extra power consumption in diode using, however, it saves even more power with a much lower preset current. As a result, Diode-GSHE logic has a 36.6% lower power dissipation then 3-stage GSHE structure. No to mentioned, to maintain a high enough reliability, 6 or 7 stages may used in multi-stage GSHE logic, which will comes with

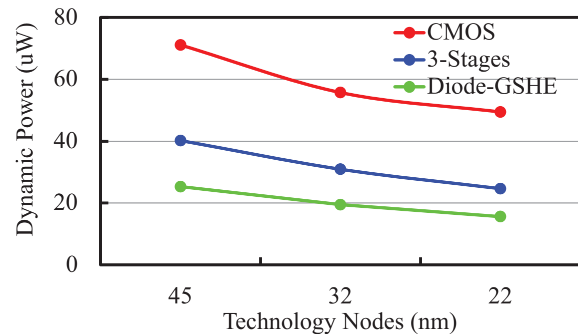


Fig. 8. Dynamic Power Consumption Under 22nm, 34nm, and 45nm tech nodes.

TABLE III
COMPARISON OF FULL ADDERS BETWEEN CMOS CIRCUIT AND PROPOSED DIODE-GSHE CIRCUIT.

| | CMOS | Diode-GSHE |
|---|---|---|
| Dynmaic Power | $49.4\mu W$ | $15.6\mu W$ |
| Write Time | 1ns/bit | 10ns/bit |
| write Energy | 2pJ/bit[14] | 20pJ/bit |
| Static Power | 1.5nW | 0.3nW |
| Area (Device Counts) | 42MOSs | 14 GSHE MTJ + 20 Diodes |

a even higher power consumption. When scales down the technology nodes from 45nm to 22nm, power consumption of all three designs will decrease. For both GSHE based logic structure, the power reduction is proportional to the technology nodes. However, the reduction of CMOS tech is slower than GSHE logics. It proves that GSHE could be a better candidate for technology scaling.

Besides dynamic power consumption, TABLE III summarizes the comparison between CMOS circuit and our proposed structure circuit, under 22nm tech nodes: except the reduction of dynamic power, the static power is also largely reduced. The leakage power in our proposed structure circuit comes from the control line, GSHE device doesn't have ability to float the line, thus, there is one pass-gate applied on each control line to switch the control line from supply voltage, ground, and floating state. Even though, the usage of CMOS transistor is much less than conventional CMOS based circuits, thus, its static power consumption will be much smaller.

The proposed non-volatile logic circuits make it possible not only to eliminate the power consumption, but also to reduce the chip area. With a full adder, a CMOS based full adder with steam bit structure (which has a latch connect with the carry-out output) will cost around 42 MOSs, while GSHE logic requires only 14 GSHE MTJ + 20 diodes, even by using with conventional diodes in this structure, the total area of GSHE based logic is still much smaller than CMOS circuits.

Write time is one of the most important disadvantage in GSHE logic, it also dominates the write energy when updating stored data. GSHE logic has already had a larger update progress comparing with conventional spin-logic utilizing STT-RAM. We can expect that it is possible to further improved the operation speed.

## VI. CONCLUSION

In this paper, we have presented a new technique that reduces leakage and dynamic power in a deep-submicron microprocessor by migrating power and performance-critical hardware resources from CMOS to Spin based Logic. We also provide an unique programming scheme, which adapts the three terminal behaviors of GSHE spin logic device. By leveraging the low current threshold, and high programming speed, GSHE MTJ shows a even better performance in spin logic design. We evaluated the power consumption of a multi-bits full adder under 22nm, 32nm and 45nm technology nodes. The results explored that GSHE spin logic is a great candidate for the continuously scaling down technologies. We believe that emerging non-volatile devices are the best trends for computer system for better performance and efficiency in the future.

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