On-Chip Measurement of Bandgap Reference Voltage Using a Small Form Factor VCO Based Zoom-in ADC

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Abstract— **A robust and scalable technique for measuring the output voltage of a band-gap reference (BGR) circuit is described. The proposed technique is based on an ADC architecture that uses a voltage controlled oscillator (VCO) for voltage to frequency conversion. During production testing, an external voltage reference is used to approximate the voltage/frequency characteristics of the VCO with 5ms test time. The proposed zoom-in ADC approach is manufactured with 0.5μm CMOS process. Measurement results indicate that 12 bits of resolution within the measurement range can be achieved with the zoom-in approach. Worst-case INL for the ADC is less than 0.25LSB (50μV).**

I. Introduction

In recent years, SOCs tend to integrate multiple voltage regulators and therefore multiple bandgap reference (BGR) circuits [1]. The accuracy of the BGR voltage directly affects the circuit performance. High process variations result in wide variations in the BGR behavior, conflicting with the trend of increasing performance demands. Hence, calibration of BGR performance is essential as a first step in the test process.

There are two major challenges in measuring the output voltage of BGR circuits. First, BGR circuits do not present with much drive capability. Hence, voltage measurement needs to be local; the BGR circuit cannot drive long traces in the IC, test busses, and pads. One can remedy this problem by introducing a buffer at the output, and letting the buffer drive a test bus or an I/O pin. However, this would require the integration of an analog buffer with adequate drive capability in addition to the mixed-signal test busses and multiplexers, which would present with significant design-for-test (DFT) overhead. Second, it would be advantageous to measure and calibrate multiple BGRs in a given SOC in parallel since these circuits need to be calibrated before any additional testing can be done. Hence, it is desirable to measure and calibrate BGR voltages with dedicated on-chip measurement circuitry. For this approach to be economically feasible, the measurement circuit needs to be highly accurate and extremely compact. Unfortunately, the accuracy requirements for the measurement is counter-indicative for a low-cost analog-to-digital converter solution. Hence, a built-in-test (BIST) technique is needed to enable small footprint measurement of BGR voltages such that multiple such measurement and calibration steps can be performed at once and locally without the need for additional buffer circuitry.

In this paper, we present a novel zoom-in test method using an on-chip VCO as the voltage to frequency converter and a counter for digitization. The VCO is designed in a way to eliminate any drive need from the BGR circuit by using a current starved pair and the current limit is modulated by the control voltage. As a result, the control voltage of the VCO is connected to the gate of the respective transistors as opposed to the supply voltage (which is the case for many VCO architectures). Voltage/frequency characteristics of VCOs are generally non-linear and extremely susceptible to process variations. In order to obtain the desired accuracy for the voltage measurement, we use a programmable reference from the tester and conduct three to five consecutive adaptive measurements on the VCO frequency. The two (or four) measurements are used to determine the VCO characteristics based on the tester references and the one measurement with the BGR connected to the VCO input is used to determine the actual BGR voltage. The measurements are staggered in a way to adaptively zoom around the BGR voltage and thereby obtain a piecewise linear approximation of the VCO transfer curve around the area of interest. We have manufactured the proposed VCO based zoom-in architecture and manufactured it using a 0.5um single-well process. Measurement results show that even though the VCO current/voltage linearity is limited to 8-bits of the full scale range, we can obtain 13 bits resolution (with respect to FS) by using the zoom-in approach. The entire test time for the BGR voltage using the proposed approach is less than 5ms. We have also implemented the proposed BIST architecture using the 130nm process and conducted extensive post layout simulations to show that technology scaling does not affect the accuracy of the proposed test method.

II. Previous Work

The VCO is commonly used as a voltage-to-frequency converter in ADCs. However, the performance of the VCO based ADC is limited by the nonlinear behavior of the VCO, frequency drifts over time due to 1/f noise, and process, voltage, and temperature variations. In general, there have been two types of VCO-based ADC architectures: closed-loop and open-loop architectures.

In closed-loop architectures, a VCO based quantizer is used for the inherent noise shaping property. VCO non-linearity is suppressed by employing a high gain loop filter and an analog feedback circuitry that requires a multi bit highly linear DAC in the feedback loop [2][3].While closed loop architectures generate accurate and stable results, the area overhead is prohibitive for the application that we have outlined in the Introduction section.

Open-loop architectures generally use digital calibration methods along with enhanced linearity delay elements or pulsed-width modulation techniques [4]-[8]. Enhanced

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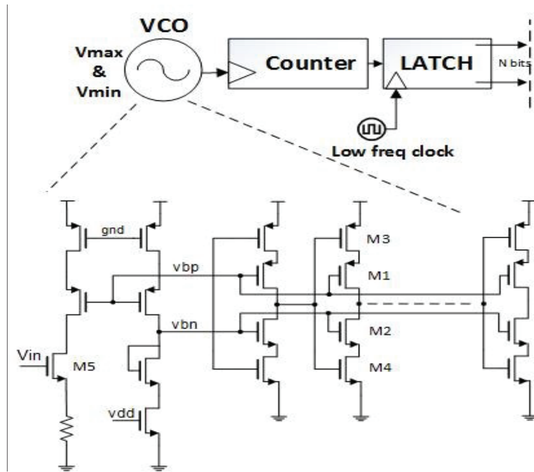

Figure 1: Baseline ADC Architecture

linearity delay elements generally suffer from limited input range [6], which is not controllable. PWM based VCO ADCs operate the VCO only at two frequencies either in f_{HIGH} (correspond to V_{HIGH}) or f_{LOW} (correspond to V_{LOW}), resulting in more linear response. However, this technique requires two active RC integrators and a comparator circuit for pulse width modulation and is not suitable for the application due to large area overhead [8].

Digital calibration approaches have been proposed as an alternative to hardware calibration [4][5][7]. In [4], a VCO based open-loop ADC is proposed for measuring sensor outputs. Drift and nonlinearity problems are solved using an on-chip accurate reference voltage and running it occasionally for calibration. While this technique achieves high resolution, the range is limited and the technique is only applicable to VCOs that present a certain voltage/frequency transfer curve. In [5], a parabolic approximation is proposed to suppress the nonlinearity in a wider range using three on-chip references. However, again the parabolic approximation function is not valid for all VCOs. In [7], an 11-point foreground calibration method is proposed. However, this technique requires the calibration with respect to 11 points in the input range. More importantly, techniques outlined in [4][5][7] utilize a VCO where the supply voltage is used as the control input. This architecture makes the VCO behavior more linear but it requires a buffer to drive the supply input of the ring oscillator, hence increasing the area overhead.

III. Principles of Operation

A. Open-loop VCO-based ADC architecture

Since open-loop VCO based ADC architectures provide the best trade-off for area overhead, we use this architecture as the baseline ADC. Figure 1 shows the simplified ADC architecture. The VCO is designed by using current starved inverters, also shown in Figure 1. The middle transistors in each stage, M1 and M2, form a current bottleneck during the transition. If the saturation current of M1 and M2 is less than the current of the inverter MOS pair, M3 and M4, the bottleneck slows down the transition, hence reduces the oscillation frequency. By changing the bias voltage, it is

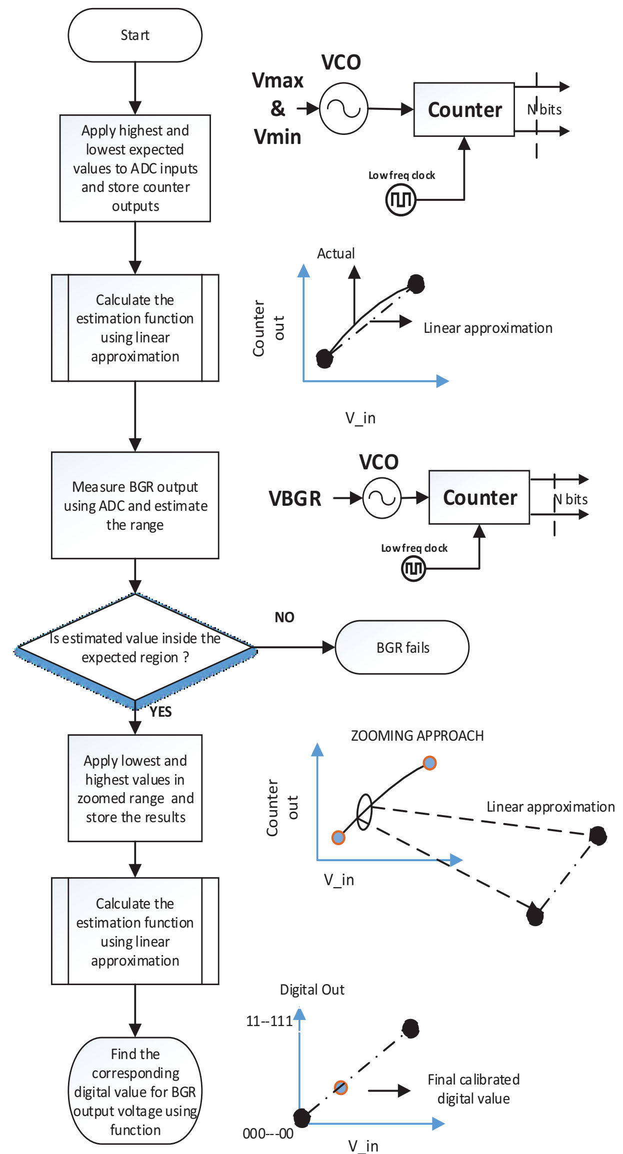

Figure 2: Demonstration of the zoom-in operation for the VCO

possible to modulate the current bottleneck, hence change the frequency. The input stage transistor size and the resistor primarily determine the sensitivity and the linearity of the VCO. Generally, these two parameters cannot be independently set, and there is a trade-off between the sensitivity and the linearity. The output of the frequency is used as the clock input of a counter, which is enabled during a given measurement window

B. Zoom-in non-linearty suppresion technique

The proposed zoom-in ADC based test method is presented in Figure 2. We use a basic voltage controlled ring oscillator architecture with two transistors modulating the current to slow down or speed up the transition of each inverter. The control input is tied to the gate of the current modulation transistors to avoid any significant current draw from the BGR

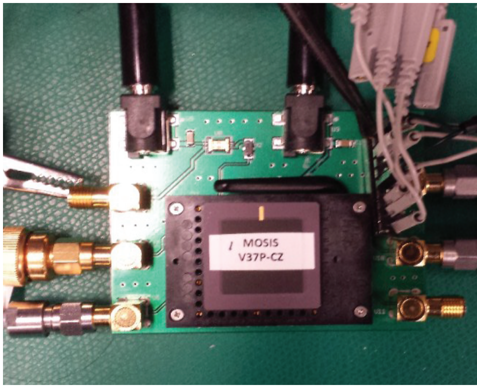

Figure 3: ADC chip with the test board

circuit. Such VCO architectures have been used in ADCs in the literature, albeit with large hardware overhead to overcome the limitations of frequency-to-voltage conversion.

In the proposed method, we use a novel zoom-in approach to estimate the VCO characteristics within a very small region of interest. The uncalibrated BGR voltage may fall within a large range (e.g. 800mV-1.6V). In the first calibration step, the minimum and maximum voltages of this range are applied to the VCO control input via the external (tester) reference. The VCO frequency is measured using a window-enabled counter. Hence, we can obtain two data points in the voltage-to-frequency curve of the VCO. This enables us to approximate the VCO's voltage-frequency characteristics with a linear function. After this step, the BGR circuit output is applied to the control voltage of the BGR and the VCO frequency is measured by the same counter. Using the approximated curve, it is possible to determine the BGR voltage within a certain accuracy that is limited by the linearity of the VCO. We conduct a second, fine calibration step for the ADC. The external tester reference is set to two voltages around the first estimate and a new linear fit is established. The BGR voltage is calculated more accurately with this new curve.

IV. EXPERIMENTIAL RESULTS

The target BGR for our application yields a reference voltage

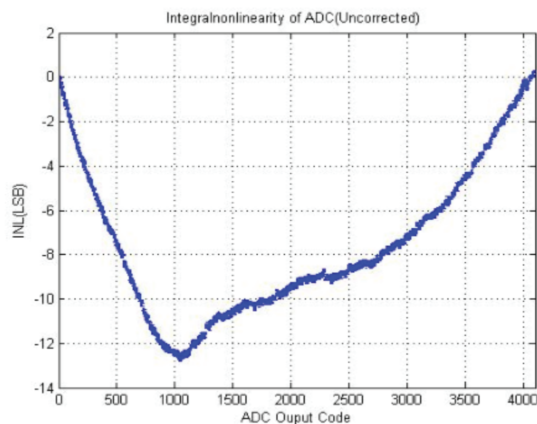

Figure 4: INL of the digitally calibrated ADC with two calibration inputs [5] (Hardware measurements with 0.5µm)

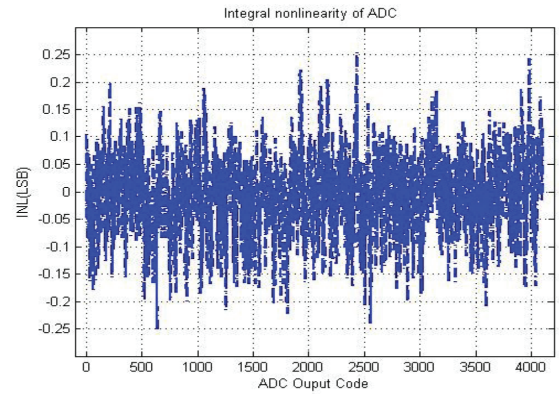

Figure 5: INL of the proposed zoom-in ADC with 4 adaptive calibration inputs (Hardware measurements with 0.5µm)

around 1.25V. Process variations cause 25% uncertainty in this value. Hence, with a reasonable margin, the overall range of interest for our implementation is 850mV-1.65V. We would like to obtain 13 bits resolution with respect to the 1.65V FS voltage; hence 200uV LSB. The ADC is intended to be used to measure the voltage of several BGR circuits on-chip.

In order to evaluate the performance of the zoom-in ADC, we have implemented two versions. First, we implemented the basic VCO together with the counter using the 0.5µm single-well CMOS technology and manufactured this device to obtain hardware results. Next, we scaled this implementation to the 45nm technology and evaluated the resulting design using post layout simulations. .

A. 0.5µm Implementation and Hardware Measurements

With the 0.5µm implementation, we aimed to limit the digital signal frequency to around 10MHz. The VCO is designed with 7 stages to achieve this frequency target. The resistor R in Figure 1 is set to 14.5kΩ to achieve the best linearity. The frequency step for this VCO is around 8kHz. We used a 15-bit counter to accommodate the opposite process corner for faster VCOs. Total area of the ADC is 0.031 mm^2.

The test board designed for the prototype IC is shown in Fig 3. A highly accurate DC source and a logic analyzer are connected to the input and output of the circuit respectively, and a PC is used for test automation. The test program that serializes the reference input and BGR connections and sets the reference voltages for the zoom-in rage is written in Labview

The first step is to evaluate the integral non-linearity of the digitally calibrated ADC without the zoom-in approach (similar to the techniques in [4-7]). We use both a parabolic and a linear approximation of the VCO voltage/frequency characteristics. We then calculate the maximum deviation of the actual ADC response from the approximated curve. Note that in all these previously proposed calibration techniques, the inputs are pre-determined. The major difference of our proposed zoom-in technique is that the inputs are adaptively set with respect to the reading from the BGR circuit. Figure 4 shows the INL of the digitally calibrated ADC with two calibration inputs [5]. The INL is as large as 13LSB, corresponding to 2.7mV. Even for the parabolic calibration

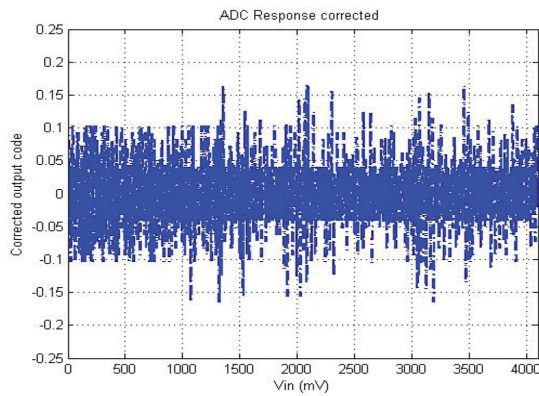

Figure 6: INL of the proposed zoom-in ADC with 4 adaptive calibration inputs (130nm simulation)

technique (with 4ms test time) presented in [5], the calibrated INL is 5.5LSB, corresponding to 1.1mV. This error is not acceptable for BGR calibration. With the application of the zoom-in approach, the INL of the ADC can be reduced to 0.25LSB, corresponding to 50uV. The INL per code of the proposed ADC is shown in Figure 5. The trade-off is the increase in the test time from 3ms to 5ms, which is negligible.

B. 130 nm implementation and post-layout simulation results

One advantage of the proposed ADC architecture is that it is easily scalable since it comprises mostly of digital blocks. In order to evaluate the scalability of the design, we also implemented the proposed zoom-in architecture with the 130nm technology and conducted post-layout simulations. All parameters of the ADC are similar to the first implementation.

The proposed technique uses 4 calibration inputs and yields an INL of less than 0.16LSB as shown in Figure 6. The test time 4ms is considered negligible compared to the overall test time of the target SOC application which is more than several seconds. The major difference of the second implementation is that it is designed with a double well technology which enables us to use an isolated pwell for transistor M5 in Fig1 and connect the bulk of NMOS transistor directly to the source of the transistor. Hence, the threshold voltage of the transistor is independent of source to bulk voltage and it is more linear.

The ADC occupies an area of 0.045 mm^2, which corresponds to 4% of the area of the target reference system. The area overhead is well within acceptable range for analog DFT. It should be noted that even if this ADC is not integrated as a DFT technique, at least an analog buffer and an analog multiplexor are necessary to measure BGR circuit voltage externally due to limited drive capability. In comparison to these circuits, the proposed ADC occupies a similar area. In the final version of the paper, we will provide hardware measurement results for the second implementation.

V. CONCLUSION

In this paper, we present a highly accurate and low cost built-in test solution for BGR output voltages. Our technique is based on using an area efficient on-chip VCO based ADC and adaptive digital calibration to suppress the nonlinearity and overcome process variations of the VCO

A prototype IC is manufactured using 0.5µm technology. The proposed technique is validated in the lab environment using the prototype IC, a highly accurate DC source, a logic analyzer, and a PC based automation system. Hardware measurement results show that the non-linearity of the ADC is suppressed from 13LSB to less than 0.25LSB for a wide input range of 820mV whereas process variations and drift have no significant impact on the ADC behavior.

In order to evaluate scalability and the effect of higher process variations, the ADC is also implemented using the 130nm process technology. Post-layout simulations show that the proposed ADC can achieve similar results in terms of measurement accuracy than 4% area overhead for the target reference system.

VI. ACKNOWLEDGEMENTS

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