Impact of Interconnect Multiple-Patterning Variability on SRAMs

Ioannis Karageorgos*† Michele Stucchi* Praveen Raghavan* Julien Ryckaert* Zsolt Tokei*
Diederik Verkest* Rogier Baert* Sushil Sakhare* Wim Dehaene†*

* imec, Kapeldreef 75, B-3001 Leuven, Belgium
† KU Leuven, ESAT, B-3001 Leuven, Belgium
email: ioannis.karageorgos@imec.be

***Abstract*— The introduction of Multiple Patterning (MP) in sub-32nm technology nodes may pose severe variability problems in wire resistance and capacitance of IC circuits. In this paper we evaluate the impact of this variability on the performance of SRAM cell arrays based on the 10nm technology node, for a relevant range of process variation assumptions. The MP options we consider are the triple Litho-Etch (LE^3) and the Self Aligned Double Patterning (SADP), together with Single Patterning Extreme-UV (EUV). In addition to the analysis of the worst-case variability scenario and the impact on SRAM performance, we propose an analytical formula for the estimation of SRAM read time penalty, using the RC variation of the bit line and the array size as input parameters. This formula, verified with SPICE simulations, allows a fast extraction of the statistical distribution of the read time penalty, using the Monte-Carlo method. Results on each patterning option are presented and compared.**

I. Introduction

As the semiconductor industry struggles to keep pace with Moore's Law, it faces ever increasing challenges. Many of these challenges are lithography related [1]. Dry and later immersion lithography at 193nm drove successfully the semiconductor roadmap down to 45nm node [2]. However, as the resolution of photoresist patterns begins to blur at around 45 nm half-pitch [3], a single lithography exposure is not sufficient for printing the denser features of the next technology nodes. The two most apparent solutions to overcome this issue can be either the transition to a shorter wavelength source lithography, as in Extreme-UV (EUV), or the use of Multiple Patterning (MP) which is an enhanced lithography process that produces multiples of the minimum-sized features. However, EUV has been confronted with a series of materials and source issues, making it not yet a manufacturable solution. As a result, the use of MP in optical lithography currently appears the only viable solution for further technology scaling [4], [5]. In the semiconductor industry, double patterning was introduced for the 32nm half-pitch node and beyond [2], allowing double feature density with the incumbent technology.

There are several technology options available for double or multiple patterning [6]. Yet, the two most viable and widely adopted options in industry for the 10nm technology node (imec N10 node), which are considered also in this paper, are: the Self Aligned Double Patterning (SADP) and the triple Litho-Etch approach (LELELE) [5], [7], [8].

The use of MP options in Back-End-of-Line (BEOL) introduces new variability challenges in wires. MP variations can lead to different geometries and spacing in arrays of parallel wires, which results in variations in resistance, capacitance and coupling-capacitance. This leads to a performance unbalance in supposedly identical parallel wires and may pose problems in circuits sending and receiving signals through these parallel interconnects. The continuous reduction of interconnect dimensions predicted by the scaling roadmap [9] can only exacerbate these problems.

In this study we evaluate the impact of MP options on the performance of SRAMs based on the N10 technology node. The assessment includes the comparison of multiple Litho-Etch and SADP options together with Single Patterning (SP) EUV for a relevant range of process variation. The content of this paper is organized as follows: Section II covers the impact of worst case variability on SRAM read time, using time-to-discharge of bit lines (td) as the figure of merit (FOM). In Section III a simple analytical formula is proposed for the estimation of td penalty as a result of bit line RC variations. Based on the formula, we present a comparison of td penalty distribution for each patterning option using Monte-Carlo sampling of process variation as input. The conclusions of this study are presented in Section IV.

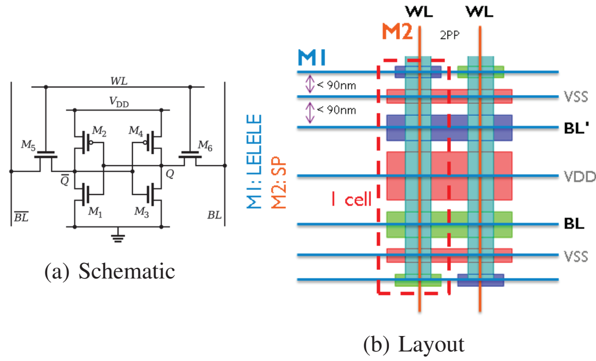
II. SRAM worst case variability study

The variability assessment presented in this section is based on the six-transistor (6T) SRAM cell (Fig. 1a). As a target layout we used a high-density optimized SRAM cell design, developed at imec for the N10 node (Fig. 1b). This layout uses unidirectional (u/d) horizontal metal1 at minimum spacing for the bit lines and power grid and u/d vertical metal2 for the word lines. The three options we consider for metal1 patterning are: LE^3, SADP (because of u/d arrangement, layout can be easily derived with double patterning SADP) and single patterning EUV. The top view of metal1 layout and the patterning details for each option are shown in Fig. 2.

A. Simulation environment

This analysis is based on SPICE-level simulations of the SRAM cell array including the N10 transistor compact models. The netlists with parasitics were extracted from the SRAM array layout by a parameterized Layout Parasitic Extraction (LPE) tool, developed at imec and based on the standard LPE tool flow but adapted to include process variability. The tool

978-3-9815370-4-8/DATE15/©2015 EDAA



(a) Schematic

(b) Layout

Fig. 1: 6T SRAM cell circuit and layout.

inputs are technology parameters (layer thickness, tapering angles, material properties, etch and CMP parameters) and MP-related layer operations (CD, overlay and spacer thickness variation) together with the target layout (GDSII); the tool generates the LPE deck, runs the simulations and stores the target metrics (R, C, CC) or netlists (with parasitics), in an iterative loop. The implementation of Monte-Carlo sampling of the input variability parameters allows the extraction of the RC distribution for any wire (e.g. the bit line).

The technology parameters and the MP process variation assumptions we use in our simulations are based on in-house experimental data. The most relevant of these assumptions are the following:

- 3σ CD variation of $3nm$ for LE^3, SADP core layer and EUV (although this value may be pessimistic for EUV)
- 3σ SADP spacer variation of $1.5nm$
- $3nm$ to $8nm$ range of 3σ OL error for LE^3
- metal1_B and metal1_C are aligned to metal1_A for LE^3
- spacer-defined bit lines for SADP (Fig. 2:SADP)

B. Variability worst cases for C_{bl}

Our simulation results show that bit line capacitance (C_{bl}) is the dominant parameter affecting the SRAM performance, even for long arrays (up to 512 cells). The resistance of bit lines is relatively low due to the non-minimum CD of bit line wires, which is typical in SRAM. We focus on metal1 layer since this is the layer of the bit lines in this design and because it is often the most critical interconnect layer [10]. Initially we consider the extreme case of $8nm$ 3σ OL error for LE^3. Using all combinations of CD and OL errors as input parameters, we identified the worst case scenario for each option with respect to C_{bl} increase. The results are listed in Table I. Patterning details and the consequent layout distortion for each case are shown in Fig. 2. Each color of LE^3 in Fig. 2 represents a different patterning step and 'plus', 'minus' signs refer to 3σ values.

The impact of LE^3 worst case variability on C_{bl} is quite high. On the other hand, for SADP, because of the self-aligned nature of the process, the impact is limited and even smaller than EUV (assuming the same $3nm$ 3σ CD in EUV).

C. Array size & worst case td variation

The impact of RC_{bl} variation on td is also related to the size of the array (since the FEOL resistance path doesn't scale with

TABLE I: Worst case variability for each patterning option.

Pat. option	Param	Layer	Value	R & C impact
LELELE	CD CD CD OL(vert.) OL(vert.)	metal1_A metal1_B metal1_C metal1_B metal1_C	$+3\sigma$ $+3\sigma$ $+3\sigma$ -3σ $+3\sigma$	C_{bl} : $+61.56\%$, R_{bl} : -10.36%
SADP	CD CD	metal1_core metal1_spacer	-3σ -3σ	C_{bl} : $+4.01\%$, R_{bl} : -18.19%
EUV	CD	metal1_A	$+3\sigma$	C_{bl} : $+6.65\%$, R_{bl} : -10.36%

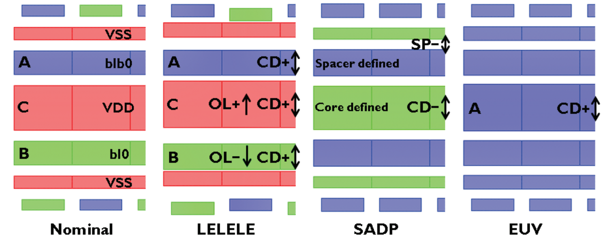


Fig. 2: Worst case variability & metal1 layout distortion.

array size). In our Design of Experiments (DOE) we consider four different SRAM array sizes of 16 word lines (wl), 64 wl, 256 wl and 1024 wl and a fixed number of 10 bit line (bl) pairs (or 10bit word-length). An overview of this arrangement is shown in Fig. 3. The length of bl is proportional to the number of wl. We keep the bl count fixed because it is not relevant for this study; their number is large enough to consider the simulation results of the central lines not affected by edge related effects.

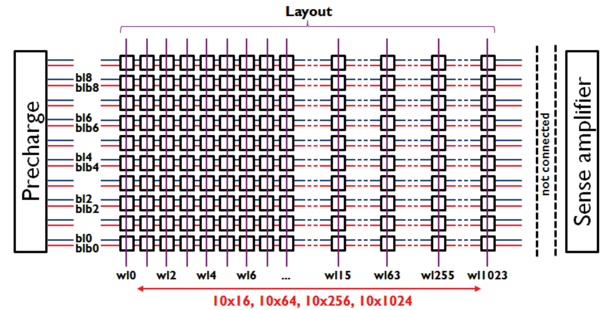


Fig. 3: Overview of the SRAM arrays used in simulations.

Our simulation assumptions include:

- vdd, precharge, wl enable: $0.7V$
- sense amplifier sensitivity: $|V_{bl} - V_{blb}| = 0.07V$
- driving strength of the precharge circuit scales with (horizontal) array size

The simulation results of the worst case analysis, when using 3σ OL error of $8nm$, are shown in Fig. 4. The x axes give the different array sizes and the y axes give the nominal (without patterning variability) td value along with the variability-induced td penalty (td_p) for each option and array size. The worst case of LE^3 variability shows up to ~20% td_p. Worst case impact of SADP and EUV is limited and less than 3% td_p in all cases.

Since this is a worst case analysis, it is important to evaluate

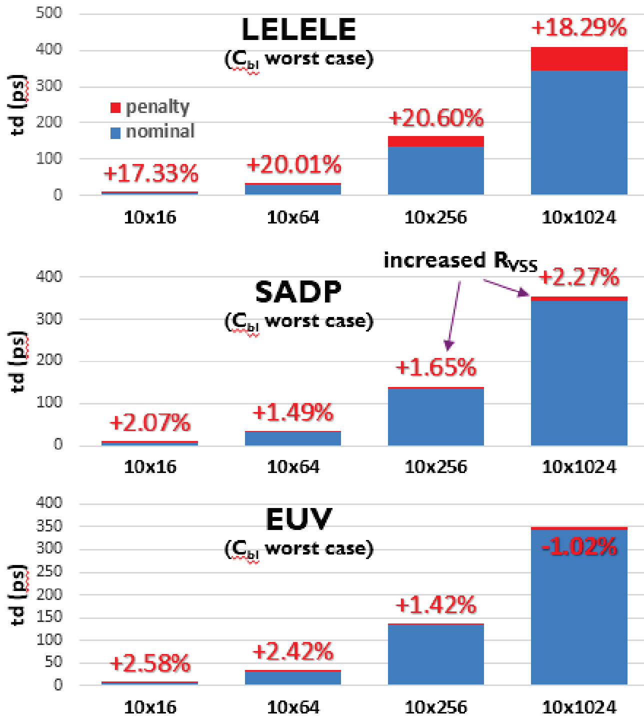


Fig. 4: Worst case wire variability impact on td.

the probability of the worst case occurrence. However, the extraction of statistical distributions of td_p by simulation of full netlists of SRAM arrays, including parasitics, would be extremely time consuming. Furthermore, there is an unclear trend in td_p values for different array sizes: td_p initially increases and later tends to reduce for LE^3 and becomes even negative for EUV, as shown in Fig. 4.

These issues are addressed by an analytical formulation of td & td_p, presented in the next section.

III. Analytical Formulation & Statistical Distribution of td_p

The analytical formula to calculate td should take into account the RC_{bl} variability and the array size as parameters. Then, td_p can be derived as the ratio of: td including RC_{bl} variability over nominal td (without RC_{bl} variability), for a given array size.

A. Lumped RC delay formula

Based on the transient response function of an RC circuit with a constant input voltage V [11]:

$$V_{out}(t) = \left(1 - e^{-t/RC}\right) \cdot V \tag{1}$$

we can define td as:

$$td = t = a \cdot RC \tag{2}$$

where RC is the time constant (with R the lumped resistance of the bl net and C the lumped capacitance) and a is a constant defined by the target discharge level. Constant a can be derived from eq. (1) by defining the ratio $Vout/V$ and by solving for t. For example, a is 1 for a charging level V_{out}≈63.2% of the applied voltage (V). In this case study, for 10% discharge level, a is calculated as:

$$0.1 = 1 - e^{-t/RC} \Rightarrow t \approx 0.105 \cdot RC \tag{3}$$

Breaking RC into the [lumped] resistance and capacitance components and including the length of the array as n, the following equation can be derived:

$$td = a \cdot \Big(n \cdot R_{bl} \cdot Rvar + R_{FE}\Big) \cdot \Big(n \cdot (C_{bl} \cdot Cvar + C_{FE}) + C_{pre}(n)\Big) \tag{4}$$

where: n is the the bl length as the number of SRAM cells connected in series, R_{bl} is the bl resistance of one SRAM cell, $Rvar$ is the bl resistance variation (induced by the patterning option) expressed in percentage $(1 + x\%)$, R_{FE} is the Front-End resistance of the 'discharge path' or the resistance of the pull-down NMOS transistors in one cell (constant value), C_{bl} is the total capacitance of the bl net of one SRAM cell, $Cvar$ is the bl capacitance variation (induced by the patterning option) expressed in percentage $(1 + x\%)$, C_{FE} is the Front-End capacitance or the capacitance at wl pass-gates where the bl is connected to, and $C_{pre}(n)$ is the capacitance of the precharge circuit which is connected to the bit lines. The value of C_{pre} is a function of n according to the scaling formula that is used.

If we transform the equation to a general polynomial in n the result is a second-degree-like polynomial of the form:

$$\begin{aligned} td = {} & n^2 \cdot \Big(a \cdot R_{bl} \cdot Rvar \cdot (C_{bl} \cdot Cvar + C_{FE})\Big) \\ & + n \cdot \Big(a \cdot R_{FE} \cdot (C_{bl} \cdot Cvar + C_{FE}) \\ & + a \cdot R_{bl} \cdot Rvar \cdot C_{pre}(n)\Big) + a \cdot R_{FE} \cdot C_{pre}(n) \end{aligned} \tag{5}$$

In this form it can be seen that there is a quadratic dependency on n, plus an -almost- linear dependency on n, plus an -almost-constant term (loosely depended on n). Thus, the time penalty td_p is expressed as a rational function of two polynomials: actual td over nominal td (td_{nom} where $Rvar, Cvar = 1$). The polynomial nature of td_p and the negative values of $Rvar$ in the worst cases considered, are the primary reasons for the fluctuation in td_p values over various array lengths.

To test the formula we substitute the values of all parameters (obtained from our models) and compare the results with the simulated td_{nom} values for the different array lengths (n). Table II shows the results of this test.

TABLE II: Formula versus simulation td_{nom} values.

Array size	Simulation	Formula
10x16	$5.59E-12$	$2.09E-12$
10x64	$30.07E-12$	$7.56E-12$
10x256	$134.62E-12$	$30.87E-12$
10x1024	$344.85E-12$	$144.02E-12$

The results show a deviation between simulation and formula td_{nom} values. This deviation is expected since the formula is based on the lumped RC equation, though bl is a distributed line which can be better approximated with the

Elmore delay. Furthermore, other components are not behaving as lumped elements, like R_{FE}, but are considered as lumped in the formula; or are not taken into account at all (though are included in simulation deck), like leakage currents, RC contribution of metal vias, etc.

Yet, if we introduce the same RC variation as in our simulation, the analytical formula gives very similar td_p percentage values with respect to the simulation results. Table III shows the results for the considered worst cases of variability.

TABLE III: Formula versus simulation td_p values (%) using the worst case variability.

Method	Array size	LELELE	SADP	EUV
Simulation	10x16	17.33	2.07	2.58
	10x64	20.01	1.49	2.42
	10x256	20.60	1.65	1.42
	10x1024	18.29	2.27	-1.02
Formula	10x16	18.37	1.88	2.20
	10x64	20.43	1.62	2.15
	10x256	20.49	0.88	1.66
	10x1024	18.84	-4.00	-1.47

The formula gives a good approximation of td_p for LE^3 and EUV but not for the SADP case. For $n > 64$, the simulation of SADP shows an uptrend of the td_p value (Fig 4), which is not captured by the formula. A possible reason is that for SADP in this design there is an anti-correlation of the R_{bl} and R_{VSS} since CD variation of the first introduces reversed CD variation to the latter. In the worst case of SADP there is a drop in R_{bl} of $\sim 18\%$ which introduces an increase in R_{VSS}, that is not considered in the formula. Since this R_{VSS} change is negligible for short array lengths, the formula can still approximate td_p correctly for SADP for $n \leq 64$; this is not the case for SADP and longer array lengths.

B. Monte-Carlo distribution of td_p

Using the analytical formula, the statistical distribution of td_p can be easily extracted given the RC_{bl} variation distribution. We use our parameterized tool to extract the RC_{bl} distribution with Monte-Carlo sampling of process variability for each option as input. For the LE^3 case we use four values of 3σ OL error in the range from $3nm - 8nm$. An example of the Monte-Carlo distribution of td_p for $8nm$ OL and array size of $10x64$ ($n = 64$), is shown in Fig. 5.

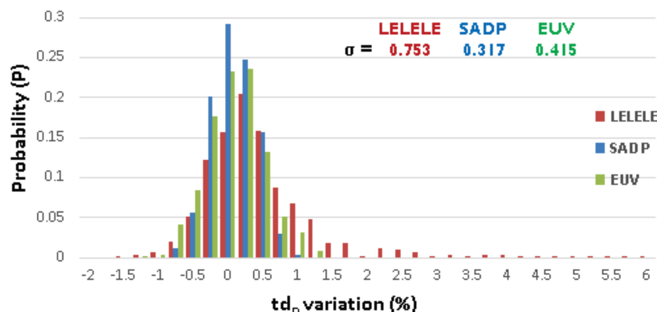


Fig. 5: Monte-Carlo td_p distribution: $8nm$ 3σ OL, $n = 64$.

The standard deviation of td_p for LE^3 with $8nm$ 3σ OL is more than double compared with SADP. A summary of all standard deviation values for the three patterning options and for a set of 3σ OL values is included in Table IV.

TABLE IV: Patterning options & td_p σ values.

Array size	Patterning option	Std. deviation (σ)
$10x64$	LELELE $3nm$ OL	0.414
	LELELE $5nm$ OL	0.454
	LELELE $7nm$ OL	0.552
	LELELE $8nm$ OL	0.753
	SADP	0.317
	EUV	0.415

The OL error plays a decisive role in LE^3 performance impact distribution. Tight OL control, with a 3σ error of $3nm$ or less, is required for LE^3 to reach similar performance variation values with SADP and EUV. If this tight OL budget cannot be met and if the introduction of EUV in IC manufacturing keeps being postponed, SADP appears to be the optimal MP option, as far as performance variation impact is concerned.

IV. Conclusions

In this paper we simulate the performance variation in SRAMs, due to the interconnect variability generated by MP options and EUV. In the worst case scenario of interconnect variability, the read time penalty introduced by the LE^3 option can be as high as $\sim 20\%$, compared to $< 3\%$ for SADP and EUV. The full distribution of the performance variations, obtained from Monte-Carlo simulations based on an analytical model of the read time, confirms the low impact of SADP. The distribution of LE^3, on the other hand, shows the higher performance variation, with a standard deviation (σ) value as much as double than the other options. The main contributor to this performance variation of LE^3 is the exposure overlay (OL) error. Limiting the 3σ OL error to $\leq 3nm$ allows LE^3 to reach comparable performance variations with respect to SADP and EUV.

References

[1] B. Smith, "Immersion techniques carry 193nm lithography beyond the 65nm node," Rochester Institute of Technology, SPIE's oemagazine, Jul 2004.
[2] C. Fonseca *et al.*, "Advances and challenges in dual-tone development process optimization," Proc. SPIE vol. 7274, 72740I, Mar 2009.
[3] T. Honda *et al.*, "Influence of resist blur on ultimate resolution of ArF immersion lithography," J. Microlith., Microfab., Microsyst., Vol. 5, 043004, Oct-Dec 2006.
[4] "List of leading EUVL technical challenges," 2014 International workshop on EUVL, Makena beach, Maui, Hawaii, Jun 2014.
[5] R. Ghaida, P. Gupta, "Role of design in Multiple Patterning: technology development, design enablement and process Control," IEEE Design Automation and Test in Europe (DATE), pp. 314 - 319, Mar 2013.
[6] A. Hazleton *et al.*, "Exposure tool requirements for 32nm node: Double Patterning and alternatives," International Symposium on immersion lithography extensions, Sept 2008.
[7] D. Abercrombie, "Mastering the magic of Multi-Patterning," Mentor Graphics white paper, Dec 2013.
[8] Nikon eReview, "Lithography experts report on advanced multiple patterning solutions and cost," Spring 2014.
[9] International Technology Roadmap for Semiconductors. [Online]. Available: http://www.itrs.net/Links/2013ITRS/Summary2013.htm.
[10] T. Chiou, M. Dusa, A. Chen, D. Pietromonaco, "Lithographic challenges and their solutions for critical layers in sub-14nm node logic devices," Proc. SPIE vol. 8683, 86830R, Apr 2013.
[11] J.M. Rabaey, "Digital Integrated Circuits: A Design Perspective," second edition, Prentice Hall, 0130909963 978-0130909961, Jan 2003.