Sub-10 nm FinFETs and Tunnel-FETs: From Devices to Systems

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***Abstract*—In this paper, a detailed device/circuit/system level assessment of sub-10nm GaSb-InAs Tunneling Field Effect Transistors (TFET) versus Silicon FinFETs operating at near-threshold voltages is reported. A source underlapped GaSb-InAs TFET is used to achieve lower subthreshold swings than previously reported TFETs and an analytical justification is provided to explain the observed improvement. Through atomistic, 2D ballistic simulations using self-consistently, coupled Non-equilibrium Green's Function (NEGF)-Poisson approach, GaSb-InAs TFET and Silicon FinFET device characteristics are derived from which compact models are extracted for SPICE simulations. Circuit simulations of a 6-stage inverter chain show that sub-10nm underlapped TFETs are especially suited for near-threshold computing because of their ability to achieve higher throughput while consuming ~100x lower power compared to Si FinFETs. To analyze the suitability of sub-10 nm TFETs for medium-throughput and ultra-low power applications in future very large scale integrated designs, a LEON3 processor is synthesized at V_{DD}=0.25V. The impact of interconnect parasitics on the performance of TFETs is considered by studying the power-performance of the LEON3 under varying wire-load conditions. Under moderate interconnect parasitics, TFETs-based processor is shown to exhibit more than 50% power reduction compared to FinFETs.**

Keywords—Double-gate (DG), FinFET, Heterojunction TFET (Het-j TFET), International Technology Roadmap for Semiconductors (ITRS), LEON3 Processor, Subthreshold Swing (SS), Tunnel field-effect transistors (TFETs).

I. INTRODUCTION

Continuing scaling of transistors as density approaches the terascale regime requires evaluating new devices that can perform on several metrics beyond density scaling, such as performance improvements and energy efficiency. One of the major roadblocks in the continued scaling of standard CMOS technology is its alarmingly high leakage power consumption. Although circuit and system level methods can be employed to reduce power, the fundamental limit in the overall energy efficiency of a system is still rooted in the MOSFET operating principle: an injection of thermally distributed carriers, which does not allow subthreshold swing (SS) lower than 60mV/dec at room temperature [1-4]. FinFETs have been shown to achieve excellent control over short-channel effects in ultra-scaled technologies, but further scaling beyond 10nm nodes results in high off-state currents due to direct source to drain tunneling [5]. Tunnel field-effect transistors (TFETs) are of interest for future low-power technologies due to their ability to surpass the 60mV/dec lower limit on SS at room temperature [1-4].

To date, the published work on sub-10nm TFETs has mainly focused on device level dc transfer characteristics and not on circuit/system level performance, especially when the interconnect parasitics are becoming higher than the gate parasitics. In this paper, we compare a sub-10nm gate-length GaSb/InAs double-gate (DG) n/p-TFET with an n^+/p^+-doped underlap layer towards the source with symmetrically underlapped DG n/p Silicon-FinFET [5], develop look-up table based device models to perform SPICE-level simulations of 6-stage inverter chain based on these devices and synthesize a LEON3 processor to assess the performance of TFETs in comparison to FinFETs, at near-threshold voltage of 0.25V. We also include varying wire-load models in our cell libraries to assess the impact of interconnect parasitics on the performance of TFET-based system-level implementation.

Major conclusions of this paper can be summarized as follows:

1) Underlapped n/p-TFETs based on GaSb/InAs heterostructure at sub-10nm nodes are shown to exhibit lower SS than previously reported TFETs. A simple analytical formulation is presented that supports the observed improvement in SS.

2) Sub-10nm TFETs are particularly suited for medium throughput ultra-low power applications. In spite of lower currents than FinFETs, the delays are lower for loaded 6-stage inverter chain realized using TFETs at sub-threshold voltages.

3) Under moderate interconnect parasitics of the order of gate parasitics, at near-threshold voltages, sub-10nm TFETs can operate at similar performance as FinFETs but at ~50% lower power consumption. Under heavy interconnect dominated scenarios; FinFETs are a better candidate than TFETs for high-performance applications.

The rest of the paper is organized as follows. Section II summarizes previously reported TFET structures and their limitations. Section III describes the n/p-FinFET and TFET device structures, the simulation setup and methodology used to generate SPICE compatible look-up table models. In Sections IV and V, we compare the I-V and C-V curves of these devices and discuss why TFETs are a better choice over FinFETs for near-threshold computing. In Section VI, delay-power characteristics of 6-stage inverter chain realized using these devices is compared. In Section VII, we implement a

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LEON3 processor to discuss the potential of TFETs in future computing applications in the presence of interconnects. Section VIII summarizes the key results from this work.

II. Previous Work

III-V semiconductor based TFETs have gained wide interest due to the availability of wide range of compositionally tunable effective barrier heights [6], [7]. Simulations of vertical homojunction-based TFETs have been reported by Asra et al. [8] for Si and by Agarwal et al. [9] for InAs. However, the homojunction TFETs are severely limited by their low on-current. GaSb/InAs heterojunction TFET is one of the leading TFET options because of the broken-gap band-alignment which results in high drive current [10],[11]. Although different TFET structures have been reported in the literature [2], [3] and a vertical n-type TFET has been proposed in [12] to improve I_{ON} and SS, the on-currents reported in these works are well below that of CMOS, or they exhibit threshold voltages higher than 0.4V. Moreover, the reported p-type TFETs usually require gate voltages larger than the power-supply voltage to operate [13], which makes them difficult to be integrated in digital circuits. System-level evaluation of 22 nm TFETs by Swaminathan et al. [14] shows that TFET cores present more energy efficient alternative to conventional CMOS processors at near-threshold voltages.

In this work, we utilize a GaSb/InAs DG p-TFET, with a p^+-doped underlap layer of GaSb towards the source, which exhibits low SS (~15-20 mV/dec), on-currents similar to n-TFETs and can be integrated in CMOS process and digital circuits. The n/p-TFET has a gate-length of 9 nm, i.e. ITRS 2022 node [15] with a source underlapped region of 6 nm.

III. Device Structure And Simulation Approach

A. n/p Silicon-FinFET

We consider a symmetrically underlapped double-gate Si FinFET for our comparison as shown in Fig. 1 with parameters listed in Table I. Underlapping has been used since it can reduce the thermionic component and direct source to drain tunneling component of leakage current by increasing the effective channel length [5].

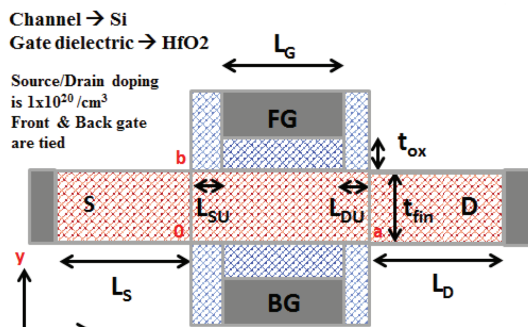

Fig.1. Symmetrically underlapped FinFET device structure.

The spacer above the underlap is composed of Si_3N_4 (ε_r=6.3) and high-K HfO_2 (ε_r=25) has been considered for gate oxide.

B. n/p GaSb-InAs TFET

The vertically-grown double-gate (DG) GaSb-InAs n-TFET with an intermediate n^+-doped InAs layer between p^+ GaSb-source and intrinsic InAs-channel is shown in Fig. 2(a). Similarly, a p-TFET utilizes an intermediate p^+-doped GaSb layer between n^+-InAs source and intrinsic-GaSb channel as shown in Fig. 2(b). Abrupt doping profile has been assumed for simulations. The devices can be grown on GaSb using solid-source molecular-beam-epitaxy process [12] with in-situ source doping, thus realizing abrupt source-channel junctions, another important factor determining the performance of TFETs [13].

TABLE I
FinFET/TFET Device Parameters

Quantity	n-FinFET	p-FinFET	n-TFET	p-TFET
L_G(nm)	5	5	9	9
L_S,L_D(nm)	30	30	30	30
T_{OX} (nm)	1.9	1.9	1.9	1.9
T_{FIN} (nm)	2.725	2.725	3	3
N_A (cm^{-3})	$1X10^{20}$	$1X10^{20}$	$4X10^{18}$	$1X10^{19}$
N_D (cm^{-3})	$1X10^{20}$	$1X10^{20}$	$1X10^{19}$	$4X10^{18}$
N_{UN}(cm^{-3})	-	-	$1X10^{19}$	$4X10^{18}$
L_{DU} (nm)	1.09	1.09	0	0
L_{SU} (nm)	1.09 nm	1.09 nm	6	6
$\|V_{DS}\|$	0.5 V	0.5 V	0.5 V	0.5 V
$\Delta\Phi_g$ (gate-workfunction)	0.293 eV	0.881 eV	-0.5 eV	-0.8eV

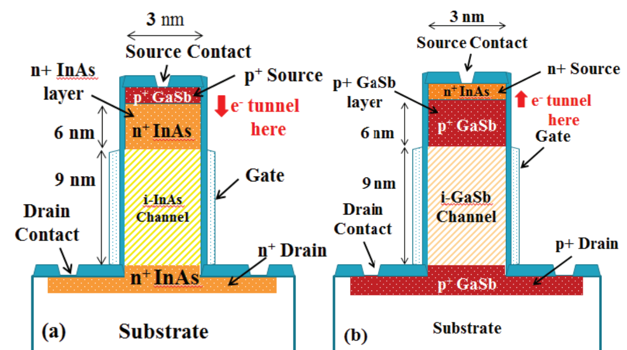

Fig.2. Schematics of vertical (a) Underlapped n-TFET (b) Underlapped p-TFET device structures under study. The configuration parameters are listed in Table I.

C. Atomistic Device Simulation

The simulations were performed using NEMO5, which is an atomistic quantum mechanical device simulator based on a tight-binding approach that calculates carrier density self-consistently with the Poisson equation [16]. We used atomistic sp^3s^* tight-binding model, with spin-orbit coupling, to solve coupled two-dimensional Poisson-NEGF transport equations for simulating TFETs. For FinFETs, $sp^3d^5s^*$ tight binding

model was used for device simulations. Transport is assumed to be ballistic. The design methodology for generation of SPICE compatible look-up table models from the device simulations is summarized in Fig.3. For SPICE simulations, the fin width was set to four times the fin thickness.

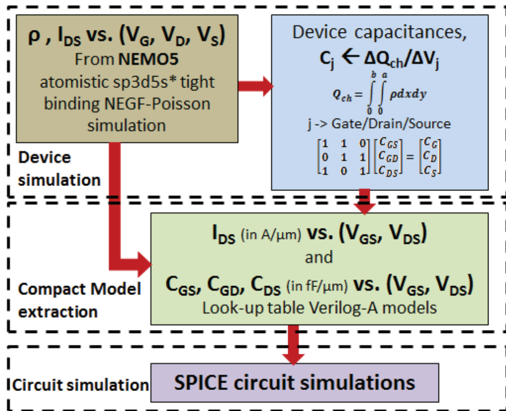

Fig.3. Simulation flow for generation of I-V and C-V look-up table models for n and p-type FinFETs / TFETs. V_{GS} and V_{DS} were swept from 0V to 0.5V.

IV. TFET DESIGN OPTIMIZATION

A. Non-underlapped v/s Source- underlapped TFETs

To improve the current-voltage characteristics of our TFET, we adopt a 6nm long n+ underlap InAs layer toward source side. A comparison of I_D-V_{GS} characteristics of our 6nm underlapped n/p TFETs and that of a non-underlapped, conventional n/p TFET is shown in Fig. 4.

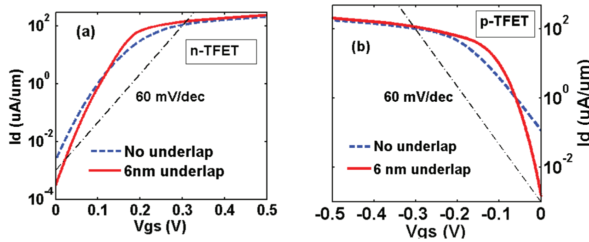

Fig.4. I_D vs V_{GS} for non-underlapped and 6nm underlapped (a) n-TFET (b) p-TFET. Underlapped TFETs yield lower SS at low-voltages, thereby resulting in lower OFF currents while exhibiting same ON currents.

Our TFETs exhibit lower SS while giving the same on-currents. To understand this behavior, a plot of the band-diagrams and electron-density along the current-transport direction, near the center of the fin for n-TFETs, at the onset of tunneling, is shown in Fig. 5.

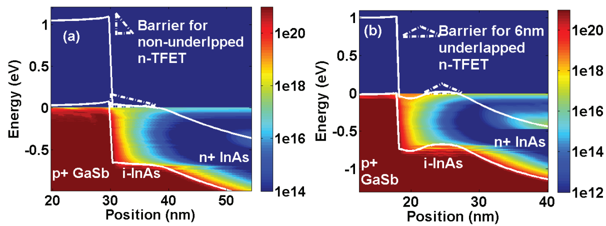

Fig.5. Band diagram and energy resolved charge density for (a) non-underlapped n-TFET (b) 6nm underlapped n-TFET.

The transport in an underlapped TFET is a two-step tunneling process, the standard broken-gap band-to-band tunneling followed by direct underlap-to-drain tunneling. We achieve a low SS by engineering the second tunneling barrier. The WKB approximation [16] for the triangular barrier shows that the transmission, T(E), increases exponentially as the tunneling width decreases (Eqn. 1). The top of the barrier, U_o, is equally affected in both the devices for the same increase in gate voltage. The only differentiating factor between the two devices is the width of tunnel barrier, W, which is a function of gate voltage, V_g. We collect all the common terms between the two devices in a constant term denoted by, α (Eqn. 2). The derivative of $\log_{10}T(E)$ with respect to gate voltage determines the steepness of I_D-V_{GS} curve, i.e. SS.

$$T(E) \approx e^{-2\int_{x_o}^{W} k(x)dx} = e^{-2\int_0^W \frac{\sqrt{2m}}{\hbar}\left[U_0\left(1-\frac{x}{W}\right)-E\right]^{1/2} dx} \quad (1)$$

$$T(E) \approx e^{-\left[\frac{4\sqrt{2m}}{3\hbar}\left(\frac{W}{U_0}\right)(U_0-E)^{3/2}\right]} \approx e^{-\left[\alpha . W(V_g)\right]} \quad (2)$$

$$\frac{dT(E)}{dV_g} \approx -\alpha e^{-\left[\alpha W(V_g)\right]} . \frac{dW(V_g)}{dV_g} \approx -\alpha . T(E) . \frac{dW(V_g)}{dV_g} \quad (3)$$

$$SS^{-1} = \frac{d[\log_{10}(I_d)]}{dV_g} \propto \frac{d[\log_{10}(T(E))]}{dV_g} \approx -\alpha . \frac{dW(V_g)}{dV_g} \quad (4)$$

Eqn. 4 shows that SS is inversely proportional to rate of change of tunnel barrier width with respect to gate voltage. As the tunneling width changes on both sides of the intrinsic-InAs channel barrier for underlapped device, we see a greater decrease in its tunneling barrier width compared to non-underlapped device for the same increase in gate voltage. So the following relationship holds true.

$$\left|\frac{dW(V_g)}{dV_g}\right|_{underlapped} > \left|\frac{dW(V_g)}{dV_g}\right|_{non-underlapped} \quad (5)$$

As SS is inversely proportional to rate of decrease of tunneling barrier width with respect to applied voltage (Eqn. 4), SS of the underlapped device is lower than that of conventional non-underlapped TFET.

B. Source-underlapped TFETs v/s Si-FinFETs

To compare our optimized TFET with Si FinFETs, the gate-workfunctions for the n- and p-type devices were adjusted to obtain symmetrical transfer characteristics (Fig. 6). The exact values are listed in Table.I. n/p-FinFET shows an I_{OFF} of around 100nA/μm and I_{ON} of around 1mA/μm for a gate voltage swing of 0.5V. In comparison, n/p- type TFET shows ~100x lower I_{OFF} of 3nA/μm, but a significantly lower I_{ON} of ~250μA/μm at V_{DD}=0.5V. The TFETs show low SS in the range of 20-25 mV/dec and sub-60 mV/dec SS for several orders of current magnitudes.

At a near-threshold voltage of 0.25V, TFET and FinFET have equal drain current. However, for the same on-current at V_{DD}=0.25V, TFET shows much lower off-currents, thereby making it a potential candidate for near-threshold and ultra-low power applications.

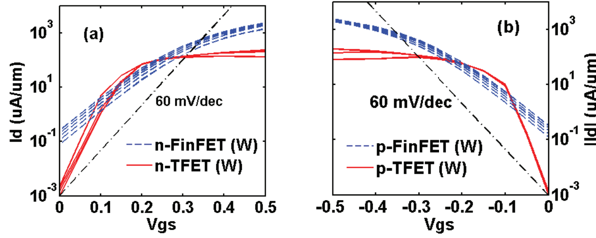

Fig.6. I_D vs V_{GS} for (a) n-TFET and n-FinFET (b) p-TFET and p-FinFET for varying V_{DS}. TFETs yield sub-60 mV/dec SS for 3-4 orders of drain current magnitude. At Vgs=0.25V (near-threshold voltage), TFETs and FinFETs show approximately same on-current.

V. CAPACITANCE VOLTAGE CHARACTERISTICS

Device capacitances play an important role in determining performance together with on-current. The capacitance versus voltage characteristics for Si n-FinFET and GaSb-InAs n-TFET at two different values of drain-source bias are shown in Fig. 7(a) and (b). In FinFETs, both C_{gs} and C_{gd} contribute equally toward inducing charge within the channel in the linear region whereas C_{gd} becomes negligible in saturation region due to higher potential barrier between the channel and drain. On the other hand, for TFETs, the gate-to-drain capacitance (C_{gd}) reflects the entire gate capacitance [17] and the gate-to-source capacitance (C_{gs}) remains very small due to the presence of source-side tunnel barrier. As the gate voltage is increased, C_{gd} increases due to the reduction in channel-to-drain side potential barrier and resulting inflow of charge. The gate capacitance in III-V based TFETs is much lower than Si FinFETs, especially below near-threshold voltages, due to the low density of states in III-V materials. This results in reduced delay for TFET based logic circuits when operating at near-threshold voltages in spite of their lower average drive currents.

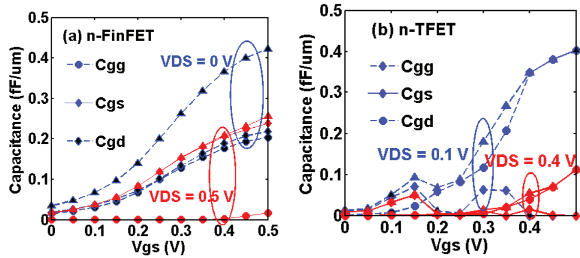

Fig.7. C-V characteristics for (a) n-FinFET and (b)n-TFET.

To estimate the improvement in the delay and the total energy achievable with TFETs, we use a 6-stage inverter chain as a benchmark circuit in the following section.

VI. INVERTER CHAIN ENERGY AND DELAY

To evaluate the circuit-level metrics of the heterojunction n- and p-type TFET devices discussed in Section III, a loaded TFET based 6-stage inverter chain is implemented and compared with an inverter chain implemented entirely using FinFETs. The interconnection of n- and p-type TFETs in each constituent inverter is shown in Fig.8. All the devices are minimum sized, i.e. the reference device structure described in Section III. Corresponding layouts of inverters implemented using FinFETs and TFETs are shown in Fig.9.

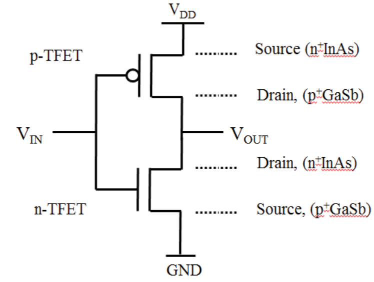

Fig.8. Inverter schematic using TFETs. Tunneling occurs near the source region for both TFETs.

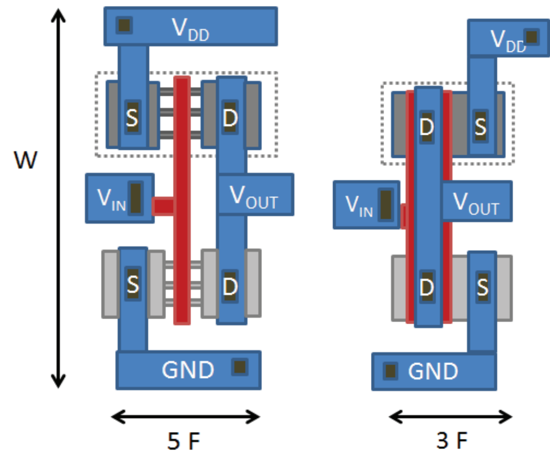

Fig.9. (a) FinFET (b) Vertical TFET inverter layout. F is the minimum feature size.

Here, ‘F’ is the minimum feature size. The vertical TFETs use gates on the sides which can be contacted outside the active region. Hence, the contacted gate area can be reduced thereby resulting in ~40% density gain over lateral devices [18].

To account for the gate parasitics, a fanout of 4 was considered at each stage. A logic activity factor of 10% is considered to represent switching activity realistically. The delay v/s supply voltage curve for these 6-stage inverter chains is shown in Fig. 10(a). At high V_{DD}, due to the low on-current of TFET, a TFET-based inverter chain cannot achieve as high performance as FinFET-based logic. However, for lower supply voltage targets, the TFET-based logic shows higher performance than FinFET-based logic due to its lower parasitic capacitance. In addition, the total energy consumption which includes the leakage energy and dynamic energy, shown in Fig. 10(b) is also low due to TFET’s ~100x lower standby leakage currents. While the reduction in supply voltage and capacitances causes the dynamic energy to improve in both FinFETs and TFETs, the leakage energy in TFET-based logic does not rise as severely as in FinFET-based logic (Fig. 11).

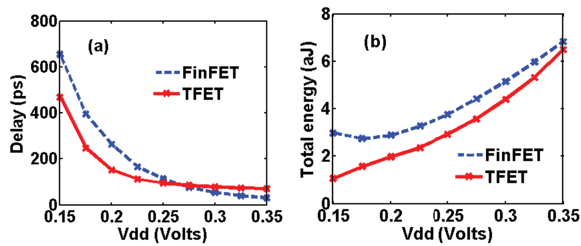

Fig.10. (a) Delay v/s supply voltage (b) Total energy v/s supply voltage for 6-stage inverter chain implemented using FinFETs (dashed line) and TFETs (solid line).

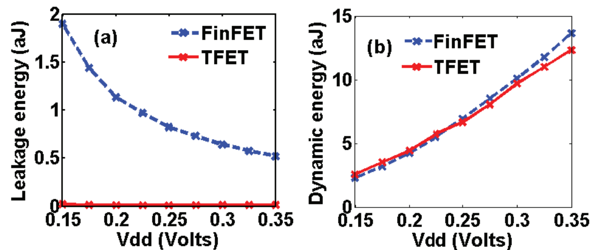

Fig.11. (a) Leakage energy v/s supply voltage (b) Switching energy v/s supply voltage for 6-stage inverter chain implemented using FinFETs (dashed line) and TFETs (solid line).

From the above analysis, it follows that TFETs would be good candidates for ultra-low voltage applications (or near-threshold voltage applications) which require medium-throughput but with ultra-low power consumption. To estimate the energy and performance metrics of systems built using TFETs and FinFETs in the presence of interconnect delay, we consider a LEON3 SPARC processor in the next section.

VII. System Level Evaluation of LEON3 Processor

Delay due to on-chip interconnections has become a critical factor for high performance designs in recent years. With devices scaling down into sub-20nm regime, wire resistance R and wire capacitance C have increased and hence, wire delays are significant. To assess the benefits of TFETs at scaled nodes in a realistic manner, in this section, we evaluate the performance of a TFET-based LEON3 processor and compare it with FinFET-based processor in the presence of interconnects modelled as distributed RC wire-loads.

The values for wire R and C per unit length were extracted from the analytical interconnect model of CACTI cache simulator [19] which models RC based wires up 32nm technology node. Beginning with the projected R and C, multiple wire-load model sets were generated by scaling the R and C. The exact RC values, for varying wire-load conditions, used in this work are listed in Table II. For example, for device structures described in Section III, assuming Copper interconnect, the resistance for FinFET is R=73Ω/μm, while for TFET, R=44Ω/μm. For a gate pitch of ~40 nm for vertical TFETs, the resistance per fanout would be 1.76Ω.

TABLE II
Wire Load Models

Device	Resistance per fanout (Ω)		Capacitance per fanout (fF)	
	FinFET	TFET	FinFET	TFET
WL1	2.92	1.76	0.011	0.011
WL2	5.84	3.52	0.022	0.022
WL3	11.68	7.04	0.044	0.044
WL4	23.36	14.08	0.088	0.088
WL5	46.72	28.16	0.176	0.176

The above wire-load models were used to synthesize LEON3 processor at a near-threshold V_{DD}=0.25V using Synopsys Design Compiler. The cell libraries needed for the synthesis included an inverter, 2 input NAND gate, 2 input NOR gate and a transmission gate based positive edge triggered D flip-flop. SPICE compatible compact lookup table models of TFETs and FinFETs were used to describe these gates and D flip-flop in the form of a SPICE netlist. Using Cadence Encounter Library Characterizer, these gates and the D flip-flop were characterized for power and timing characteristics by applying various input slew and load conditions. Due to non-availability of layouts for these cells, we do not consider the exact area information. Hence, the synthesis tool optimizes only for the delay and power while ignoring area constraints.

The maximum attainable frequency of operation, as reported by the synthesis tool, for the LEON3 processor is shown in Fig. 12. The wire load was varied for each new synthesis. It is observed that with no wire load or at very small wire loads, when the gate parasitics entirely dominate the interconnect parasitics, LEON3 realized using FinFETs can deliver higher performance than when realized using TFETs. When the gate parasitics become comparable to interconnect parasitics (WL1-WL4), TFETs turn out to be a better choice in terms of performance for realizing large circuits. Under heavy interconnect dominated situations (WL5), FinFETs are preferable for achieving high performance primarily because of their higher average drive currents.

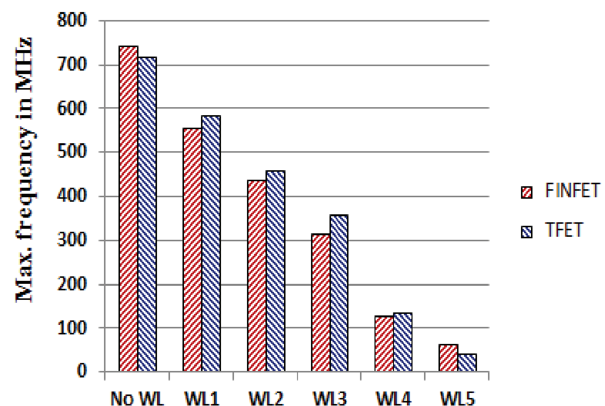

Fig.12. Maximum operable frequency of LeonSPARC for varying interconnect RC values listed in Table II.

The total power consumption of the LEON3 processor, as reported by the synthesis tool, for the various TFET and FinFET realizations with varying interconnect parasitics is compared in Fig.13.

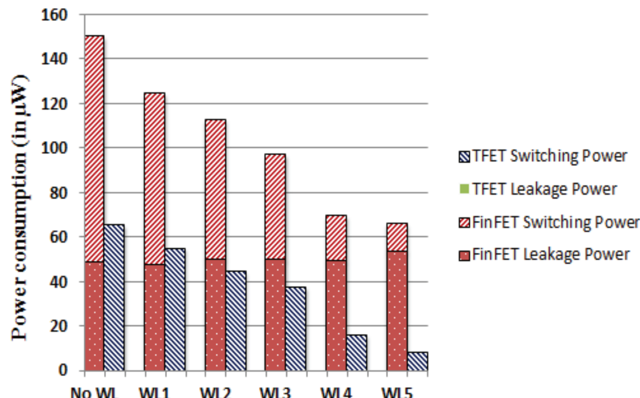

Fig.13. Power consumption of LEON3 processor realized using TFETs and FinFETs under varying interconnect parasitics.

The LEON3 processor realized using TFETs operates at much lower power (>50%) than that realized using FinFETs for all load conditions. The leakage power accounts for almost 50% of the total power consumption in FinFET-based realization. In contrast, the LEON3 processor realized using TFETs shows nearly 50% total power reduction primarily because of negligible leakage current of TFETs. The switching power dissipation is given by $C_L V_{DD}^2.f$, where f is the frequency of operation. As the interconnect parasitics increase, the maximum frequency at which the processor can operate reduces. Even though the wire load capacitance increases, this reduction in operating frequency causes the active power dissipation to fall drastically. On the other hand, leakage power being independent of the operating frequency remains nearly constant and starts to dominate the total power consumption in FinFETs with increasing interconnect parasitics.

VIII. Conclusion

A double-gate vertical n-type and p-type underlapped TFETs based on heterostructure GaSb-InAs, compatible with digital-circuit implementation, were compared with symmetrically underlapped FinFETs, at sub-10 nm gate lengths for near-threshold logic operation. An investigation of TFET-based 6-stage inverter chain shows that TFETs can deliver a better performance at sub-threshold voltages (≤0.25 V) while operating at ~100x lower standby power. A detailed circuit assessment of these devices was carried out at near-threshold voltages by synthesizing a LEON3 processor under varying interconnect scenarios. At near-threshold voltages and in the presence of moderate interconnect parasitics, TFET implementations were found to be preferable because of their ability to deliver similar performance as FinFETs while consuming nearly 50% lower power. As a result, GaSb-InAs TFETs appear to be a good choice for future ultra-low power applications since they enable a continuation of device scaling. At the same time, they provide additional benefits in power savings while delivering the same performance as Si FinFETs at near-threshold voltages.

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