Empirical Modelling of FDSOI CMOS Inverter for Signal/Power Integrity Simulation

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***Abstract*—This paper presents a multiport empirical model based on artificial neural network for I/O memory interface (e.g. inverter) designed based on fully depleted silicon on isolator (FDSOI) CMOS 28 nm process for signal and power integrity assessments. The analog mixed-signal identification signals that carry the information about the I/O interface's nonlinear dynamic behavior are recorded from large signal simulation setup. The model's functions are extracted based on a nonlinear optimization algorithm and then implemented in Simulink software. The performance of the resulted model is validated in typical power and ground switching noise scenario. The developed empirical model accurately predicts the timing signal waveforms at the power, ground, and at the output port.**

Keywords—FDSOI CMOS inverter; large signal multiport model; signal and power integrity; transient analysis;

I. INTRODUCTION

The characterization and modeling of high-speed I/O memory interfaces designed based on fully depleted silicon on insulator (FDSOI) transistors for signal and power integrity (SPI) is the key aspect to successfully design the future high-speed (high-frequency) analog/mixed-signal (AMS) devices in system-on-chip architecture [1]. In fact, the FDSOI transistor technology is considered as one of the best candidate for the short channel effect control and leakage current reduction in future sub 28nm CMOS generations to increase the switching speed and reduce the power dissipation of the I/O interfaces previously designed based on bulk MOSFET transistor [2-4].

However, the standard bulk device equations used in computer aided design (CAD) tools are not valid for describing the mechanism affecting the dc current-voltage (I-V) and the capacitance-voltage (C-V) characteristics which are typical for FDSOI structure. Moreover, SPI can be assessed based on the accurate but impractical transistor level (TL) model (e.g. BSIMSOI [3]), that can contain hundreds of physical parameters required for each single transistor [3], which slows down the simulation and reveals its intellectual property. Therefore, the progress in empirical modeling is well behind the success of the SPI assessment in order to fast and accurately simulate the AMS I/O interface and to cope with their design technology advancements [2], [5].

SPI is assessed by predicting the high-speed signals propagating on the printed circuit board that links various I/O interface pins while the power and ground (PG) rails fluctuate due to the parasitic resistance (*IR* drop) and inductances (ΔI-noise) of the packages pin and bond wires as shown in Fig. 1.

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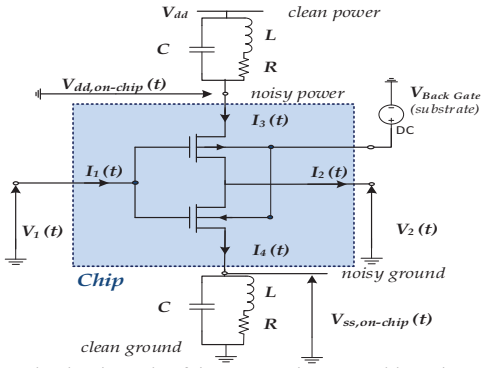

Fig. 1. A circuit schematic of the RLC package parasitic at the power and ground nodes of an FDSOI CMOS inverter.

This results in an extra delays in the transmitted signals to the active receivers or causes logic errors for the quiet ones [1].

Empirical models can be classified into two categories. Firstly, the equivalent circuit approaches such as IBIS (input/output buffers information specification) [6] and CSM (current source model) [7] models that assume discrete constant power supply voltage, V_3, (i.e. typical-minimum-maximum data) which limit their prediction accuracy due to the *Ldi/dt* spikes. In fact, the IBIS and CSM characterize only the output currents, therefore, they may fail to accurately model the I/O device for SPI analysis due to the dynamic and continuous PG voltage fluctuations caused by the on-chip package under simultaneous switching noise scenarios [1]. An equivalent circuit extension and lookup table implementation for CSM is presented in [7]. This modeling approach simplifies the model formulation and extract the model by only a dc simulation [7]. Secondly, the parametric approaches such as Mpilog [8] or I-Q [9] models which share the same piece-wise model formulation of IBIS (i.e. $I_2(t) = w_1(t) \times f_1(V_2(t)) + w_2(t) \times f_2(V_2(t))$). Mpilog is a curve fitting technique based on artificial neural networks (ANNs) that extends the IBIS model to cope with technology advancement and SPI prediction. However, Mpilog only provides an extension of IBIS model for power supply, V_3, variation in the driver's pull-up (PU) function $f_1(V_2(t), V_3(t))$, and pull-down (PD) function $f_2(V_2(t), V_3(t))$, and on the timing switching functions, $w_1(t)$ and $w_2(t)$, without characterizing and modeling the ground bouncing [7-9].

In this work, the proposed empirical model captures the PG bouncing by extending the two port model formulation to single piece multiport for SPI prediction of an output interface

(e.g. driver or inverter gate) designed based on 28 nm FDSOI CMOS process. The variation of the PG currents (I_3 and I_4) are modeled as nonlinear function of the applied voltages at the all the device terminals. The model also copes with the advancement in the new technology by considering the changes caused by the FDSOI transistors on the static I-V curves and accurately modeling the nonlinear displacement currents of the SOI architecture caused by the nonlinear capacitive (C-V) effects. The remaining of this paper is organized as follows. Section II analyzes the device electrical properties in order to incorporate this knowledge in the model formulation. Section III details the multiport characterization setup and the empirical model extraction. Section VI describes the validation setup for the evaluation of the model performance in predicting the PG bouncing. Finally, conclusions are presented in Section V.

II. System Analysis and Model Formulation

The conduction current of the FDSOI CMOS inverter is characterized by the nonlinear relationship between I_{ds} *vs.* V_{ds} and I_{ds} *vs.* V_{gs} which are extracted by a dc voltage sweep while recording the respective current. In addition, the capacitances in the FDSOI structure nonlinearly depend on the applied voltages which define the device operation regime (i.e. cut off, linear, and saturation) [2], [5]. In addition, there is an overlap-ping between these capacitances which usually model the input, output, and PG capacitances as well as the coupling between these port terminals. The identification of these lumped capacitances requires a separate time consuming step and complex three dimensional nonlinear C-V models. For these reasons, we opt to include the inverter's displacement currents in the general formulation of the PG currents.

In order to incorporate these effects, the two port model is extended to multiport to capture the PG voltages fluctuation, V_3 and V_4, respectively. Therefore, a relation is drawn between driver PG currents (I_3 and I_4) and PG voltages, V_3 and V_4, input and output voltages V_1 and V_2, respectively. The ground voltage, V_4, is used as a reference (e.g. $V_{14} = V_1 - V_4$, $V_{24} = V_2 - V_4$, and $V_{34} = V_3 - V_4$) while the input current, $I_1(t)$, and the backgate current are neglected.

$$\begin{cases} I_3(t) = F_3(\theta_3, X_3(q)) \\ I_4(t) = F_4(\theta_4, X_4(q)) \end{cases} \quad (1)$$

The $F_i(.), i = 3,4$ functions capture both the conduction caused by slow dc variation and the displacement current caused by the fast variation of the independent voltage variables. For each function, the fitting parameters θ_i is defined. The model representation is shown in Fig. 2 where the output current is computed by $I_2(t) = I_3(t) - I_4(t)$ and the regressor vector $X_l(q)$ is defined as:

$$X_l(q) = \begin{bmatrix} V_{14}(t), \dots, V_{14}(t - qT_s) \\ V_{24}(t), \dots, V_{24}(t - qT_s) \\ V_{34}(t), \dots, V_{34}(t - qT_s) \end{bmatrix}; l = 3,4 \quad (2)$$

where T_s is the sampling time. The regressor vector could be nonlinear or expanded as polynomial [5]. The selection of dynamic order, q, depends on the dynamic of the output

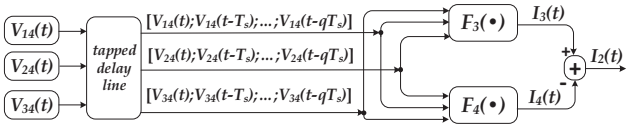

Fig. 2. Block diagram of the empirical ANN-based model representation.

interface/driver circuit to be modeled. Equation (2) highlights that the selected model is direct (e.g. non-recursive) which avoids the instability issues that can be triggered by the nonlinear recursive model formulation.

The empirical modelling task consists in identifying the nonlinear dynamic trajectory of the FDSOI CMOS inverter's behavior given a time series of an observable current and voltage signals. This is achieved by determining the dynamic order, q, and the number basis functions (BF) approximating $F_i(.)$. Since the driver circuit manifests an inherent capacitive dynamic effect, the model in continuous time-domain is formulated as, $I_i(t) = F_i(V(t), dV(t)/dt)$, which can be converted in discrete time-domain, $I_i(t) = F_i(V(t), V(t - T_s))$ by considering the discretization of the derivative based on backward Euler approximation $C_i\, dV(t)/dt \cong C_i/T_s\,(V(t) - V(t - T_s))$. Therefore, this prior knowledge analysis of the driver's internal circuitry yields a low dynamic order (i.e. $q = 1$) model [8]. Moreover, the type (i.e. Gaussian or hyperbolic tangent) and number of BF used to approximate the static PU and PD I-V nonlinearities depend on FDSOI short channel effects such as channel length modulation, velocity saturation and drain induced barrier lowering.

III. Device Charaterization and Model Extraction

A. Characterization Setup

The characterization setup consists of designing excitation signals that reflect the AMS nonlinear static and dynamic behaviors of the inverter for wide operation range of amplitude and frequency. The large signal voltages are designed in order to reflect the usual device working conditions at all the device terminals as shown in Fig. 3. A high data rate input random bit sequence (e.g. trapezoidal waveform) with short rise/fall (t_r/t_f) time is used at the input port, $V_1(t)$. In addition, a high frequency sinusoidal signals that cover the voltage range of the pull-up and pull-down of the SOI MOSFET transistors used at the PG and output ports:

$$\begin{cases} V_2(t) = a_2 + a_{20} sin(2\pi f_2 t + \varphi_2) \\ V_3(t) = a_3 + a_{30} sin(2\pi f_3 t + \varphi_3) \\ V_4(t) = a_4 + a_{40} sin(2\pi f_4 t + \varphi_4) \end{cases} \quad (3)$$

where $a_2 = a_3 = 0.5 \times V_{dd}$, $a_4 = 0$, $a_{20} = 0.5 \times V_{dd} + \Delta_2$, and $a_{30} = a_{40} = \Delta_{34}$. The frequency f_2 is chosen to be 10% till 20% higher than the maximum frequency of in the input signal $V_1(t)$ (i.e. $f_2 = 1.2 \times 0.35/t_r$). The frequency f_3 and f_4 are *non-commensurate* with f_2 ($f_3/f_2 \notin \mathbb{Q}$ and $f_4/f_2 \notin \mathbb{Q}$) and higher than f_2. The overvoltage margin, Δ_2 and Δ_{34} are chosen to account for the effects of signal overshoot and undershoot. The sampling time is determined in order to avoid antialiasing while considering a representative and small data set of the training sequences for the ANNs to reduce the model identification complexity (e.g. $T_s = 0.1 \cdot \min(t_r, t_f)$).

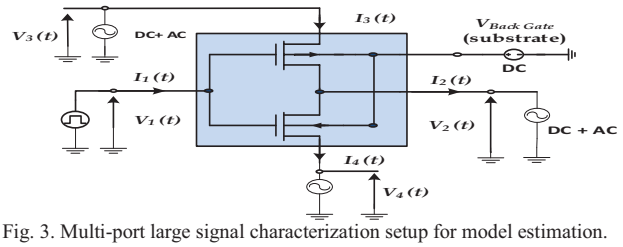

Fig. 3. Multi-port large signal characterization setup for model estimation.

TABLE I
DESCRIPTION OF THE CHARACTERIZATION SETUP PARAMETERS.

Parameters	Value	Parameters	Value
Data rate ($V_1(t)$)	0.8 Gbps	V_{dd}	1.5 V
$t_r = t_f$	400 ps	Δ_2	0.35 V
f_2	1.14 GHz	Δ_{34}	0 V
f_3	1.37 GHz	φ_2=$\varphi_3 = \varphi_4$	0 º
f_4	1.49 GHz	$V_{\text{Back Gate}}$	0 V

The phases, φ_2, φ_3, and φ_4 can be arbitrarily selected to achieve a better amplitude coverage of the $V_2(t)$ *vs.* $V_1(t)$, as shown in Fig. 4, $V_3(t)$ *vs.* $V_2(t)$, and $V_4(t)$ *vs.* $V_2(t)$. The nonlinear static and looping capacitive effect of the ground current $I_4(t)$ as a function of the voltage $V_{24}(t)$ is illustrated in Fig. 5. The parameters describing the simulation setup for recording the identification time series voltages and currents are described in Table I.

B. Model Extraction

As described in Section II, the dynamic order has been deduced (i.e. $q = 1$) which enables the four ports model to handle an FDSOI CMOS circuit described by a first-order nonlinear ordinary differential equation. After that, the two single-valued multivariate model's functions, $F_3(.)$ and $F_4(.)$ are described by feed-forward ANNs structure from MATLAB ANNs toolbox. The voltage variables and their delayed versions are the inputs to the ANNs which their parameters were extracted using the Levenberg–Marquard (LM) nonlinear optimization algorithm by minimizing the mean squared errors (MSE) between the large signal model's PG output currents and the desired output current of each function [10]. The extraction procedure for the same direct model structure may require multiple (e.g. 4 times) runs of the LM algorithm for different θ_i initialization while adjusting the number BF and verifying the network generalization capabilities by means of the validation I/O signals. This identification step should also consider the model's overfitting and the convergence to local minima in order to generate a model that balances the tradeoff between running and identification complexities.

The estimated model functions, $F_3(.)$ and $F_4(.)$, turn out to be decomposed of 7 and 6 hyperbolic tangent BF, respectively. The total number of parameters of the complete empirical model is 107 as described in Table II with other metrics evaluating the identification model's complexity. Since the FDSOI transistor described by BSIM3SOI model requires 126 parameters [3], a reduction of the number of parameters by 57.53 % is achieved which consequently lead to a reduction of the floating point operations in such modelling problem where only two FDSOI MOSFET are used.

TABLE II
PERFORMANCE OF EMPIRICAL MODEL'S FUNCTIONS IDENTIFICATION.

Model's Functions	Number of BFs	Number of Parameters	Training		MSE
			Epochs	Time	
$F_3(.)$	7	58	100	11s	3.6e-4
$F_4(.)$	6	49	100	11s	4.0e-6

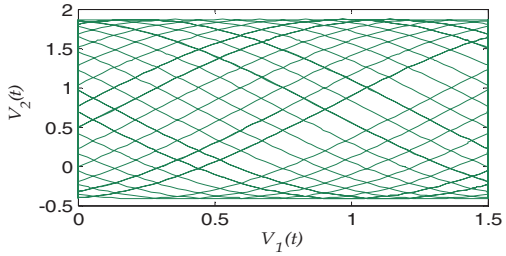

Fig. 4. Coverage of the plane $V_2(t)$ *vs.* $V_1(t)$.

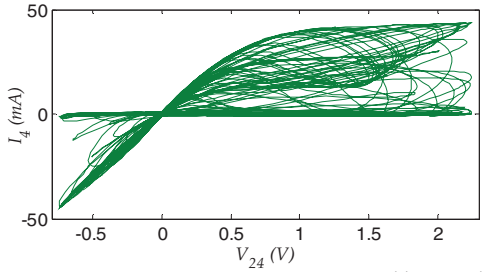

Fig. 5. Hysteresis effect of the ground current $I_4(t)$ *vs.* $V_{24}(t)$.

IV. MODEL CORRELATION AND VALIDATION

The model described by (1) and (2) was implemented in Simulink time domain solver. A realistic validation setup composed by the modeled FDSOI CMOS inverter, driven by 1 Gbps input bit pattern "010110100" with t_r=t_f=300 ps while it is loaded by a parallel RC circuit emulating the receiver impedance and an RLC circuit at the PG ports emulating the on-chip package impedance, as shown in Fig. 6 is used to compare the prediction results of the PG bouncing and the output signals of the empirical and TL models. The simulation is performed considering the parameters shown in Table III.

Figs. 7 and 8 show good agreement between the PG currents, $I_3(t)$, $I_4(t)$ and voltages, $V_3(t)$, $V_4(t)$, respectively, of the implemented empirical model and the reference FDSOI inverter simulated using BSIM SOI model in Cadence using HSPICE. In addition, Fig. 9 illustrates the accurate prediction of the current and voltage at the output port which confirms the good accuracy and the correctness of the model formulation, characterization, and extraction steps. We quantify the prediction accuracy by means of the normalized mean squared error (NMSE) [9]. The NMSE for I_3 and I_4 is -25.93 dB and -23. 50 dB, respectively. The NMSE for V_3, V_4, and V_2 is -35.32 dB, -18dB, and -29.44 dB, respectively.

TABLE III
DESCRIPTION OF THE PARAMETERS OF THE VALIDATION SETUP OF FIG.6.

Parameters	Value	Parameters	Value
C	0.01 pF	R_{L}	200 Ω
R	10 Ω	C_{L}	5 pF
L	4 nH	$V_{\text{Back Gate}}$	0 V

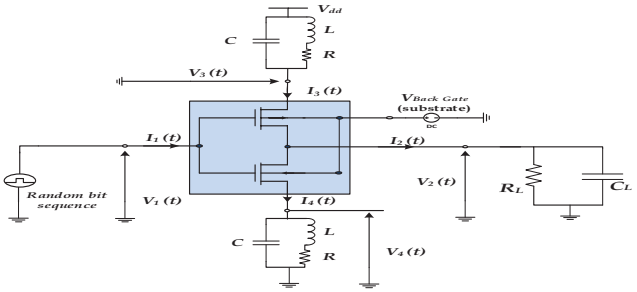

Fig. 6. Validation setup for FDSOI CMOS 28 nm inverter/driver.

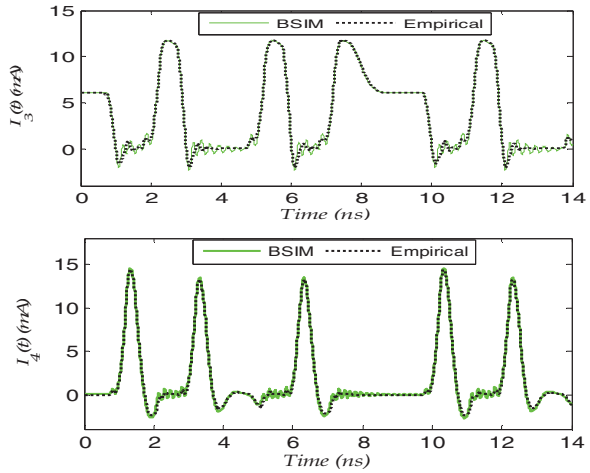

Fig.7. Comparison between model's prediction the power supply current $I_3(t)$ and ground current $I_4(t)$ of the validation setup of Fig. 6.

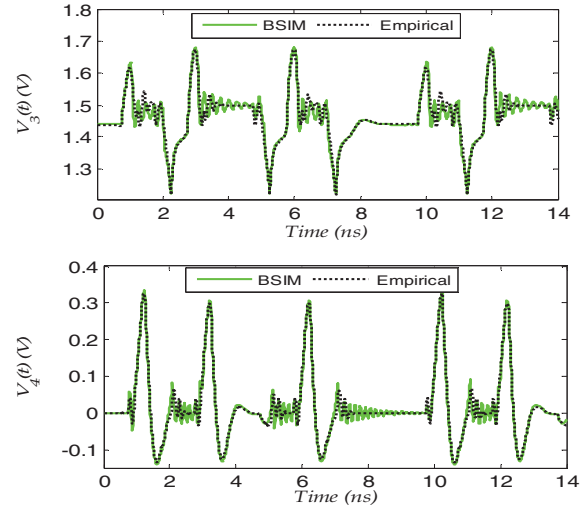

Fig.8. Comparison between model's prediction of the power supply voltage $V_3(t)$ and ground voltage $V_4(t)$ of the validation setup of Fig. 6.

V. Conclusion

This paper has presented a large signal multiport time domain model formulation, characterization, and extraction. The validation setup has confirmed that the proposed modelling procedure has accurately captured the nonlinear dynamic behavior of an inverter gate designed based on 28nm FDSOI CMOS process in predicting the PG switching *IR* drop

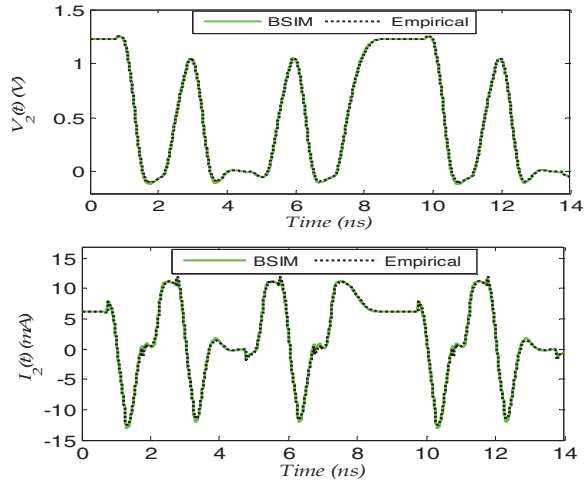

Fig. 9. Comparison between the output voltage, $V_2(t)$, and current, $I_2(t)$, waveforms of the reference and the empirical models.

and ΔI-noise. This modelling procedure can be extended to large circuit drivers with cascaded inverters or slew rate control in order to predict simultaneous switching output noise scenario where the simulation speed up is more noticeable.

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