Detection of Asymmetric Aging-Critical Voltage Conditions in Analog Power-Down Mode

Michael Zwerger, Helmut Graeb
Institute for Electronic Design Automation
Technische Universität München, Munich, Germany

***Abstract*—In this work, a new verification method for the power-down mode of analog circuit blocks is presented. In power-down mode, matched transistors can be stressed with asymmetric voltages. This will cause time-dependent mismatch due to transistor aging. In order to avoid reliability problems, a new method for automatic detection of asymmetric power-down stress conditions is presented. Therefore, power-down voltage-matching rules are formulated. The method combines structural analysis and voltage propagation. Experimental results demonstrate the efficiency and effectiveness of the approach.**

I. Introduction

Power efficiency and reliability are important requirements for modern chips [1], [2]. These design goals have to be achieved in short development cycles due to the high competitive pressure in the microelectronics industry and in a scenario where leakage currents and aging effects are becoming more and more significant with shrinking technology nodes [1], [3], [4], [5]. In order to increase power-efficiency, most modern chips implement power-management features, i.e., they are equipped with power-down modes. In this work, we are focusing on the power-down mode of analog circuit blocks [6], [7]. For analog circuits, matching is an important design principle [8], [9]. Matched devices are required to be as identical as possible, or alternatively, the ratios of device parameters, like e.g., the transistor widths, need to have an exact value.

In power-down mode, transistors are exposed to different voltages than during normal operation. This can cause negative aging effects like HCI or NBTI [3], [10]. Therefore, the matching can be degraded in power-down mode [11], [12]. This can cause the circuit to fail when it is powered up again.

A lot of attention is paid to achieve good matching after manufacturing and in verifying that the negative effects of aging are minimized during normal operation. The commonly applied approaches are sizing rules for robustness [8], sophisticated layout structures [13] and comprehensive aging simulations [10]. However, less attention is paid on verifying that there are no reliability problems induced by the power-down mode.

In this work, a new method for detecting asymmetric voltage conditions in power-down mode that would degrade the matching is presented. The method can be used as part of a sign-off verification flow for analog circuit blocks.

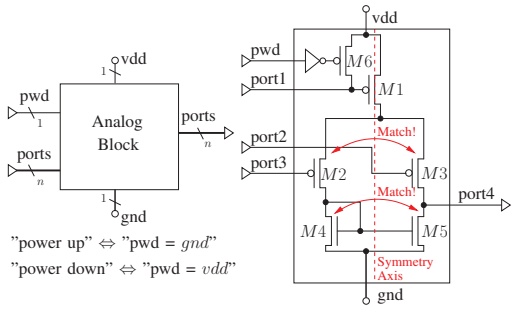

Fig. 1. Differential amplifier as example for an analog block

II. Power-Down Reliability Verification

In this section, the verification task is introduced using the example of the differential amplifier shown in Fig. 1 on the right. The differential stage has three input ports and one output port as well as a positive supply vdd and a ground gnd. The power-down mode is controlled by signal pwd.

During normal operation signal pwd is low, i.e., the voltage is gnd. Consequently, the gate of $M6$ is vdd, as it is connected via an inverter. Thus, $M6$ is not conducting and has no major influence on the circuit. In power-down mode, the signal pwd is high, i.e., the voltage is vdd and the gate of $M6$ is gnd. Therefore, $M6$ is conducting and the gate of $M1$ is pulled to vdd. Consequently, the bias current through $M1$ is zero and no power is consumed.

The functionality of the given differential amplifier in normal operation mode relies on the fact that the transistors of the differential pair $M2$, $M3$ as well as the transistors of the current mirror $M4$, $M5$ are matched. This is illustrated by the red dotted symmetry axis in Fig. 1. In order to guarantee matching over the lifetime of a circuit, the matched transistors should be exposed to symmetric voltage conditions in power-down mode, as asymmetric stress will degrade the matching [12], [11], [3].

In this work, the verification is carried out for analog circuit blocks, like the one shown in Fig. 1 on the left. It is assumed that the circuit block has an arbitrary number of input and output ports. Furthermore, there must be one or more external signals controlling the power-down mode. For the sake of a clearer presentation, it is assumed that there is only one signal controlling one power-down mode. For multiple power-down modes, the method described in this work can be executed

978-3-9815370-4-8/DATE15/©2015 EDAA

repeatedly. We follow the convention that the power-down signal is called pwd and pwd = vdd means power-down or idle mode and pwd = gnd means power-up or normal operation mode. In power-down mode, internal nodes of the circuit can have a defined voltage near the positive supply or near the ground. This is denoted with voltages vdd and gnd, respectively. Nodes can also be floating. Floating nodes are nodes which have only high resistive connections to other nodes. This is denoted as $float$.

The task solved in this work is to detect asymmetric aging-critical voltage conditions that would degrade the matching. Matched pairs are automatically identified. Critical voltage conditions are automatically detected by checking a new set of voltage matching rules for the power-down mode.

III. State of the Art and Contributions

Due to the increased need for dynamic power-management, verification for low-power designs, including verification of power-down modes and verification of correct power-domain transitions, is a field that has gained increased importance [2], [5]. This can be seen by the fact that new tools for detecting issues like floating gates, static leakage, electrical overstress at thin-oxide devices or missing level shifters at the border between voltage domains are emerging [2], [14].

One approach for detecting the above mentioned problems would be to use excessive numerical simulation. The electrical behavior of a circuit can be simulated using spice and optimized fast spice simulators [15]. The aging effects can be investigated using aging simulators [10]. However, approaches based on numerical simulations are computationally expensive and, therefore, infeasible for large designs. The situation is aggravated if the circuit needs to be simulated for a large number of input vectors and power-down modes. Furthermore, defining suitable assertion rules is not straightforward. Additionally, simulation results are often not trustworthy for the power-down mode, as devices are operating in the sub threshold region, which is often not modeled accurately enough by the available device models [7].

In order to avoid the problems induced by simulation, state-of-the-art methods use static voltage propagation approaches in order to estimate the node voltages [6], [7], [4]. Furthermore, they perform topological checks by using pattern matching [4], specialized algorithms for structural analysis [8] or signal flow analysis [9]. Asymmetric stress conditions are, e.g., mentioned in [16] or [3]. None of the above mentioned methods is able to detect asymmetric stress conditions as the method described in the following does.

Compared to the state-of-the-art, this work makes the following new contributions:

- Automatic detection of asymmetric power-down stress conditions.
- Power-down voltage-matching rules.
- Enabling use of state-of-the-art structure recognition by automatic partitioning of the circuit in analog functional part and power-down part.

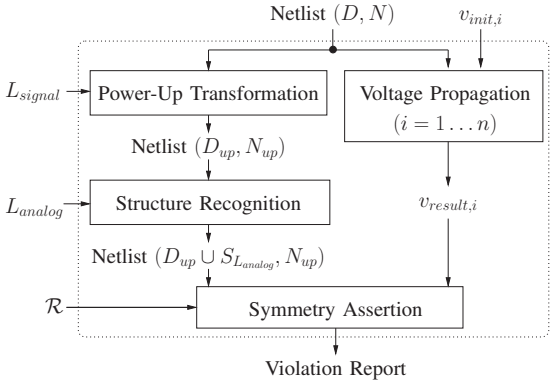

Fig. 2. Overview over the power-down reliability-verification method

IV. Power-Down Reliability Verification Algorithm

A. Overview

Fig. 2 shows the data flow of the algorithm. The method takes the circuit netlist as input. The netlist is denoted as (D, N), where D is the set of devices and N is the set of nets. The method combines structure recognition, e.g., [4], [8], [9] and static voltage propagation, e.g., [2], [7], [6] to solve the verification task.

In order to enable analog structure recognition by state-of-the-art algorithms, the netlist is transformed to a power-up representation of the circuit. Power-up transformation is described in section IV-D. During power-up transformation the parts of the circuit carrying the power-down signal to the power-down switches as well as the power-down switches themselves are identified and removed. For power-up transformation, structures like the inverter in Fig. 1 are recognized using a library L_{signal}. For example, in Fig. 1, the inverter connected to the gate of $M6$ is detected and then removed together with power-down switch $M6$. The resulting netlist is denoted as (D_{up}, N_{up}) and contains the analog functional part of the circuit. It is passed on to a structure recognition algorithm. Structure recognition takes a library L_{analog} as input. The recognized structures are denoted as $S_{L_{analog}}$. They are added to the netlist.

The internal node voltages of the circuit are estimated using voltage propagation. Voltage propagation takes the voltages at the external terminals of the circuit block as input. The voltages are denoted as $v_{init,i}$. The input vectors can be chosen in the following ways:

- Full enumeration, if the analog block needs to be fully isolated from the circuitry connected to the ports.
- Selection of all combinations that were encountered during system level simulation.
- Manual selection, if the combinations are known or given as specification.

For each input vector $v_{init,i}$, voltage propagation is performed. The results are denoted as $v_{result,i}$ and contain also the voltages of internal nets. For each result, the symmetry rules

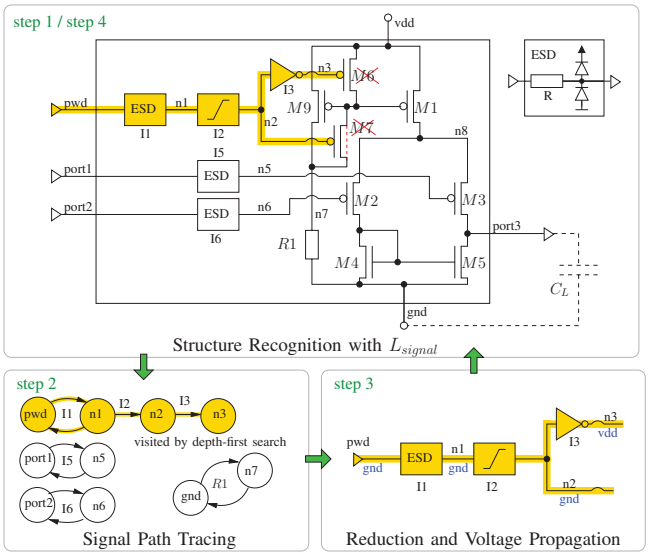

Fig. 3. Power-up transformation

$\mathcal{R}$ (see IV-E) are asserted. The violations are collected in a violation report.

B. Structure Recognition

For the proposed method, a structure identification method is required. Structure recognition takes a netlist (D, N) as input. During recognition, structures are identified according to a library L. The set of structures recognized with library L is denoted as S_L. For the proposed method, two libraries are required: L_{analog} and L_{signal}. L_{analog} should contain analog matched pairs like differential pairs and current mirrors, e.g., [8] and [9]. $L_{digital}$ should contain all the functional blocks, that form the power-down part. Therefore, structures like e.g., inverters, nand and nor gates, level shifters and pass-gates need to be detected. For the experimental results an algorithm based on [8] and [9] was used.

C. Voltage Propagation

In order to calculate internal node voltages in power-down mode efficiently, a voltage propagation method is required. For the experimental results, an algorithm based on [7] was used. Voltage propagation takes initial voltages as input. The set of voltage levels is denoted as V. The set of nets with initial voltages is called N_{init}. Initial voltages are, e.g., assigned to the supplies, the pwd signal and the ports. The initial voltages corresponding to the i-th input vector are described by a function $v_{init,i}(n)$ which assigns a voltage out of V to each net in N_{init}. The result of voltage propagation for the i-th input vector is a function $v_{result,i}(n)$ which assigns a voltage out of V to each net in N. The functions $v_{init,i}(n)$ and $v_{result,i}(n)$ are used in Fig. 2.

D. Power-Up Transformation

In order to enable detection of all structures by state-of-the-art methods the initial netlist needs to be transformed to the power-up state. Therefore, power-down switches, e.g., $M6$ and $M7$ in Fig. 3 need to be removed. Fig. 3 illustrates the principle of power-up transformation. In order to identify all power-down switches, the pwd signal needs to be traced from the external terminal to the gate of each power-down switch. This procedure is described in the following: First, all structures of the power-down part like, e.g., inverters, nand/nor gates, pass-gates and level-shifters need to be identified by structure recognition using the library L_{signal} (Fig. 3, step 1). Secondly, a graph is created based on the detected structures and a depth-first search (DFS) [17] on the resulting graph is carried out starting at the external pwd terminal (Fig. 3, step 2). All components and nets visited during DFS belong to the power-down part. In Fig. 3, they are highlighted in yellow. Thirdly, voltage propagation is carried out on the identified power-down part of the circuit in order to determine the voltages of the nets (Fig. 3, step 3). The resulting voltages are annotated in blue. Based on those voltages, all transistors with a gate connected to a signal net are replaced by a short or open circuit (Fig. 3, step 4). In our example, transistor $M6$ is replaced by an open circuit and $M7$ is replaced by a short circuit. The transformation makes the current mirror $M9/M1$ detectable with L_{analog}.

E. Symmetry Rules

In the following, voltage matching rules to avoid asymmetric aging in power-down mode are introduced. A matching rule is a set of pins which should have equal voltages in power-down mode. This set of pins is formulated in dependence of L_{analog}, such that for each instance of a recognized structure the rule can be asserted.

During power-up transformation nets are shortened while removing power-down switches from the original netlist (D, N). It follows, that there is no bijective mapping between the original nets N and the transformed nets N_{up}. Due to this fact, a formulation of matching rules in terms of nets of the structures in L_{analog} is not possible. Therefore, we suggest to formulate the rules in terms of transistor pins. It must be ensured that each pin of the transistors that form a matched pair is uniquely addressed. For achieving this, pin addresses are used in our implementation. A matching rule $R_{t,i}$ for a structure type t is a set of pin addresses. All pins in the set are required to have the same voltage in power-down mode, in order to enforce symmetric voltages. This is denoted as *matching rule*. Alternatively, rules to enforce or forbid a specific voltage for a pin can be specified, e.g., enforce vdd for the gates of a PMOS differential pair in order to avoid NBTI. This is denoted as *voltage rule*. For each type t several rules $i = 1 \ldots n$, e.g., to match drain, source, gate and bulk pins, respectively, are specified. The rules for a type t are collected in set $\mathcal{R}_t$, i.e., $\mathcal{R}_t$ is a set of sets of pin addresses. The complete set of rules is $\mathcal{R}$. Fig. 2 shows that $\mathcal{R}$ is an input for symmetry assertion.

F. Symmetry Assertion

For each recognized structure of type t out of $S_{L_{analog}}$ the corresponding rules $R_{t,i}$ are asserted. For a matching rule,

TABLE I
VIOLATION REPORT FOR THE DIFFERENTIAL AMPLIFIER OF FIG. 3

Violation	Voltages (port1, port2)
dp ($M2.drain$, $M3.drain$)	all except (gnd, gnd)
dp ($M2.gate$, $M3.gate$)	all except (gnd, gnd) and (vdd, vdd)
scm ($M1.drain$, $M9.drain$)	all with port2 $\neq gnd$
scm ($M4.drain$, $M5.drain$)	all except (gnd, gnd)

it is asserted that the voltages at all the addressed pins are equal for all results of voltage propagation $v_{result,i}$, i.e., for all input vectors $v_{init,i}$. For a voltage rule, it is asserted that all the addressed pins have one of the specified voltages for all results of voltage propagation $v_{result,i}$, i.e., for all input vectors $v_{init,i}$. The result of an assertion is $pass$ or $fail$. All assertions with result $fail$ are reported in a violation report.

V. EXPERIMENTAL RESULTS

In the following, experimental results are presented for the differential amplifier shown in Fig. 3 and for an industrial circuit. The algorithms have been implemented in C++. The experiments have been carried out on a standard workstation with Intel(R) Core(TM) i7-4770 CPU running at 3.40 GHz. In order to reduce the influence of different load conditions of the workstation on the measured runtime, the program has been executed 10 times repeatedly. The resulting average runtime and standard deviation are given in the following.

A. Differential Amplifier

The differential amplifier of Fig. 3 has 30 devices and 19 nets. It was assumed that port3 is used to drive a capacitive load C_L. Thus, it was not included in N_{init}. It was assumed that the circuit block should be capable to handle any boundary condition on port1 and port2. For voltage propagation, the levels $V = \{gnd, float, vdd\}$ were used. Therefore, a total of 3^2 combinations for $v_{init,i}$ was analyzed. The result is shown in Table I. It can be seen that 4 violations are reported. In the left column the structure type t as well as the corresponding pins where the violation occurred is reported. Violations are reported for the differential pair (dp) $M2$/$M3$ and for the simple current mirrors (scm) $M1$/$M9$ and $M4$/$M5$. In the right column, the input vectors out of $v_{init,i}$ for which the violations occurred are described. The average runtime was 244 ms with a standard deviation of 10.8 ms.

The reported violations could be fixed by adding additional circuitry. The inputs port1 and port2 have been insulated from the gates of $M2$ and $M3$ with two pass gates. Two power-down switches have been added to pull both gates to vdd. Additionally net n8 and port3 were pulled to gnd. For the modified circuit, all voltage matching rules were fulfilled. Zero violations were reported.

B. Industrial Circuit

An industrial circuit used for our tests was an LVDS driver with 229 devices and 120 nets. The average runtime was 462 ms with a standard deviation of 66.2 ms. The industrial circuit is designed in a way that only differential pairs have matched power-down voltages. Therefore, we have relaxed the symmetry rules to only contain the rules for dp. Set N_{init} contained two ports. One port was a reference voltage, the other port a digital data signal. Four violations were reported. Two violations were due to differential amplifier inputs being connected to floating nodes. The other two violations were due to floating nodes inside an operational amplifier.

VI. CONCLUSION

In this work, the need to match voltages in power-down mode has been met by new voltage-matching rules and a new method for automatic verification of these rules. Voltages are estimated using static voltage propagation. In order to enable circuit analysis by state-of-the-art structure recognition, the circuit is partitioned into a power-down part and an analog functional part. Experimental results have demonstrated the efficiency and efficacy of the method. Even for a larger industrial analog block, the runtime was below one second. The presented method can be used as part of a sign-off verification flow for analog blocks. It provides the necessary tool support for designers to ensure reliability of the power-down mode.

ACKNOWLEDGEMENT

This work has been supported in part by a subcontract from Infineon Technologies AG, funded by the German Federal Ministry of Education and Research (BMBF) in the Project RELY under Grant No. 01M3091.

REFERENCES

[1] "ITRS Roadmap, 2013 Edition," *online: http://www.itrs.net*.
[2] M. Hogan, "Reduce Verification Complexity in Low/Multi-Power Designs," *Mentor Graphics White Paper, online: http://www.mentor.com*.
[3] E. Maricau and G. Gielen, "Transistor Aging-Induced Degradation of Analog Circuits: Impact Analysis and Design Guidelines," in *ESSCIRC*, Sep. 2011.
[4] J. Lescot *et al.*, "Static Low Power Verification at Transistor Level for SoC Design," in *ISLPED*, 2012.
[5] D. Medhat, "Power-Aware Verification in Low Power ICs," *Chip Design Magazine, online: http://chipdesignmag.com*, 2012.
[6] S. Blieck and E. Janssens, "Software Check for Power-Down Mode of Analog Circuits," in *ESSCIRC*, Sep. 1996.
[7] M. Zwerger *et al.*, "Verification of the Power-Down Mode of Analog Circuits by Structural Voltage Propagation," *Analog Integrated Circuits and Signal Processing*, Aug. 2013.
[8] T. Massier *et al.*, "The Sizing Rules Method for CMOS and Bipolar Analog Integrated Circuit Synthesis," *TCAD*, Dec. 2008.
[9] M. Eick *et al.*, "MARS: Matching-Driven Analog Sizing," *TCAD*, Aug 2012.
[10] "Virtuoso RelXpert Reliability Simulator User Guide," *Cadence MMSIM Product Documentation*, 2013.
[11] C. Michael *et al.*, "Mismatch Drift: A Reliability Issue for Analog MOS Circuits," in *Reliability Physics Symposium 1992. 30th Annual Proceedings., International*, March 1992.
[12] Y. Chen *et al.*, "Stress-Induced MOSFET Mismatch for Analog Circuits," in *Integrated Reliability Workshop Final Rep., IEEE Int.*, 2001.
[13] A. Hastings, *The Art of Analog Layout*, 2nd ed. Pearson Prentice Hall, 2006.
[14] "Synopsys CustomSim Circuit Check," *online: http://www.synopsys.com*.
[15] M. Rewieski, "A Perspective on Fast-SPICE Simulation Technology," in *Simulation and Verification of Electronic and Biological Systems*. Springer Netherlands, 2011, pp. 23–42.
[16] G. Georgakos, "Circuit Analyzer Systems and Methods," U.S. Patent US 2014/0 019 928 A1, 01 16, 2014.
[17] R. Sedgewick, *Algorithms*. Addison-Wesley Publishing Company, 1988.