DSP Based Programmable FHD HEVC Decoder

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***Abstract*—A programmable video decoding system with multi-core DSP and co-processors is presented. This system is adopted by Digital TV System on Chip (SoC) and is used for FHD High Efficiency Video Coding (HEVC) decoder under 400MHz. Using the DSP based programmable solution, we can reduce commercialization period by one year because we can parallelize algorithm development, software optimization and hardware design. In addition to the HEVC decoding, the proposed system can be used for other application such as other video decoding standard for multi-format decoder or video quality enhancement.**

Keywords—HEVC;FHD;DSP;

I. INTRODUCTION

Recently embedded systems should support a wide range of video standards. New video standards (VP8, HEVC[1]) as well as existing ones should be supported at multimedia devices. The merit of processor based approach is that commercialization period can be saved dramatically because the hardware can be developed based on existing processor and the software supporting the new video standard can be optimized in parallel with the hardware development. In spite of the advantages of processor based approach, it has weakness compared to full hardware approach. Y. Kikuchi et al [2] used a hybrid approach to trade-off between flexibility and performance. But their approach also has limitations for future extensions.

In this paper we propose a full programmable video decoding system composed of two Reconfigurable Processors (RPs) and two special purpose co-processors. We can get high performance and flexibility using the RP because it has massive parallel computing architecture and programmable feature. Bitstream decoding and SDRAM accessing performance are enhanced by Bitstream Process Unit (BsPU) and Memory Process Unit (MemPU) respectably.

Because the HEVC standard was not fixed when we started developing the RP based system, we developed the hardware architecture and software in parallel with the HEVC standard progress. By using this parallel development method, we could reduce the commercialization period by one year.

The remainder of this paper organized as follows. Section II gives an overview of the RP. In section III, problems of processor based system for video decoding are described in terms of video decoding application. The proposed video decoding system is presented in section IV. The experimental results and conclusion is followed in section V and section VI respectively.

II. OVERVIEW OF RECONFIGURABLE PROCESSOR

The basic RP architecture is a coarse-grained array and reconfigurable architecture [3]. The RP is consisted of coarse-grained arrays of functional units (FU), global and local register files, instruction cache, internal memory, configuration memory, and several bus connections for off-chip data transfer. The FUs are arranged on a NxM grid. In this paper 4x4 grid is used.

The RP has two operation modes: Very Long Instruction Word (VLIW) and Coarse-Grained Array (CGA). In VLIW mode, the RP behaves like a general purpose n-issue VLIW processor. The 2-issue was used for video system in this paper, which implies 2 FU out of 16 FU was used in VLIW mode. VLIW mode is used for sequentially or infrequently executed code. In CGA mode, the RP operates in data flow mode. In other words, there is no control flow. All entities are programmed via bits in so-called configuration memories. CGA mode can exploit loop level parallelism with all FUs and has good performance at repetitive arithmetic operations.

III. PROBLEM DEFINITION

We identified three disadvantages of RP for video applications. The first is that the RP is very inefficient for VLD (Variable Length Decoding), which has very strong dependencies between operations. The RP can execute 16 instructions in one cycle but the average instructions per cycle of VLD are about 1.5.

The second is huge memory bandwidth which results in waste of time for data transfer. In case of video decoding application major memory bandwidth is consumed by fetching the reference frame data for motion compensation.

The third is the low CGA efficiency due to the heavy control operations of video decoding application. The control operations can't be mapped in CGA but it can be mapped in VLIW. In VLIW mode only 2 FUs are in operation out of 16 FUs, which result in very low resource utilization.

To overcome these disadvantages, we introduce BsPU and MemPU to accelerate bitstream decoding and memory access respectably. Besides, the new parallelization architecture is developed to increase resource utilization.

IV. PROPOSED DECODING SYSTEM

In this section, the proposed decoding system is described as shown in Fig. 1. The proposed decoding system is composed of a BsPU, a MemPU and two RPs.

The bitstream decoding function is accelerated by using special instructions of BsPU. The SDRAM bandwidth is reduced by using MemPU. The performance enhancement is realized

through dual thread parallel execution architecture.

A. Bitstream Processing Unit (BsPU)

The processing flow of VLD is composed of bit acquisition, table mapping, and bit position update. These operations take 24 cycles using basic instructions of RP. We accelerated the bit acquisition and position update by using bitstream manipulation instructions. These instructions share a common hardware to buffer input bitstream from SDRAM, process the bit manipulation logic, and detect of three byte emulation prevention code.

B. Memory Processing Unit (MemPU)

The function of the memory processing co-processor is transferring data between the external memory and the internal memory of RP with a minimum bandwidth. By adopting tile based SDRAM access we can reduce wasted cycle by SDRAM latency. The number of SDRAM access is reduced by using a pixel cache which has 3-D feature (2-D block position and time). The detailed of the tiled memory access and the pixel cache are described in our previous work [3]. Additionally we adopted the multiple outstanding feature of BUS architecture. The co-processor of memory processing gives multiple read commands to the SDRAM controller. The SDRAM controller schedules the SDRAM and transfers data to memory processing co-processor.

C. Dual Thread Parallel Execution

The characteristic of video decoding application is that it has many control operations. The major control operations are motion vector decoding, mode decision including intra and inter mode. As shown in Fig. 2 (a) almost half of total cycle is consumed in VLIW mode. In VLIW mode only 2 FUs are operational, which results in the computing resources of 14 FUs are wasted in VLIW mode.

The resource utilization can be dramatically improved by parallelize the VLIW and CGA mode as shown in Fig. 2 (b). The control operations are performed in one block proceeding to the computational operations to parallelize the two operational modes. Parameters for the computational operations are drawn by the control operations and transferred via a FIFO between the VLIW and CGA as shown in Fig. 1.

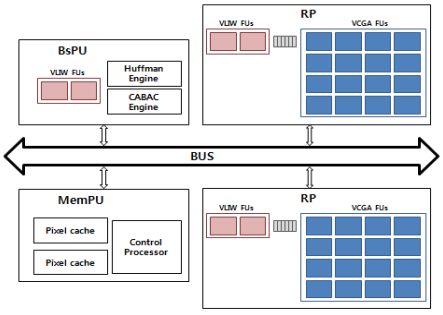

Fig. 1. System block diagram of video decoding system

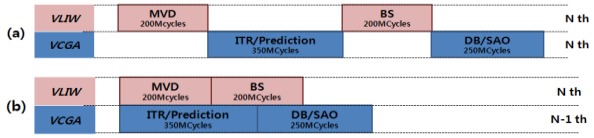

Fig. 2. Resource utilization enhancement using parallel dual threading (a) Single thread, (b) Dual thread

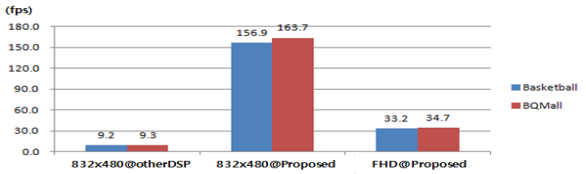

Fig. 3. The decoding performance comparison

V. EXPERIMENTAL RESULTS

We implemented our video decoding system on a DTV SoC chip and evaluated the decoding performance at 400MHz. HEVC main profile software supporting FHD resolution is implemented in the proposed video decoding system. The performance comparison of the proposed system and other DSP implementation [4] is shown in Fig.3. The required operation frequency of proposed system for FHD 30fps HEVC with 8Mbps is about 350MHz.

VI. CONCLUSION

This paper proposes a RP based video decoding system, which can decode FHD HEVC stream in real time. The system is composed of a BsPU, a MemPU, and two RPs. Bitstream decoding is accelerated by the BsPU. Memory bandwidth is reduced by MemPU. We also explored the new dual thread parallel execution architecture. By adopting this architecture we could enhance the performance about 40% compared to single thread architecture. The proposed system is embedded in DTV SoC and commercialized for FHD HEVC decoding. Using the RP based programmable solution, we can reduce commercialization period by one year because the hardware can be developed based on existing processor and the software can be optimized in parallel with the hardware development.

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