BASTION: Board and SoC Test Instrumentation for Ageing and No Failure Found

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***Abstract*— This is an overview paper that motivates and describes performed work done in the European Commission funded research project BASTION, which focuses on two critical problems of modern electronics: the No-Fault-Found (NFF) and CMOS ageing. New defect classes contributing to NFF have been identified, including timing related faults (TRF) at board level and intermittent resistive faults (IRF) at IC level. BASTION has addressed the mechanisms of ageing and developed several techniques to improve the longevity of electronic products. Embedded Instrumentation, monitors, and IEEE 1687 standard for reconfigurable scan networks (RSN) are seen as an important leverage that helped mitigating the impact of the above listed problems by facilitating a low-latency, scalable online system health monitoring and error localization infrastructure as well as integration of all heterogeneous technologies into a homogeneous demonstration platform. This paper helps the reader to get a general overview of the work performed and provides a collection of references to publications where the respective research results are described in detail.**

Keywords—No-Fault-Found, No-Trouble-Found, Aging, Embedded Instruments, IEEE 1687, IJTAG

I. INTRODUCTION

It is widely and well understood that shrinking feature sizes in semiconductor manufacturing technologies keep causing new reliability issues, especially in consumer electronics. International Technology Roadmap for Semiconductors (ITRS) lists ageing (Negative Bias Temperature Instability (NBTI), Positive Bias Temperature Instability (PBTI), Hot Carrier Injection (HCI), etc.) in semiconductor devices as one of the few most difficult challenges of process integration that affects reliability [ITRS12]. Another hard issue is product-level malfunctions that are difficult or impossible to reproduce – referred to as No Fault Found – NFF (also known as No Trouble Found – NTF) [ACC08].

Due to electrochemical effects, the ageing rate is a function of feature size that tends to increase when shifting to new technology nodes. Without additional measures, ageing would eventually manifest itself clearly by the end of the current decade. NFF in its turn is caused by a combination of test escapes, ageing, and environmental impact. The lack of understanding failure mechanisms and the need for modeling new materials, processes and devices are both constantly increasing. Hence, the impact of both phenomena is expected to grow unless corrective actions are taken.

NFF is being increasingly reported by industry and according to Accenture Report [ACC08], around 70% of all product returns were characterized as NFF. Cost-wise (including returns processing, scrap and liquidation), NFF amounted up to 50% of total 13.8 billion USD.

The general objective of the BASTION project is to develop methods united by the goal to improve overall dependability and stamina of nanoelectronics-based systems under pressure of ageing and unknown defects. The new approach to achieve the mentioned goal is based on the concept of embedded instrumentation and the corresponded standard IEEE 1687 that helps leveraging the silicon complexity problem in respect to system test and monitoring by proposing a scalable infrastructure for error processing that fits with heterogeneous System-on-Chip (SoC) integration and intellectual properties (IP) reuse target. On the way towards the general goal, we explore such uncharted application areas as IEEE 1687 assisted in-field fault management as well as reuse of embedded instrumentation at the system/board level.

In the rest of the paper, we give an overview of the research performed in the BASTION project. The paper is organized as follows. In Section II, we review existing test coverage metrics and detail identified criteria to handle ageing and NFF at component, board and system level. In Section III, we detail results on the development of instruments for realistic fault

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injection/evoking for high-performance test and diagnosis and methods and techniques for analysis, verification and optimization of IEEE 1687 network topologies. In Section IV, we present the results on modular (hierarchical) on-line test and monitoring based on IEEE 1687 to quickly detect errors, localize failing resources and perform failure recovery and system maintenance and a methodology for proper module isolation to allow simultaneous testing of one area while other areas maintain their functional mode of operation. In Section V, we present results obtained on using functional test programs exploiting the embedded instrumentation. The paper is concluded with a section describing the demonstrator (Section VI) and conclusions (Section VII).

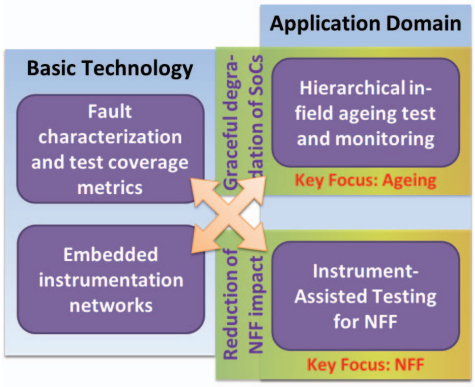

Figure 1. Application domains of BASTION project.

II. Fault Characterization and Test Coverage Metrics

We review existing test coverage metrics (based on Material, Placement & Solder (MPS), Presence, Polarity, Value & Solder (PPVS), Presence, Correct, Orientation, Live, Alignment/Short, Open, Quality, Feature, At-Speed, Measurement (PCOLA/SOQ/FAM)) and identify criteria to handle ageing and NFF at component (SoC, ASIC or FPGA), board and system level, and design a process to extract Defect Per Million Opportunity (DPMO) from traceability & repair database; investigate ageing mechanisms in CMOS chips and their manifestations in terms of faults in digital circuits; developed coverage metrics that use DPMO, and developed criticality and test coverage to measure the test efficiency.

A. Investigation of the No Fault Found phenomenon

We have designed a process to extract DPMO from traceability & repair database. A software application has been developed to collect & understand in-real time the DPMO, group defect label and root cause by defect class, and compute long term, medium term, short-term DPMO metrics. We have performed investigation of "preferred" area of occurrence for each defect class, and defined approximation criteria that can be used for new component: extrapolate the number from similar components. A gap in test coverage of board assemblies that resulted from insufficient measures available to the industry and in the literature in respect of handling Timing Related Faults (TRF) has been identified [JUT15]. We have carried out a study on intermittent resistive faults (IRF), a typical category of NFF. In [KER15], a dedicated computer-aided design (CAD) environment has been developed for fault simulation of IRFs in digital complementary metal-oxide-semiconductor (CMOS) circuits, including a versatile fault-injection module. As a result, we discovered the most sensitive parts to IRFs, which subsequently was extended to real hardware measurements, including the implementation of an IRF fault generator [EBR16a], showing indeed the predicted failures in a CMOS universal asynchronous receiver/transmitter (UART). The next step was the development of an IRF detector [EBR16b] which can start-up a logging of environmental conditions, thereby enhancing the diagnostic capabilities significantly.

B. Investigation of ageing faults in digital CMOS ICs

We have recapitulated the physical origins of dominating ageing faults, including intermittent faults, collected data based on characteristics (e.g. duration), represented faults for sensitivity fault simulations, and made sensitivity analysis on an industrial digital core. The latter included sensitivity to software constructions. With these efforts we reduced the number of embedded instruments for detection as well as their optimal locations and potential stimuli data. One of the aging mechanisms investigated in detail, is negative bias temperature instability (NBTI). We developed a model, also able to cope with non-digital stress voltages and it was verified by measurements [WAN16]. The required health monitors for aging of a processor core were employed during high temperature operating life (HTOL) tests for a long time and the results were used to give a first life-time prediction based on actual life-time measurements [ZHA16].

C. Instrument-assisted fault injection and sensitization

We characterized and investigated how faults are emulated in software and hardware. For board-level, we used field-programmable gate array (FPGA)-based high-performance embedded instruments and developed new ones for NFF investigation (speed/timing-related faults in the first place). To detect IRFs in printed circuit boards (PCBs), a set-up was made using test boards incorporating mixed-signal modules for IEEE 1149.4 PCB diagnosis. By adding components, like a current source and additional comparator, it was possible to detect IRFs in a particular resistance range [KER15].

D. Improvement of test coverage metrics

We imported real time DPMO and analyzed the information produced by Failure Mode Effects and Criticality Analysis (FMECA), which were combined with DPMO and test coverage to measure the test efficiency at system, board and component level. The weighted combined test coverage provided by the production lines of end users along with the collected DPMO and component failure criticality was used to calculate the overall test efficiency based on PCOLA/SOQ/FAM coverage metrics. We used the DPMO extraction for what-if analysis, performed cross-analysis to verify where the defect occurs, and made conformity analysis with estimated/measured coverage. We considered how defects should be detected early within the test flow. Traditional net and pin-level static fault models have been extended towards

TRFs in a way that enables straightforward integration with existing board test coverage analysis tools as well as detailed quantification of the "A" category in PCOLA/SOQ/FAM coverage metric [JUT15]. We also investigated the influence of ageing faults on the test-coverage metrics.

III. Embedded instrumentation networks

We detail results on development of instruments for fault injection/evoking for high-performance test and diagnosis and methods and techniques for analysis, verification and optimization of IEEE 1687 networks. More specifically, we developed: instruments for detection, diagnosis and recovery of ageing faults; HW/SW methods of injecting realistic faults based on: occurrence, shapes, and duration; instruments to cover delay/performance faults and provide diagnostic feedback; methods and techniques for retargeting, verification, optimization of IEEE 1687 topologies.

A. Design & validation of error detecting embedded instruments

We investigated to which extent our current solutions for permanent and temporary faults could be adapted, and incorporated data logging for instant repair and later diagnostics. The reuse at other hierarchical levels was considered, and to address smooth IP core integration and monitoring, we considered aspects like inter-instrument synchronization and interrupting [JUT16b], which are missing in the current version of IEEE 1687 standard.

B. Realistic fault evoking instruments

A software approach in combination with access embedded instruments was investigated to evoke certain faults. Simple instrument models were provided to simulate them in their environment and reuse at other hierarchical levels was kept in mind. Our measurements in the framework of evoking instruments have shown that intermittent resistive faults (IRF) are sensitive to their local temperatures. In that case, the resistance will significantly change due to thermo-mechanical stress in PCB soldering as well as chip interconnect (voids, cracks). This has stimulated the idea of controlling local temperatures (in a processor) by means of functional test-program generation [ALT16]. Along this line, programs were developed (and reused) which can determine the local temperature in a chip accurately, based on certain workloads in parts of a processor [ROH16]. In this local temperature stress can be evoked, enhancing the probability of occurring IRFs and hence detection. Instruments for high-performance test and diagnosis. We formulated requirements for both chip-level and FPGA-based embedded instruments to better address fault detection of those fault classes mostly contributing to NFF. We addressed design and redesign of chip-level embedded test instruments in a way that facilitated their later reuse for monitoring and board-level test purposes. We also concentrated on improvement FPGA-based board test instruments to cover delay/performance faults and provided diagnostic feedback [ALE16].

C. Analysis, verification and optimization of IEEE 1687 network topologies

We developed structural analysis methods for IEEE 1687 network topology, correctness and minimization of the hardware overhead while achieving the lowest possible test time. This involved, for example, the analysis if the network topology of an ICL network is functionally correct and conclusive (related to IEEE 1687 standards). New efficient and scalable approaches for sophisticated network analysis have been developed [ZAD14a], [ZAD14b], [ZAD16a]. The set of subtasks addressed contained, for example, the adaption of network topologies and mechanisms to support modular test as well as optimizing IEEE 1687 topologies with respect to requirements coming from the monitoring tasks and fault tolerant operation [JUT16a]. During the monitoring tasks, the instruments have to be constantly controlled and the IEEE 1687 instrumentation network has to be reconfigured on the fly, which is done by the embedded processor. This was considered as dynamic pattern retargeting done on the fly given the instrument connectivity language (ICL), the current state of all segment insertion bits (SIBs) in the network and desired actions to be performed with a target instrument, procedural description language (PDL) [PET14]. To secure IEEE 1687 networks we proposed an access protection concept. It is based on separation of the group of instruments applicable by the future device user and the group of security relevant instruments into two separate IEEE 1687 networks [BEC16].

IV. Hierarchical in-field ageing test and monitoring

We worked on modular (hierarchical) on-line test and monitoring based on IEEE 1687 aiming at quickly detect errors, localize failing resources and perform failure recovery and system maintenance and a methodology for proper module isolation to allow simultaneous testing of one area while other areas maintain their functional mode of operation. More specifically, we developed: error classification schemes and appropriate fault handling solutions; methods for adaptation and optimization of IEEE 1687 networks for fast and efficient error detection and diagnosis purposes; dynamic pattern retargeting, fault management methodology and in-field learning. Below we detail the main contributions.

A. Error classification schemes

We developed methods to classify the defects and for each class define appropriate error handling schemes [SHI16].

B. IEEE 1687 network for error detection and diagnosis

Given instruments for on-line error detection, we developed methods for infrastructure design that efficiently collects and propagates error detection and error diagnostics information to the top-level handler [SHI14], [ZAD16b], [LAR16]. . The work included adaptation and optimization of IEEE 1687 network topologies, development of optimized solutions for hardware insertions for IEEE 1687 compliant blocks with the focus of in-field testing. The developed methods facilitate module test isolation that allows simultaneous testing of one area while other areas maintain their functional mode of

operation and are not disturbed by the results of the module area under test. We developed a mechanism such that when errors occur the IEEE 1687 network is automatically configured so that only instruments that detected errors are included in the scan-path [ZAD16b], [LAR16]. With this scheme, the time for error localization is reduced significantly. The proposed IEEE 1687 networks also need to be tested against permanent faults affecting them. Effective solutions to automatically generate stimuli for test [CAN15] and diagnosis [CAN16a][CAN16b] have been proposed, taking into account that the adoption of suitable algorithms may significantly reduce the duration of the test. Finally, the BASTION partners introduced a suite of benchmark IEEE 1687 networks allowing researchers to better assess the effectiveness of their algorithms [TSE16].

C. Fault management methodology and field learning

Based on the above developed fault classification, instrument design and network topologies, we developed the top-level management schemes to collect information from instruments, classify errors, perform appropriate action [SHI16] create reports for NFF study. Focus was on the dynamic retargeting process, memory requirements, hierarchical module isolation, propagation of test coverage results. We also develop mathematical frameworks where we studied Rollback Recovery with Check-pointing under various assumptions, such as multiple jobs [NIK15a], [NIK15b], [NIK16].

D. Aging mitigation

We have proposed an approach to mitigate the time-dependent variation caused by NBTI based on *rejuvenation* of the stressed pMOS devices at NBTI-critical paths with dedicated stimuli sequences [JEN16], [PEL16]. It was enabled by an efficient hierarchical modelling of NBTI-induced degradation and NBTI-critical paths identification techniques– [KOS14], [KOS15] (also considering process variations [COP16]). The dedicated rejuvenation stimuli are generated using the evolutionary toolkit *μGP*. The flow is implemented and demonstrated in the scalable open-source framework *zamiaCAD* [TSE12], [JEN14]. The advantage of the approach is flexibility for solving the dependencies of impacts by individual gates to the most critical NBTI-induced path delays by using evolutionary optimization processes, thus, enhances the efficiency of aging relaxation. The proposed rejuvenation approach may have a significant impact on the circuit's lifetime extension. The preliminary experimental results on individual standalone circuits and processor designs demonstrate its feasibility and efficiency (up to 4 times lifetime extension and up to 33% relaxation efficiency improvement).

V. Instrument-Assisted testing for NFF

We present results obtained by using functional test programs exploiting the embedded instrumentation (both at the IC and board level) to improve the test capabilities with respect to static and dynamic defects. In the former case the main goal is reducing the test duration and complexity (by increasing the observability). We developed techniques leading to more efficient board-level test exploiting a mix of embedded instrumentation and functional test. More specifically, we developed new techniques for the generation of functional tests able to exploit embedded instruments (in particular those offered by the debug interfaces [DU16]), identified new instruments specifically focusing on dynamic fault identification at the PCB level by hard- and/or software with reconfigurable statistics, duration and shapes controlled via boundary scan (BS) / test access port (TAP) controller at PCB level; optimization of the test in terms of duration and resource requirements [GAU15]; and automation of test generation and development of integrated PCB test platforms.

A. Background Functional test programs exploiting the embedded instrumentation

By resorting to the above developed dynamic fault models, to the available embedded instruments, and to the IEEE 1687 access mechanisms, we developed techniques for the generation of functional test programs able to excite and detect dynamic faults, which are supposed to be the main cause of NFF escapes at board level. The approach mimics what has been done in the recent past for microcontrollers and SoCs (by adding embedded instruments to be used for design validation, silicon debug, and test) and was extended to PCBs, taking advantage of the existence of software accessible embedded instruments that can significantly improve the fault observability. We also investigated the usage of other instruments, corresponding for example to the debug infrastructure [DU16] and performance counters which are present in many microprocessors [PER16], to better support functional test. Finally, the BASTION partners successfully investigated new solutions to increase the effectiveness of functional test programs [PER16] and to automate the generation of functional programs for testing permanent faults in small- and medium-sized processors [RIE16].

B. Test optimization for duration, invasiveness, and defect coverage

We are improving the test generation procedures developed in the project, and making them complaining to industry constraints in terms of test duration, invasiveness (e.g., in terms of memory requirements) and defect coverage. In particular, some relevant results demonstrated how to reduce the size and duration of a functional test program without affecting its fault coverage capabilities [GAU15]. Special attention has been devoted to delay faults, and activities are ongoing to evaluate the ability of functional test program to effectively detect this kind of faults at the PCB level, as well as to provide guidelines to improve their effectiveness.

C. Chip-Level instrumentation reuse at the board level

The chip-level instrumentation was divided into fault-evoking embedded instruments and fault-detection embedded instruments. Control of the instruments and possible data dump was using the existing BS options during test [ALE16]. We investigated how the embedded instruments at IC level can be reused/reconfigured at PCB level. We included the development of the infrastructure by CAD tools and how to

include simulation/implementation of evokers, detectors and repair, thus achieving a validation of the proposed principle.

D. Automation and integration in a board-level test environment

While test generation is highly automated, a major limitation of the functional test approach lies in the fact that currently it is still mainly based on manual effort. However, the availability of libraries of already developed test programs (or templates) for some components, and of standard ways for describing existing interconnection structures and embedded instruments access mechanisms pave the way towards the automation of the test generation process. We therefore explored the possibilities offered by the new scenario and produced examples of tools for automating the generation of functional test programs exploiting embedded instruments. The results are being integrated into an existing commercial suite for board test support provided by Testonica Lab.

VI. BASTION Demonstration Platform

We offer tools and technologies, including at-speed test instrumentation and improved test coverage for high-performance board-level test, DPMO estimation tools for electronic products as well as software tools and on-line fault monitoring solutions to mitigate aging and NFF.

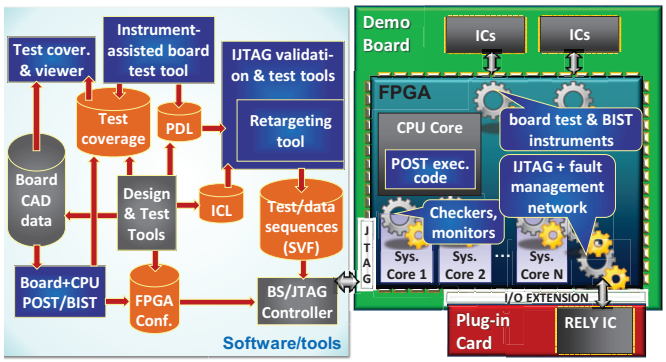

Figure 2. Demonstration platform for BASTION tools.

Most of BASTION HW solutions are based on IEEE 1687 standard infrastructure. This simplifies integration of respective tools into the demonstrator. The hardware part is based on a Xilinx ZYNQ development board. We have implemented hierarchical IEEE 1687 reconfigurable scan networks accessible through the JTAG port. In this way, standard IEEE 1687 tools can be used to access the instruments. Compatibility with traditional Boundary Scan test equipment is ensured by exporting retargeted data to SVF format. The IEEE 1687 instruments are supplied with alarm-based online fault detection and automated localization mechanisms. In addition, the FPGA supports board-level BIST and Power-On Self-Test (POST), whereas the latter is executed from the CPU core while being controlled by the instrumentation on the FPGA. Aging monitors on an external IC are integrated into the common IEEE 1687 network by means of plug-in card. The software tools shown in Figure 2 in blue have been developed in frames of BASTION. Grey boxes indicate available commercial solutions used.

VII. Conclusions

While it is well-supported by studies and surveys that No-Fault-Found (NFF) is a problem causing significant costs, we conclude, based on the survey we performed where several companies were invited, that it is difficult to get access to actual defect data to perform work to address the root causes of NFF. As future challenges we see the importance of finding ways such that industry can share sensitive data without risking that the market share is endangered or that an individual company can be pinpointed. Despite the general problem of getting access to NFF data, we have in the BASTION project made investigations on defect classes and performed significant amount of work on infrastructures (IEEE 1687) to access embedded instruments (sensors). Some key results are: (1) experimental results on circuits and processor designs demonstrate up to 4 times lifetime extension and up to 33% relaxation efficiency improvement, (2) new defect classes contributing to NFF have been identified, including timing related faults (TRF) at board level and intermittent resistive faults (IRF) at IC level, and (3) efficient algorithms for test time minimization, fault diagnosis, and fault management in IEEE 1687 networks that scale well when number of instruments increase.

VIII. References

[TSE16] A. Tsertov, A. Jutman, S. Devadze, M. Sonza-Reorda, E. Larsson, F. Ghani Zadegan, R. Cantoro, M. Montazeri, R. Krenz-Baath, “A Suite of IEEE 1687 Benchmark Networks” in Proc of 47th IEEE International Test Conference (ITC’2016), Fort Worth, TX, USA, Nov 15-17, 2016, paper 6.1.

[TSE12] A. Tšepurov, G. Bartsch, R. Dorsch, M. Jenihhin, J. Raik and V. Tihhomirov, "A Scalable Model Based RTL Framework zamiaCAD for Static Analysis," in IFIP/IEEE Int. Conf. on Very Large Scale Integration, 2012.

[RIE16] A. Riefert, R. Cantoro, M. Sauer, M. Sonza-Reorda and B. Becker, "A Flexible Framework for the Automatic Generation of SBST Programs," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 24, no. 10, 2016.

[PET14] K. Petersen, D. Nikolov, U. Ingelsson, G. Carlsson, F. Ghani Zadegan and E. Larsson, "Fault injection and fault handling: an MPSoC demonstrator using IEEE P1687," in International On-Line Testing Symposium (IOLTS), 2014.

[PER16] J. Perez Acle, R. Cantoro, E. Sanchez, M. Sonza-Reorda and G. Squillero, "Observability solutions for in-field functional test of processor-based systems: a survey and quantitative test case evaluation," MICROPROCESSORS AND MICROSYSTEMS, vol. 41, no. Sept., 2016.

[PEL16] F. Pellerey, M. Jenihhin, G. Squillero, J. Raik, M. Sonza-Reorda, V. Tihhomirov and R. Ubar, "Rejuvenation of NBTI-Impacted Processors Using Evolutionary Generation of Assembler Programs," in Asian Test Symposium (ATS), 2016.

[NIK15a] D. Nikolov and E. Larsson, "Optimizing the Level of Confidence for Multiple Jobs," IEEE Trans. on Computers, 2015.

[NIK16] D. Nikolov, U. Ingelsson and E. Larsson, "Maximizing Level of Confidence for Non-Equidistant Checkpointing," in Asia and South Pacific Design Automation Conference ASP-DAC, 2016.

[NIK15b] D. Nikolov, "Fault Tolerance for Real-Time Systems: Analysis and Optimization of Roll-back Recovery with Checkpointing," in Doctoral Thesis, 2015.
[NIK14] D. Nikolov, U. Ingelsson, V. Singh and E. Larsson, "Fault Tolerance for Real-Time Systems: Analysis and Optimization of Roll-back Recovery with Checkpointing," Microelectronics and Reliability , vol. 54, no. 5, 2014.
[LAR16] E. Larsson and F. Ghani Zadegan, "Accessing On-chip Instruments Through the Life-time of Systems," in IEEE 17th Latin-American Test Symposium (LATS) , 2016.
[KOS15] S. Kostin, J. Raik, R. Ubar, M. Jenihhin, T. Copetti, F. Vargas and L. Bolzani, "SPICE-Inspired Fast Gate-Level Computation of NBTI-induced Delays in Nanoscale Logic," in DDECS, 2015.
[KOS14] S. Kostin, J. Raik, R. Ubar, M. Jenihhin, F. Vargas, L. Bolzani Poehls and T. Copetti, "Hierarchical identification of NBTI-critical gates in nanoscale logic," in 15th IEEE Latin American Test Workshop (LATW), 2014.
[JEN16] M. Jenihhin, G. Squillero, T. Copetti, V. Tihhomirov, S. Kostin, M. Gaudesi, F. Vargas, J. Raik, M. Sonza-Reorda, L. Bolzani Poehls, R. Ubar and G. Medeiros, "Identification and Rejuvenation of NBTI-Critical Logic Paths in Nanoscale Circuits," JETTA, vol. 32, no. 3, 2016.
[JEN14] M. Jenihhin, A. Tsepurov, V. Tihhomirov, J. Raik, H. Hantson, R. Ubar, G. Bartsch, J. Escobar and H. Wuttke, "Automated Design Error Localization in RTL Designs," IEEE Design & Test, vol. 31, no. 1, 2014.
[ZAD14a] F. Ghani Zadegan, G. Carlsson and E. Larsson, "Robustness of TAP-Based Scan Networks," in International Test Conference (ITC), 2014.
[ZAD16a] F. Ghani Zadegan, R. Krenz-Baath and E. Larsson, "Retargeting Challenges in IEEE 1687 Networks," in Test Standards Application Workshop (TESTA), 2016.
[ZAD14b] F. Ghani Zadegan, E. Larsson, A. Jutman, S. Devadze and R. Krenz-Baath, "Design, Verification and Application of IEEE 1687," in Asian Test Symposium (ATS), 2014.
[ZAD16b] F. Ghani Zadegan, D. Nikolov and E. Larsson, "A Self-Reconfiguring IEEE 1687 Network for Fault Monitoring," in European Test Symposium (ETS), 2016.
[GAU15] M. Gaudesi, M. Sonza-Reorda and I. Pomeranz, "On Test Program Compaction," in *European Test Symposium (ETS)*, 2015.
[DU16] B. Du, E. Sanchez, M. Sonza-Reorda, J. Pérez Acle and A. Tsertov, "FPGA-controlled PCBA Power-On Self_test using Processor's Debug Features," in *19th IEEE International Symposium on Design & Diagnostics of Electronic Circuits and Systems*, 2016.
[COP16] T. Copetti, G. Medeiros, L. Bolzani Poehls, F. Vargas, S. Kostin, M. Jenihhin, J. Raik and R. Ubar, "Gate-level modelling of NBTI-induced delays under process variations," in *17th Latin-American Test Symposium (LATS)*, 2016.
[CAN16a] R. Cantoro, M. Sonza-Reorda, F. Ghani Zadegan, E. Larsson, A. Jutman and S. Devadze, "Test, Validation and Diagnosis of IEEE 1687 Networks," in *Test Standards Application Workshop (TESTA)*, 2016.
[CAN15] R. Cantoro, M. Montazeri, M. Sonza-Reorda, F. Ghani Zadegan and E. Larsson, "On the Testability of IEEE 1687 Networks," in *Asian Test Symposium (ATS)*, 2015.
[CAN16b] R. Cantoro, M. Montazeri, M. Sonza-Reorda, F. Ghani Zadegan and E. Larsson, "Automatic Generation of Stimuli for Fault Diagnosis in IEEE 1687 Networks," in 22nd IEEE International Symposium on On-Line Testing and Robust System Design, 2016.
[BEC16] M. Beck and P. Engelke, "On Safety and Security Aspects of IEEE 1687 Networks," in International Test Standards Application Workshop (TESTA), 2016.
[SHI14] K. Shibin, S. Devadze, A. Jutman, "Asynchronous fault detection in IEEE P1687 instrument network", in Proc of IEEE North Atlantic Test Workshop, Binghamton, NY, USA, May 14-16, 2014.
[SHI16] K. Shibin, S. Devadze, A. Jutman, "On-line Fault Classification and Handling in IEEE1687 based Fault Management System for Complex SoCs" in Proc. 17th IEEE Latin-American Test Symposium, Foz do Iguaçu, Brazil, April 6-8, 2016, pp. 69-74.
[SHI16] K. Shibin, S. Devadze, A. Jutman, "On-line Fault Classification and Handling in IEEE1687 based Fault Management System for Complex SoCs" in Proc. 17th IEEE Latin-American Test Symposium, Foz do Iguaçu, Brazil, April, 2016, pp. 69-74.
[JUT16a] A. Jutman, K. Shibin, S. Devadze, "Reliable Health Monitoring and Fault Management Infrastructure based on Embedded Instrumentation and IEEE 1687," in Proc. of AUTOTESTCON'2016, Anaheim, USA, Sept, 2016, pp. 240-249.
[JUT16b] A. Jutman, S. Devadze, K. Shibin, "Synchronization, Calibration and Triggering of IEEE 1687 Embedded Instruments", in *Proc. of the 17th Workshop on RTL and High Level Testing (WRTLT'2016)*, Nov. 24-25, 2016, Hiroshima, Japan, pp. 1-6.
[JUT15] A. Jutman, "Filling a Gap in Board-Level At-Speed Test Coverage" in Proc. IEEE Int. Workshop on Defects, Adaptive Test, Yield and Data Analysis, Anaheim, CA, USA, Oct 8-9, 2015, pp. 1-7.
[ALE16] I. Aleksejev, S. Devadze, A. Jutman, K. Shibin, "Optimization of Boundary Scan Tests using FPGA- based Efficient Scan Architectures", in Journal of Electronic Testing: Theory and Applications (JETTA), June 2016, Vol. 32, No. 3, pp. 245-255.
[ALE16] I. Aleksejev, A. Jutman, S. Devadze, "Run-Time Reconfigurable Instruments for Advanced Board-Level Testing", in Proc. of AUTOTESTCON'2016, Anaheim, USA, Sep., 2016.
[KER15] Kerkhoff, H.G. and Ebrahimi, H. ,"Intermittent Resistive Faults in Digital CMOS Circuits," in IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS), Belgrade, Serbia, April 2015, pp. 211-216.
[EBR16a] Ebrahimi, H and Kerkhoff, H.G., "Testing for Intermittent Resistive Faults in CMOS Integrated Systems", (DSD), ISBN 978-1-5090-2817-7/16, Limassol, Cyprus, August 2016, pp. 703-707.
[EBR16b]Ebrahimi, H and Rohani, A and Kerkhoff, H.G., "Detecting Intermittent Resistive Faults in Digital CMOS Circuits," in IEEE Defect and Fault Tolerance in VLSI and Nanotechnology Systems Symposium (DFT), Storrs, USA, September 2016, pp. 1-5.
[WAN16] Wan, J and Kerkhoff, H.G.," Simulating NBTI degradation in arbitrary stressed analog/mixed-signal environments," in IEEE Transactions on Nanotechnology,, 15 (2), 2016, pp. 137-148.
[ZHA16] Zhao, Y and Kerkhoff, H.G.," Highly Dependable Multi-Processor SoCs Employing Life-time Prediction Based on Health Monitors," in IEEE Asian Test Symposium, Japan, Nov. 2016..
[KER15] Kerkhoff, H.G. and Ebrahimi, H. ,"Detection of intermittent resistive faults in electronic systems based on the mixed-signal boundary-scan standard," in 6th Asia Symposium on Quality Electronic Design, Kuala Lumpur, Malaysia, August 2015, pp. 77-82.
[ALT16] Alt, J. et al.. ,"Thermal Issues in Test: An Overview of the Significant Aspects and Industrial Practice," in IEEE 34th VLSI Test Symposium, ISBN 978-1-4673-8454-4,, USA, April 2016, pp. 1-4.
[ROH16] Rohani, A and Ebrahimi H. and Kerkhoff H.G., "A Software Framework to Calculate Local Temperatures in CMOS Processors," in International Workshop on Power And Timing Modeling, Optimization and Simulation, Sep. 2016.
[ITRS12] International Technology Roadmap for Semiconductors:2012 Update Overview. [Online]. Available at:www.itrs.net/Links/2012ITRS/2012Chapters/2012Overview.pdf
[ACC08] Big Trouble with "No Trouble Found" Returns, Accenture Report, 2008, Available at: http://www.accenture.com/SiteCollectionDocuments/PDF/Accenture_Returns_Repairs.pdf