Reconfigurable Threshold Logic Gates using Optoelectronic Capacitors

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***Abstract*—This paper investigates the integration of optoelectronic devices with CMOS to implement reconfigurable threshold logic gates for Boolean functions. The weight of the optoelectronic device can be altered by changing the optical power which is used to reconfigure the threshold logic (TL) gate. These novel reconfigurable gates are called the optoelectronic capacitor based TL (OECTL) gates. The OECTL gates are designed for i) simplistic AND/NAND gates and OR/NOR gates with large fan-in and ii) linearly separable Boolean functions that can be reconfigured to other linearly separable Boolean functions, constrained in reconfiguration by the specifics of TL operation. SPICE simulations in 65nm bulk CMOS technology with a Verilog-A model for the optoelectronic capacitor demonstrate i) AND/NAND gates and OR/NOR gates are 2× faster as fan-in goes above 3 and consumes low power and ii) Boolean functions can be reconfigured with 0.58× smaller delay and 0.46× less power of standard CMOS design.**

I. Introduction

One of the prohibitions of widespread adaptation of Threshold Logic (TL) has been high cost of reconfiguration, without which TL is shown not to provide substantial savings over CMOS. TL gates have been implemented using look-up-tables (LUT) [1, 2], single electron transistors [3] and resonant tunneling diodes [4]. The implementations have drawbacks in terms of power, delay and area. Memristors have been used to reconfigure TL gates, however due to energy consumption and long re-programming delay, the benefits have been overshadowed [2, 5].

The novelty of this work is utilizing optoelectronic capacitors (OEC) to provide the varying weights of the TL for reconfiguration. The proposed gate is called optoelectronic capacitor based threshold logic (OECTL) gate. The OEC is from the literature by [6], originally proposed for optoelectronic (OE) sensors. The OEC devices in [6] change electrical properties of the device depending on the optical power at a certain bias voltage for sensor operation. In the simulation-based studies in this paper, the operation of a OECTL gate with reconfigurable weights is shown to implement reconfigurable Boolean functions.

II. Technical Background

TL circuit design is discussed in Section II-A followed by a discussion of the OEC in Section II-B.

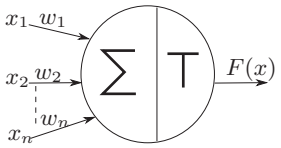

Fig. 1. Threshold Logic Gate.

A. Threshold Logic

Threshold logic is based on the majority or threshold decision principle, where the output value depends on whether the weighted sum of input variables exceeds the set threshold.

A TL gate is defined as a logic gate with n input variables, $x_i(x_1, x_2, ..., x_n)$, $x_i \in \{0, 1\}$ for which there is a set of weights $w_i \in \mathbb{R}$ and a threshold $T \in \mathbb{R}$ such that,

$$F(x) = sgn^1\{f(x)\} = \begin{cases} 0, & \text{if } f(x) < 0 \\ 1, & \text{otherwise} \end{cases} \quad (1)$$

$$f(x) = \left(\sum_{i=1}^{n} w_i x_i - T \right). \quad (2)$$

1) Capacitor based Threshold Logic Gate: Capacitance based TL gates have been presented in literature [1, 7, 8]. These designs suffer from the area overhead of accommodating multiple capacitors for different values. A self-timed threshold logic gate with poly-to-poly capacitors [8] is illustrated in Figure 2. The NMOS transistors N_3 to N_6 form the cross-coupled pair which generates the output OUT and its complement $\overline{OUT}$ after buffering through inverters. The potential at the $Input$ node is given by,

$$V_{Input} = \sum_{i=1}^{n} C_i x_i / C_{total} \quad (3)$$

where C_i is the capacitor value, x_i $(x_1, x_2, ..., x_n)$, C_{total} is the sum of the capacitances along with the parasitics at the $Input$ node N_2. The parameter V_{Input} is the weighted sum driving the gate of N_2. The threshold principle of the TL gate is the comparison of V_{Input} to the threshold voltage, as postulated in Equation (2):

$$f(x) = \sum_{i=1}^{n} C_i x_i / C_{total} - V_{Threshold} \quad (4)$$

[1] sgn(x) = 0, if x < 0, and sgn(x) = 1, otherwise

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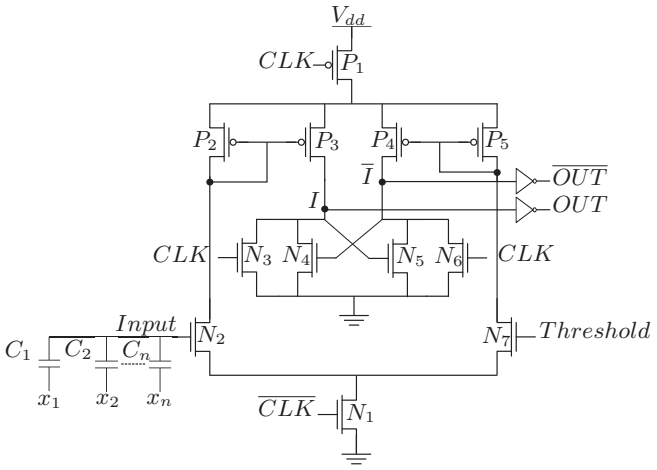


Fig. 2. Self-Timed Threshold Logic Gate [8].

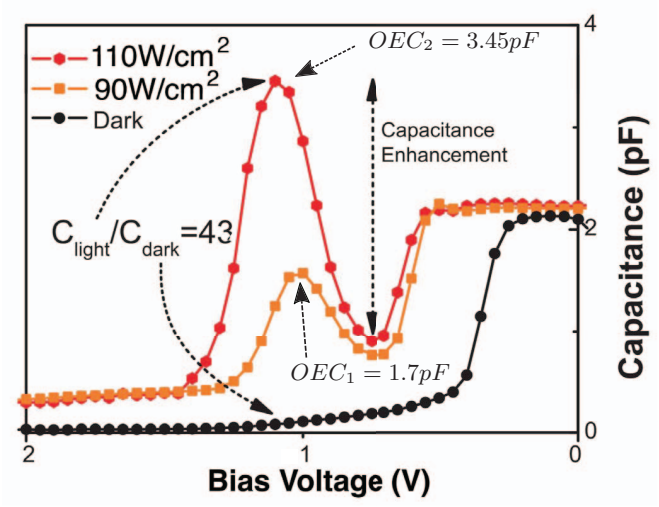


Fig. 3. Capacitance-Voltage characteristics of the device under dark and various illumination intensities [6].

B. Optoelectronic Capacitor

A device with a planar metal-semiconductor-metal (MSM) structure with a third plate consisting of a 2-D hole system (2DHS) is proposed in [6]. In the dark, the device shows the characteristics of a switchable capacitor when the CV characteristics are studied. When sufficient optical power is applied on the device at certain critical bias voltage, there is approximately 2× capacitance enhancement (CE). The structure of the device is discussed in [6]. The CV characteristics of the MSM-2DHS device obtained at a probe frequency of 10KHz and under two distinct optical powers of a 850nm laser as shown in Figure 3. The capacitance values for this work are chosen from the CV characteristics in Figure 3. For the sake of simplicity, only two capacitance values are chosen:

- OEC_1 is 1.7pF at a bias voltage of 1.1V and optical power of 90W/cm^2,
- OEC_2 is 3.45pF at a bias voltage of 1.1V and optical power of 110W/cm^2.

III. Optoelectronic Capacitor based Threshold Logic Gate

Altering the weights of a TL device makes reconfiguration possible. The weight w_i can be altered by changing the device capacitance C_i at the input voltage x_i. Here, the value of the capacitance C_i of the OEC can be controlled by its light intensity. Thus Equation (4) can be expressed as,

$$f(x) = \sum_{i=1}^{n} C_i(l_i)x_i/C_{total} - V_{Threshold} \quad (5)$$

where capacitance at the input $C_i(l_i)$, is defined as a function of the particular light intensity, l_i $(l_1, l_2, ..., l_n)$.

TL gates with OECs are designed as shown in Figure 4. In these proposed OECTL gates, the potential at the $Input$ node of Figure 4 is,

$$V_{Input} = \sum_{i=1}^{n} O_i(l_i)x_i/O_{total} \quad (6)$$

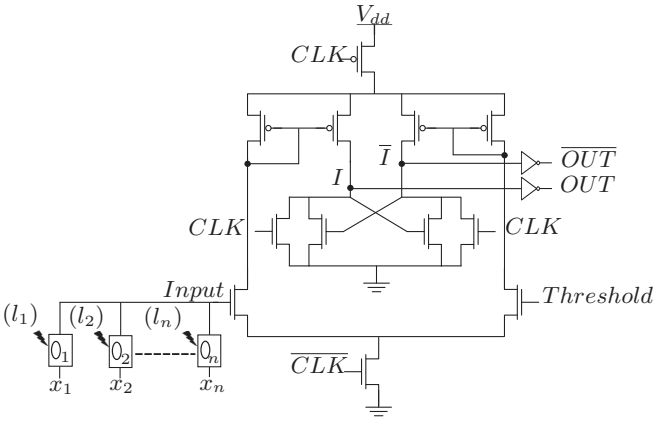


Fig. 4. OEC based Threshold Logic Gate (OECTL).

where $O_i(l_i)$ is the capacitance of an OEC at a particular light intensity l_i and O_{total} is the total capacitance including the parasitics. Thus, Equation (4) can be expressed as,

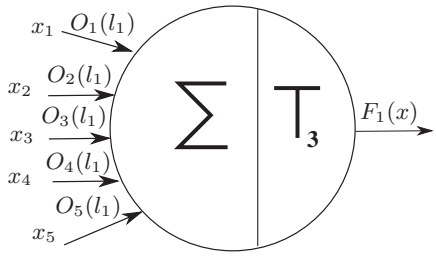
$$f(x) = \sum_{i=1}^{n} O_i(l_i)x_i/O_{total} - V_{Threshold}. \quad (7)$$

IV. Proposed OECTL Designs

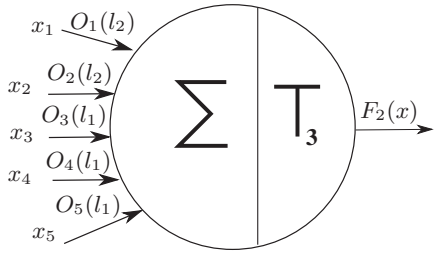
The OECTL gates are designed with CMOS transistors to design i) AND/NAND gates and OR/NOR gates and ii) reconfigurable Boolean functions.

A. Design methodology of OEC simulations

The CV characteristics of the device are reproduced using Verilog-A. The model, where the Verilog-A model has 96% accuracy compared to the CV characteristics of the device at different optical powers and in dark (measurements shown in Figure 3 [6]). Simulations for the OECTL gate are performed at a supply voltage of 1.1V in a 65nm technology node.

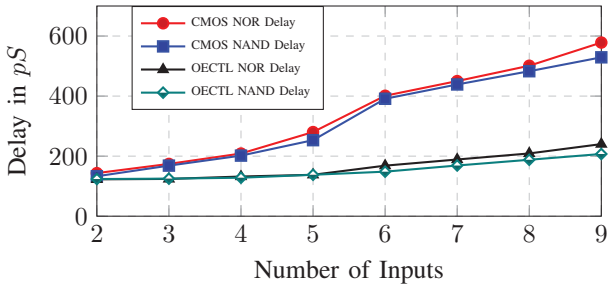


(a) $F_1(x) = x_1x_2x_3(x_4 + x_5) + x_4x_5(x_1x_2 + x_1x_3 + x_2x_3)$

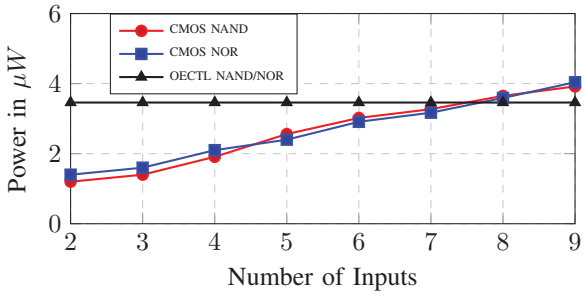


(b) $F_2(x) = x_1x_2 + (x_1 + x_2)(x_3x_4 + x_4x_5 + x_3x_5)$

Fig. 5. Reconfiguration of OECTL gate (a) Function 1 (b) Function 2, l_1 and l_2 are optical powers of $90W/cm^2$ and $110W/cm^2$ respectively.



(a) NAND and NOR Gate delay



(b) NAND and NOR Gate power

Fig. 6. Delay and power comparison of NAND and NOR Gates.

B. NAND and NOR Gate

TL gates are suitable for large fan-in AND/NAND and OR/NOR gates [9]. A two input AND/NAND gate is designed using the OECs. The unit capacitance value is chosen to be OEC_1. $V_{Threshold}$ for a two input AND/NAND gate is set at T_1 = 0.9V. The performance in terms of delay and power for fan-in of 2 to 9 are evaluated. Similarly, OR/NOR gates are designed using the OECs for a fan-in of 2 and $V_{Threshold}$ of T_2 = 0.6V. It is then evaluated for varying fan-ins. The advantage of a differential design is that AND/NAND and OR/NOR gates can be designed with the same gate. CMOS based NAND and NOR gates are implemented for similar fan-ins and evaluated for delay and power.

C. Reconfiguration of OEC based TL Gate

Two Boolean functions that are linearly separable with the same $V_{Threshold}$ of 0.85V is chosen to demonstrate the reconfiguration of an OECTL gate. The two Boolean functions are $F_1(x)$ and $F_2(x)$ as shown in Figure 5. In a single OECTL gate, the optical power of the OECs are altered to implement the functions. In Figure 5(a), l_1 is an optical power of $90W/cm^2$ on the inputs setting it to OEC_1. $V_{Threshold}$ for the OECTL gates is set at T_3 = 0.85V. The optical power for the input x_1 and x_2 is changed to l_2 setting it to OEC_2, which is a weight of 2 to implement $F_2(x)$. In Figure 5(b), the optical power on input x_1 and x_2 is changed to l_2 and for the inputs x_3, x_4 and x_5 remain at l_1.

V. Experimental Results

The delay of the proposed AND/NAND and OR/NOR gates along with standard CMOS implementation of NAND and NOR gates are shown, particularly OECTL gates have superior performance in terms of delay when the fan-in increases. For a fan-in of 6, OECTL gates are ≈2× faster when compared to standard CMOS as shown in Figure 6(a). In Figure 6(b), the power of standard CMOS NAND and NOR gates are shown along with the power for OECTL gates. It can be observed that as the fan-in increases the power consumption of OECTL does not show an increase (unlike CMOS) due to the low power characteristics of the OEC devices. In literature the power of the OEC devices are considered to be in atto-joules levels [10]. Based on this expectation of negligible power consumption of OEC devices, OECTL and CMOS designs have very similar power consumption for a fan-in of 8.

In Figure 7, the simulation results for the reconfiguration of OECTL gate are shown. During the precharge phase, the signals OUT and $\overline{OUT}$ are at V_{dd}. During evaluate phase, when V_{Input} is greater than $V_{Threshold}$ of 0.85V, OUT goes to V_{dd} and $\overline{OUT}$ is 0. When V_{Input} is less than $V_{Threshold}$, OUT and $\overline{OUT}$ go to 0 and V_{dd}, respectively. The signal $Light$ is the select line that sets optical power for the OEC. The optical powers of $O_1(l_1)$ and $O_2(l_1)$ are both changed to $110W/cm^2$, which changes the capacitance value to OEC_2. This capacitance change switches the TL function from $F_1(x)$ to $F_2(x)$ by altering the weight. The output is shown in signal OUT. Table I summarizes the results of reconfiguration of the OECTL gate. The two boolean functions are implemented in standard CMOS with 2 input NAND and NOR gates. The worst case propagation delays for $F_1(x)$ and $F_2(x)$ are 168.9ps and 178.4pS, respectively. The delay of the OECTL design is 0.58× of standard CMOS implementations for the two Boolean functions. The power consumed by both OECTL designs is 3.46μW. The OECTL design consumes 0.46× less power on average of standard CMOS implementations.

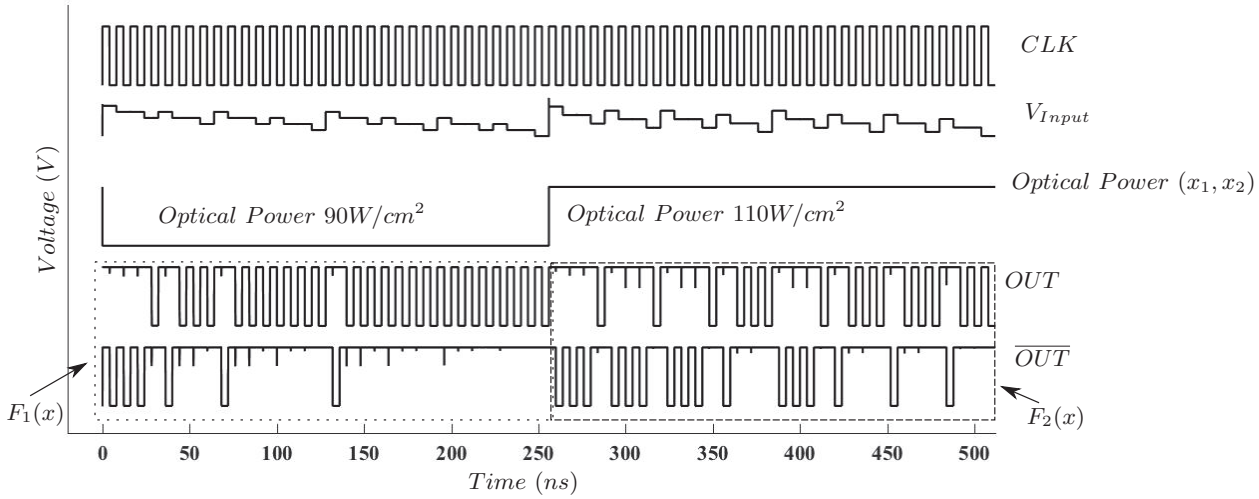


Fig. 7. Simulation waveform showing reconfiguration of OEC based TL Gate.

TABLE I. PERFORMANCE OF OECTL AND CMOS IMPLEMENTATIONS OF $F_1(x)$ AND $F_2(x)$.

Boolean Function	Delay (CMOS) (ps)	Power (CMOS) (μW)	Delay (OECTL) (ps)	Power (OECTL) (μW)	Delay (OECTL) (Normalized to CMOS)	Power (OECTL) (Normalized to CMOS)
$F_1(x)$	317.2	10.2	168.9	3.46	0.53×	0.34×
$F_2(x)$	283.7	5.9	178.4	3.46	0.63×	0.58×
Average					0.58×	0.46×

VI. PRACTICAL CONSIDERATIONS

In order for OECTL to be appealing in mainstream design, the following practical considerations need to be addressed:

1) Size of device: To design on chip capacitors of $3.45pF$ or $1.7pF$ would require considerable area. Considering a capacitance per unit area of $800aF/\mu, m^2$ the area for $3.45pF$ or $1.7pF$ would be $4312\mu m^2$ and $2125\mu m^2$, respectively. The dimensions of the OEC are not reported in [6] however, from personal communication it is known that manufacturability at dimensions of mm^2 to μm^2 are feasible for varying OE CV characteristics.
2) The authors conclude two ways for OECs to be used with CMOS: (i) OECs with large dimensions are amenable for individual light sources (l_i) as purported in this paper. (ii) OECs with small dimensions can be competitive with traditional MOSCAPs based TL implementations in addition to the reconfiguration advantage in this paper.

VII. CONCLUSION

In this work, OECs are integrated with CMOS transistors demonstrating the applicability of OEC devices to facilitate energy-efficient logic computation. It is shown that the OECTL gates can be designed to operate at $0.58\times$ higher speeds than CMOS equivalents while consuming $0.46\times$ less power on average. Reconfiguration of the TL circuit is achieved by altering the weight without significant overhead.

REFERENCES

[1] V. Beiu, J. M. Quintana, and M. J. Avedillo, "VLSI implementations of threshold logic-a comprehensive survey," *IEEE Transactions on Neural Networks*, vol. 14, no. 5, pp. 1217–1243, Sept 2003.
[2] J. Rajendran, H. Manem, R. Karri, and G. S. Rose, "An energy-efficient memristive threshold logic circuit," *IEEE Transactions on Computers*, vol. 61, no. 4, pp. 474–487, April 2012.
[3] C. Moffat, "A survey of nanoelectronics," *University College, London, U.K., 1994*, Available: http://ipga.phys.ucl.ac.uk/papers/rep94-2.pdf.
[4] K. J. Chen, T. Akeyoshi, and K. Maezawa, "Monolithic integration of resonant tunneling diodes and FET's for monostable-bistable transition logic elements (MOBILE's)," *IEEE Electron Device Letters*, vol. 16, no. 2, pp. 70–73, Feb 1995.
[5] I. Vourkas and G. C. Sirakoulis, "Emerging memristor-based logic circuit design approaches: A review," *IEEE Circuits and Systems Magazine*, vol. 16, no. 3, pp. 15–30, 2016.
[6] P. Dianat, A. Persano, F. Quaranta, A. Cola, and B. Nabet, "Anomalous capacitance enhancement triggered by light," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 21, no. 4, pp. 228–232, July 2015.
[7] H. Ozdemir, A. Kepkep, B. Pamir, Y. Leblebici, and U. Cilingiroglu, "A capacitive threshold-logic gate," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 8, pp. 1141–1150, Aug 1996.
[8] P. Celinski, J. F. Lopez, S. Al-Sarawi, and D. Abbott, "Compact parallel (m,n) counters based on self-timed threshold logic," *Electronics Letters*, vol. 38, no. 13, pp. 633–635, Jun 2002.
[9] H. Huang and T. Wang, "CMOS capacitor coupling logic circuits," in *Proceedings of the IEEE Asia Pacific Conf. on ASICs*, 2000, pp. 33–36.
[10] D. Miller, "Attojoule optoelectronics for low-energy information processing and communications - a tutorial review," *arXiv:1609.05510 [physics.optics]*.