Enabling Area Efficient RF ICs through Monolithic 3D Integration

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***Abstract*—The Monolithic 3D (M3D) integration technology has emerged as a promising alternative to dimensional scaling thanks to the unprecedented integration density capabilities and the low interconnect parasitics that it offers. In order to support technological investigations and enable future M3D circuits, M3D design methodologies, flows and tools are essential. Prospective M3D digital applications have attracted a lot of scientific interest. This paper identifies the potential of M3D RF/analog circuits and presents the first attempt to demonstrate such circuits. Towards this, a M3D custom design platform, which is fully compatible with commercial design tools, is proposed and validated. The design platform includes process characteristics, device models, LVS and DRC rules and a parasitic extraction flow. The envisioned M3D structure is built on a commercial CMOS process that serves as the bottom tier, whereas a SOI process is used as top tier. To validate the proposed design flow and to investigate the potential of M3D RF/analog circuits, a RF front-end design for Zig-Bee WPAN applications is used as case-study. The M3D RF front-end circuit achieves 35.5 % area reduction, while showing similar performance with the original 2D circuit.**

I. Introduction

The advent of M3D integration technology has opened up opportunities for the continuation of Moore's law. The M3D integration technology consists of tiers of devices fabricated one upon the other in a sequential manner. For example in a two-tier configuration, a thin semiconductor film is created over the bottom tier that serves as the top active region. The low thickness of the top active layer implies SOI transistors (planar and FinFETs) for this tier. Adjacent tiers are separated through an Inter-Layer Dielectric (ILD) and devices in different tiers are connected through Monolithic Inter-layer vias (MIVs). The latter are comparable in size with inter-metal vias enabling thus high vertical interconnection density, even at transistor level.

In this work, a design platform for custom M3D circuits is proposed and applied for RF/analog circuits. The proposed platform could facilitate the further development of M3D integration technology as well as the design and demonstration of M3D RF/analog and mixed-signal (RF/AMS) circuits. As a demonstration vehicle, a low power RF front-end receiver suitable for the Zig-Bee WPAN standard is designed using the proposed M3D platform and compared with an actual 2D implementation. This paper is structured as follows: in Section II the related work in this field is described and the need for a M3D custom design flow is identified. In Section III this design flow is presented and its features (process structure, device models, parasitic extraction flow) are analyzed. The design of the M3D RF front end is discussed in Section IV and its performance is summarized in Section V. Finally, a conclusion is reached in Section VI.

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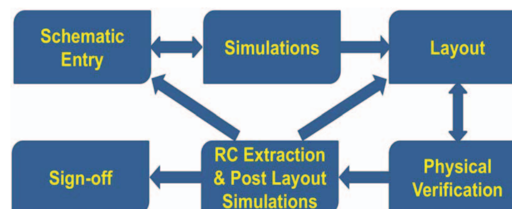

Fig. 1. Custom Design Flow for RF/AMS circuits

II. Related Work

The commercialization of M3D integration technology is currently impeded by processing issues. In particular, care must be taken to secure that the bottom tier devices do not degrade during the high-temperature processing of the top tier ones. To overcome this temperature barrier, various solutions have been proposed in [1], [2], [3] and [4] where, no degradation of the bottom tier devices is reported. As for the routing metals, tungsten should be employed for the bottom tier, in order to withstand the top tier processing, [5].

Various design methodologies for M3D digital circuits have been proposed so far, [5], [6]. To the best of our knowledge there is no prior work on M3D integration for RF/AMS ICs. For radio circuits in particular, M3D integration could have a twofold advantage that stems from the inherent area reduction and the SOI nature of the top tier devices. SOI transistors offer: a) lower junction capacitances and b) steeper subthreshold slope compared to bulk technologies, [7]. An intuitive approach for M3D RF designs is a partition scheme based on frequency-planning: the inductors along with the high frequency blocks could be implemented on the top tier with SOI devices whereas baseband blocks running at lower frequencies could be placed in the bottom tier. M3D integration has the potential to become a key enabling technology for implementing minimum sized low-range radio circuits, suitable for Internet of Things applications.

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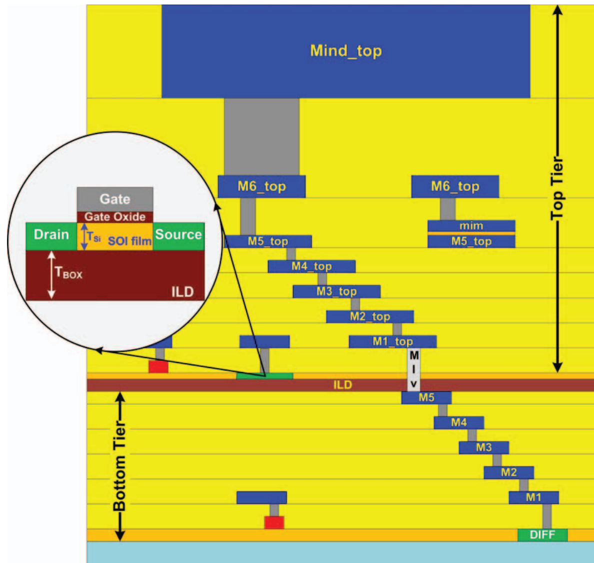


Fig. 2. Structure of the envisioned M3D process. Connection between the bottom and top tiers is achieved through MIVs.

TABLE I
METAL DIMENSIONS AND INTERCONNECT PARASITIC RESISTANCES

Metal Layer	Thickness	Sheet Resistance
M1-M5	400 nm	0.2 Ω
MIM layer	150 nm	-
M1_top - M5_top	400 nm	0.1 Ω
M6_top	800 nm	0.05 Ω
Mind_top	6 μm	-

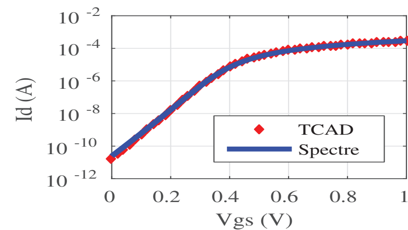


Fig. 3. Id vs Vgs for a top tier SOI with L=150 nm, W=1 μm and V_{DS}=1 V

III. M3D DESIGN FLOW

The design flow for RF/AMS M3D circuits differs from the already proposed digital design flows. There is no need to redesign digital cell libraries or modify the place and route tools. Instead, the custom design flow depicted in Fig. 1 must be used. Knowledge of the process characteristics is instrumental in every step of the design flow. In addition, accurate device models for both tiers as well as a parasitic extraction flow that can capture the coupling between two adjacent tiers are necessary. These aspects are described in the following subsections.

A. Process Structure

The M3D structure that is considered and used in this work is illustrated in Fig. 2. It is built upon a commercial 150 nm CMOS bulk process that serves as the bottom tier and will be referred to as the ”base” process. This is in accordance with [2] and [4], where M3D processes that can be integrated with any existing fab process are presented. It also offers the chance to re-use the LVS and DRC decks of the base process. Routing resources consist of five bottom tier metal layers made of tungsten (M1 - M5) and six top tier aluminum ones (M1_top - M6_top). The thickness of all the metal layers is listed in TABLE I. A 500 nm thick dielectric is assumed over M5 that serves as the Inter-Layer Dielectric (ILD). Over the ILD, a thin (13 nm thick) unstrained Si device layer is created. Its thickness has been defined to ensure similar Drain Induced Barrier Lowering (DIBL) between the top and bottom transistors.

Apart from the active devices, the envisioned M3D process contains passive elements as well. A MIM layer is considered between M5_top and M6_top. It yields approximately 1 $fF/\mu m^2$ of capacitance density. Furthermore, the base process inductors are implemented in the topmost thick metal, Mind_top (top tier), which is reserved only for this purpose. Since the distance between the topmost metal and the substrate (bottom tier) is increased (see Fig. 2), the parasitic capacitances to the substrate of the inductor models are proportionally scaled. Both the MIM capacitors and the inductors could have been designated at the bottom tier. However, in such case, the separation between two adjacent tiers would be significantly higher (see TABLE I), inducing considerable interconnect parasitics to a design. Two different resistor flavors are also available: a salicided poly-based resistor with low sheet resistance (10Ω) and a non salicided poly with high sheet resistance (2kΩ). A bottom tier resistor implementation is preferred to avoid overcrowded top tiers, given the existence of MIM capacitors and inductors on the top tier.

B. Device Models

In [8], it is shown that the top tier processing does not affect the bottom transistors' performance significantly given that the top tier thermal budget does not exceed 500°C. Therefore, the base process' BSIM3 models are used for the bottom tier transistors. The structure of a top tier transistor is shown in the inlet of Fig. 2. The ILD serves as the buried oxide (BOX) of the SOI devices. CEA-LETI's UTSOI2.1 model for ultra thin body SOIs is used for these devices, [9], [10]. The relatively thick (500 nm) ILD minimizes the coupling between the two tiers as this is described in [11]. The UTSOI2.1 model parameters have been set so as to match TCAD simulations. The results shown in Fig. 3 demonstrate the good agreement with the TCAD simulations.

Since the focus of this work lies with RF/analog circuits, the noise behavior of the top tier transistors must be captured by the models. Low frequency noise in SOIs has been studied in [13]. Given the large buried oxide (ILD) thickness, the control of the back gate over the channel area is small and

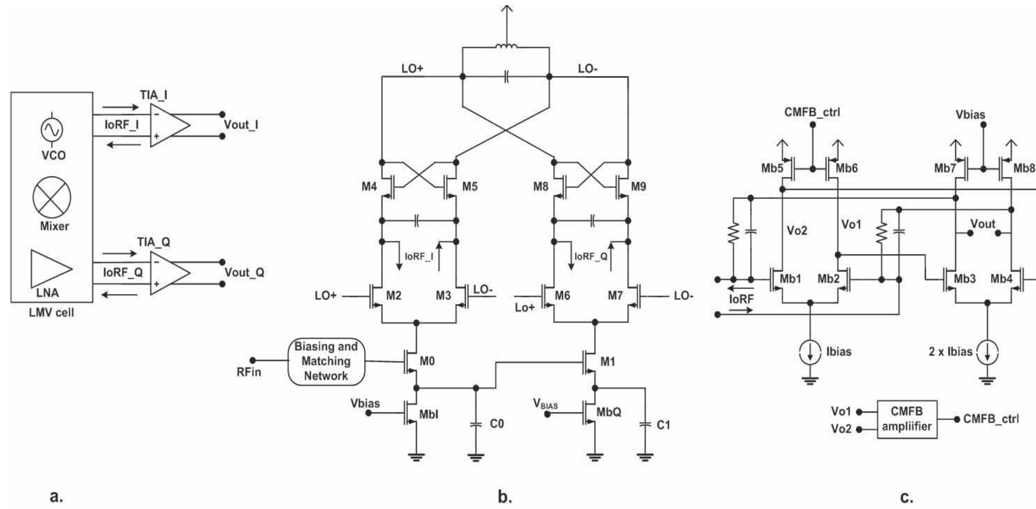


Fig. 4. a) M3D radio front end block level schematic. b) Schematic of the LMV cell [12]. The biasing implementation is not shown c) Baseband TIA schematic. The implementation of the biasing and the CMFB amplifier is not shown.

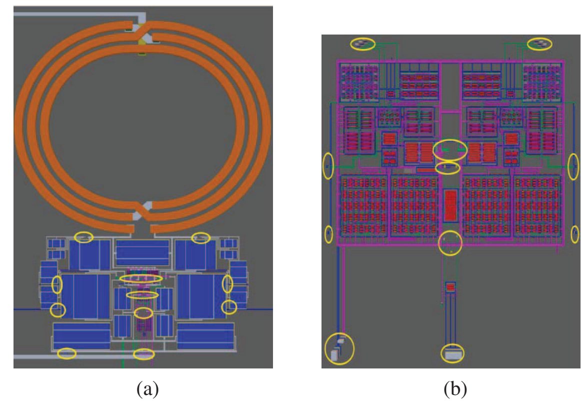
so the contribution of the buried oxide's (ILD's) interface in a top SOI's low frequency noise is assumed negligible. Thus, the UTSOI2.1 low frequency noise parameters have been leveraged to match the noise performance of the bottom transistors. The same strategy has been also applied for the thermal noise parameters.

C. Parasitic Extraction Flow

An accurate parasitic extraction flow is essential for the scope of this work. The Cadence Quantus extraction flow is employed for full compatibility with established design methodologies. The critical impediment in using a commercial extraction flow built for planar processes, is the inability to define more than one diffusion layers. Towards this, the top active layer is assumed a conductor. In a different case, the parasitics of the top tier contacts would be neglected. The parasitic extraction flow considers also the use of tungsten for the bottom tier routing. Tungsten has approximately double the resistivity of aluminum as it can be seen in TABLE I. Overall connecting M1 to M1_top with a single via stack incurs 10Ω resistance and 0.1fF of capacitance.

IV. M3D RF FRONT END

As a showcase of the proposed design platform's capabilities, a M3D radio front end for Zig-Bee applications is designed and simulated. The M3D front end utilizes the LNA-mixer-VCO (LMV) stacked cell from [12] and two transimpedance amplifiers (TIA) (see Fig. 4a). For simplicity, no complex filters or variable gain amplifiers have been added. The LMV cell (see Fig. 4b) is implemented on the top tier, except from the biasing resistors. Note that the biasing network is not included at all in Fig. 4. The LMV cell outputs a differential down-converted current. Each of the quadrature output currents I_{oRF_I} and I_{oRF_Q} feeds into the corresponding transimpedance amplifiers TIA_I and TIA_Q. A two-stage configuration is employed for each TIA (see Fig.



(a) (b)

Fig. 5. Layout view of: (a) top tier and (b) bottom tier. The location of MIVs is highlighted in yellow

4c). The transistors and resistors of the TIAs are placed in the bottom tier, whereas the capacitors in the top one. The layout of both tiers is shown in Fig. 5. The MIV locations are highlighted with yellow circles. A cluster of 36 MIVs are used in each of the four interfaces between the radio and baseband circuits (2 for I_{oRF_I} and 2 for I_{oRF_Q}), aiming to reduce the resistive paths. To avoid any inductive coupling from the top tier inductor to bottom tier devices, no bottom tier devices have been placed underneath the inductor. A snapshot of the M3D layout is illustrated in Fig. 6 .

V. RESULTS

The post-layout simulations of the M3D RF front-end are shown in TABLE II together with the standard specifications as extracted from [12]. The results in parenthesis indicate schematic simulations. The most important impact that M3D integration has on the designed front-end is, as expected, the reduction by 35.5 % of the total area. For a fair comparison, the footprint of the complex filter and the variable gain

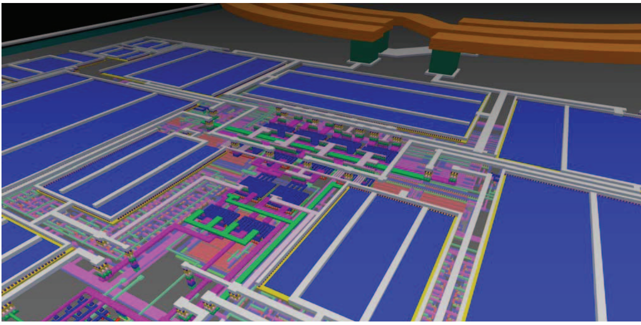


Fig. 6. Snapshot of the M3D RF front end layout. The bottom tier can be seen with less brightness

TABLE II
SIMULATED CIRCUIT PERFORMANCE

Items	This Work	[12]	Specs
Technology	M3D 150 nm	90 nm	-
Area	$0.120mm^2$	$0.186mm^2$	-
Supply	1.8V	1.2V	-
Power	3.6mW	3.6mW [a]	-
Gain	36dB [b]	75dB	65dB
Noise Figure	10.8 (10) dB	12dB	<15.5dB
IIP3	-17 (-14.5) dBm	-12.5dBm	>-32dBm
LO phase noise @ 3.5MHz offset	-122 (-128) dBc/Hz	-107.8dBc/Hz	-102dBc/Hz
LO leakage	-77dBm	-60dBm	-
S11	-15 (-17) dB	-13dB	-10dB

[a] Complete chain including variable gain amplifier and poly phase filter
[b] The M3D front end does not contain a variable gain amplifier

amplifier that are included in [12] have not been considered in the area calculations. A higher area reduction could be possible if a custom designed inductor was employed. Moreover, if a more advanced technology node is used, with thiner MIM oxides, higher capacitance densities would be possible for the MIM caps, leading to further area reductions. One last potential technique for further area reduction is the placement of bottom tier devices directly below the top tier inductor, using of course the necessary shielding techniques.

As far as the Zig-Bee specifications are concerned, the M3D RF front-end matches its 2D counterpart, [12], for most of the performance metrics (IIP3, Noise Figure, phase noise and S11). Of particular importance is the reduction of the LO leakage at the input. This feature can be attributed to the complete lack of substrate in the top tier, an additional benefit that M3D integration technology offers to radio circuits. The conversion gain versus the frequency of the output signal presented in Fig. 7, shows that a maximum gain of 36dB is achieved. By inserting a variable gain amplifier at the output of the M3D chain (which is the case in [12]), the standard specifications for the gain would be easily met.

As for the power consumption, even without the variable gain amplifier and the complex filter it is as high as [12], where the whole chain is implemented. This is due to the

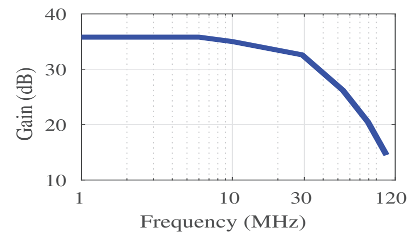


Fig. 7. Conversion gain simulation results

older technology node used (150 nm) which presents lower transit frequency f_T compared to the 90 nm CMOS process used in [12] and therefore requires more current to achieve the same performance (1.6mA is consumed by the LMV cell and 400 μA by the two TIAs).

VI. CONCLUSION

In this work, the potential of M3D integration technology for RF/analog circuits has been studied. To facilitate this study, a design platform suitable for custom M3D RF/AMS circuits, which considers all the unique process characteristics and features of M3D integration, has been proposed. To validate the functionality of the proposed platform and effectively prove the potential of M3D RF/analog circuits, a M3D RF front-end has been designed. The post-layout simulation results show that the M3D circuit exhibits around 35.5 % area reduction with no performance degradation, which demonstrates the feasibility of M3D integration for RF/analog circuits.

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