Noise-Sensitive Feedback Loop Identification in Linear Time-Varying Analog Circuits

Ang Li Peng Li Tingwen Huang Edgar Sánchez-Sinencio Department of Electrical Department of Electrical Texas A&M University Department of Electrical and Computer Engineering and Computer Engineering at Oatar and Computer Engineering Texas A&M University Texas A&M University P.B.O.X. 23874, Doha, Qatar Texas A&M University College station, TX 77843 College station, TX 77843 Email:tingwen.huang@qatar.tamu.edu College station, TX 77843 Email: ali09@tamu.edu Email: pli@tamu.edu Email: s-sanchez@tamu.edu

Abstract-The continuing scaling of VLSI technology and design complexity has rendered robustness of analog circuits a significant concern. Parasitic effects may introduce unexpected marginal instability within multiple noise-sensitive loops and hence jeopardize circuit operation and processing precision. The Loop Finder algorithm has been recently proposed to allow detection of noise-sensitive return loops for circuits that are described using a linear time-invariant (LTI) system model. However, many practical circuits such as switched-capacitor filters and mixers present time-varying behaviors which are intrinsically coupled with noise propagation and introduce new noise generation mechanisms. For the first time, we take an in-depth look into the marginal instability of linear periodically time-varying (LPTV) analog circuits and further develop an algorithm for efficient identification of noise-sensitive loops, unifying the solution to noise sensitivity analysis for both LTI and LPTV circuits.

I. INTRODUCTION

With technology scaling and growing design complexity, the designers have witnessed increased on-chip and off-chip parasitic effects in analog circuits. Parasitics can create a large number of unintended, insufficiently damped feedback signal loops, in which noise can propagate and undermine the performance of analog circuits. These problematic loops are called unstable in [1]–[3]. To make the matter clearer, we more precisely use the term "marginally unstable" or "marginal instability" to indicate that existence of these loops does not necessarily cause the circuit to lose its absolute stability, rather, it may increase the circuit sensitivity to noise. A noise sensitivity checking algorithm called Loop Finder has been proposed and developed efficiently [1]–[3], which automatically picks up the noise-sensitive loops in an analog circuit modeled by a linear time-invariant (LTI) system model.

However, many practical circuits, such as switchedcapacitor filters and mixers, have periodic time-varying behaviors. For the first time, we take an in-depth look into the marginal instability of time-varying analog circuits using a rigorous linear periodically time-varying (LPTV) system model. We characterize the marginal instability of LPTV circuits based on LPTV impedance transfer functions extracted for all circuit nodes. We define the new concepts of *noisesensitive pole groups* and *noise-sensitive loops* for LPTV circuits. Finally, we propose an algorithm for efficient identification of multiple noise-sensitive loops, which incorporates a graph building algorithm and a maximum loop finding algorithm. Capable of analyzing more general LPTV systems, the proposed algorithm unifies the solution to loop-based noise sensitivity analysis for both LTI and LPTV circuits.

II. NOISE-SENSITIVE LOOP IDENTIFICATION FOR LINEAR TIME-INVARIANT CIRCUITS

We first briefly introduce the noise-sensitive loop identification approach for LTI circuits [1]–[3]. The small-signal transfer function H(s) of an LTI circuit is described by:

$$H(s) = L^{T}(G + sC)^{-1}B,$$
(1)

where G, C, B and L are the conductance, capacitance, input and output matrix, respectively. For each circuit node, B and L in H(s) can be properly chosen to compute the scalar node impedance transfer function Z(s) as: $Z(s) = \frac{res(s)}{(s-p_1)(s-p_2)(s-p_3)\dots(s-p_n)}$, which can be further factorized: $Z(s) = \sum_{i=1}^{N_R} \frac{k_i}{s-p_i} + \sum_{j=1}^{N_C} \frac{res_j(s)}{s^2 + 2\zeta_j \omega_{0j} s + \omega_{0j}^2}$, where $n = N_R + 2 \cdot N_C$ is the order of the system. Each second-order system h_j in Z(s) has a complex pole pair $p_j = p_{j,r} \pm ip_{j,i}$ with natural frequency $\omega_{0j} = |p_j|$ and damping factor $\zeta_j = -\frac{p_{j,r}}{|p_j|}$. If $\zeta_j < 0.7$, we say that h_j is potentially noise sensitive since the impedance peaks at ω_{0j} in its frequency response, corresponding to ringing in the time domain [1]. We shall only consider potentially *noise-sensitive poles* defined as follows.

Definition 1: (Noise-sensitive poles) If a potentially noisesensitive second-order system h_j contributes the most to the node impedance at its natural frequency ω_0 among all seconder-order systems of the same impedance, each of its complex poles p_j is called a noise-sensitive pole of the circuit.

Intuitively, a pole is noise sensitive if and only if it contributes dominantly to at least one node impedance at its natural frequency. Noise-sensitive loops are found in the following way.

Definition 2: (Noise-sensitive loops) Circuit nodes sharing the same noise-sensitive pole form a noise-sensitive loop.

III. NOISE-SENSITIVE LOOP IDENTIFICATION ALGORITHM FOR LINEAR PERIODICALLY TIME-VARYING CIRCUITS

A. LPTV transfer functions

We use an LPTV transfer function H(s,t) and its Fourier expansion as the small-signal model for an LPTV circuit [5], [6]:

$$H(s,t) = \sum_{i=-\infty}^{\infty} H_i(s) e^{ji\omega_0 t},$$

$$H_i(s) = L_i^T [(G_{FD} + \Omega C_{FD}) + sC_{FD}]^{-1} B_{FD},$$
(2)

where $\omega_0 = 1/T_0$ is the fundamental frequency, $H_i(s)$ is the *i*-th harmonic transfer function with the form of (1), and the definition of each component in (3) can be found in [6].

B. Nodal harmonic impedances for LPTV circuits

Denote the impedance transfer function at a node by Z(s,t) with $Z_i(s)$ being the *i*-th nodal harmonic impedance. As in the LTI case, $Z_i(s)$ can be written as:

$$Z_i(s) = \frac{residue(s)}{(s-p_1)(s-p_2)(s-p_3)...}.$$
(4)

The poles of the circuit can be computed by solving a generalized eigenvalue problem:

$$(G_{FD} + \Omega C_{FD})X = \lambda C_{FD}X.$$
(5)

The eigenvalues λ 's are the poles and X contains the corresponding eigenvectors. Note that LPTV circuits ideally have an infinite number of poles. For practical purposes, we truncate G_{FD} and C_{FD} to retain a certain number of low-order harmonics, capturing a finite number of poles in the LPTV model. Just like in the LTI case, each $Z_i(s)$ now can be decomposed into a set of first and second order systems:

$$Z_{i}(s) = \sum_{q=1}^{N_{R}} \frac{k_{q}}{s - p_{q}} + \sum_{j=1}^{N_{C}} \frac{res_{j}(s)}{s^{2} + 2\zeta_{j}\omega_{0j}s + \omega_{0j}^{2}}$$
(6)

$$Z(s,t) = \sum_{i=-M}^{M} Z_i(s) e^{ji\omega_0 t}, \qquad (7)$$

with 2M + 1 harmonic components included.

C. Loop-based noise-sensitivity analysis for LPTV circuits

Similar to the case of LTI circuits, we first examine each (decomposed) second-order system h_j for every nodal harmonic impedance transfer function of an LPTV circuit. We say h_j is potentially noise sensitive if its damping factor $\zeta_i < 0.7$.

Definition 3: (Noise-sensitive poles in LPTV circuits) If a potentially noise-sensitive second-order system h_j contributes the most to the corresponding harmonic impedance of a circuit node at its corresponding natural frequency ω_0 among all seconder-order systems of the same harmonic impedance, its complex poles p_j are called noise sensitive for the circuit.

Time variance inherent in LPTV systems introduces frequency translation effects. Due to the *i*-th nodal harmonic impedance $Z_i(s)$ in (4), current noise with frequency ω injected into the circuit node induces a harmonic voltage response at a shifted frequency of $\omega + i\omega_0$. Such harmonics complicate the loop-based noise analysis of LPTV circuits. We illustrate the complications created by frequency translated effects through a simple example shown in Fig. 1.



Fig. 1. Noise-sensitive loops in an LPTV circuit.

Assume that zero-th order (DC) harmonic impedance $Z_0(s)$ of each node in Fig. 1 has a common noise-sensitive pole with a natural frequency of ω . This implies that current noise with frequency ω would produce a large output voltage response at same frequency at each node. Thus, these nodes can be grouped to form a "noise-sensitive loop" (black and red paths) along which there exists no frequency translation effect. Now further assume that ω is the natural frequency of a noisesensitive pole of $Z_1(s)$ of node a. Due to the frequency translation effect, noise has another way to go: the noise at frequency ω is injected to node a, producing a response at frequency $\omega + \omega_0$, which serves as the input to node b; this frequency-shifted input produces a response with a frequency back to ω , coming out of node b. This noise creation and propagation mechanism is shown by the blue path in Fig. 1. As a result, we have identified two different noise-sensitive loops through the same set of circuit nodes.

Definition 4: (Noise-sensitive pole groups in LPTV circuits) A noise-sensitive pole group is a set of noise-sensitive poles in which the difference between the natural frequencies of any two poles is an integer multiple of ω_0 .

We extend the approach of noise-sensitive loop identification for LTI circuits to analyze LPTV circuits. For each noisesensitive pole group, we find *maximum* (i.e. with the maximum number of circuit nodes) noise-sensitive loops that have two properties. First, these loops consist of circuit nodes whose noise-sensitive poles fall into the pole group. Second, when injected into some node along each such loop, current noise with a frequency same as the natural frequency of one pole in the group could propagate along the loop while creating large voltage response along the way, perhaps involving frequency translation effects.

D. LPTV noise-sensitive loop identification algorithm

The proposed noise-sensitive loop identification algorithm is run for each noise-sensitive pole group as follows:

- 1) Compute all nodal harmonic impedances.
- 2) Extract all poles and determine the potentially unstable noise-sensitive poles.
- 3) Determine the noise-sensitive pole groups for the circuit.

- 4) Build a graph for each noise-sensitive pole group; Perform maximum loop detection algorithm on each graph.
- 5) Map the maximum loops in the graph back to the noisesensitive loops in the circuit and report such loops.

IV. GRAPH BUILDING AND MAXIMUM LOOP DETECTION

We now describe the 4-th step of the above algorithm. Unlike in LTI circuits [1]–[3], frequency translation effects shall be considered for an LPTV circuit while grouping relevant circuit nodes to form noise-sensitive loops. To this end, we map a circuit to a graph G(V, E) for each noisesensitive pole group, and the mapping process ensures that the maximum loops in G can be mapped back to the circuit.

First we build a small graph for each node at each noisesensitive pole frequency in a circuit as shown in Algorithm 1. Each node in the G has three properties: type (input/output), name, frequency. We then connect each pair of input and output nodes only if they have an identical frequency.

Algorithm 1 Small graph building
procedure BUILD_SMALL_GRAPH(NODE, POLE)
Add $vi(input, node.name, \omega_{pole})$ to V
for each harmonic impedance (output freq. ω_{har}) do
if <i>pole</i> is a dominant pole for it
Add $vo(output, node.name, \omega_{har})$ to V
Add $edge < vi, vo >$ to E
end if
end for
If no vo added, delete vi
end if
end procedure

Finally, we apply a modified version of the algorithm in [8] to find maximum loops in the constructed graph G(V, E). The main idea of the algorithm is to build k-cycles from (k -1) simple paths iteratively. All the cycles in our graph have even length, which helps to shrink the search space. A list stores cycles of the maximum length detected in each iteration. The cycles left in the end are the maximum loops and are mapped back to the loops in the circuit.

A. Time complexity of the proposed method

Pole and impedance computation, which are the first two phases in our proposed algorithm, have $O([(2m + 1)N]^3)$ and $O([(2m + 1)N]^2 \times N \times num_poles \times har_num)$ costs, respectively, where N is the number of circuit nodes, and m is the number of harmonics included at each side of the DC component of node impedance. The QZ method is used for pole computation [1]. Typically, it is sufficient to set har_num to 5. More efficient model order reduction based techniques [2], [3] can be used to further speed up these two steps.

In the third phase, noise-sensitive loop identification, mapping the circuit to a graph has a low complexity. The more dominant maximum loop detection algorithm, which runs on the graph, has a worst-case complexity that is exponential in the number of circuit nodes, and can be sped up by parallel processing.

V. EXPERIMENTAL RESULTS

A C++ implementation of our algorithm has been realized on the Linux OS. We use a double-balanced mixer and a switch-capacitor (SC) gain stage designed using a commercial 90nm technology with 1.2V power supply as test cases. The search for noise-sensitive poles is limited within a broad range of [1, 10G]rad/s. We compute five harmonics including the DC component for each nodal impedance.

A. A switched-capacitor gain stage

Fig. 2 shows a switched-capacitor (SC) gain stage whose core is a two-stage opamp. The clock frequency is 1MHz. The phase margin of the opamp is 62 degrees with a load capacitor of 1pF. Our algorithm finds two noise-sensitive loops based upon two noise-sensitive pole groups in Table I. While there is no frequency translation immediately present in the identified loops, it must be noted that such analysis is only possible under the presented LPTV framework in the first place. The first noise-sensitive loop is highlighted by the blue lines in Fig. 2, containing two nodes connected to a few MOS switches. These nodes have dramatic impedance changes due to the varying magnitude of the clock signal, which defines the large periodically time-varying operating point for the circuit.



Fig. 2. A switched-capacitor gain stage and its noise-sensitive loops

TABLE I Two noise-sensitive pole groups in the SC gain stage

Name	Re	Im	Natural Freq. ω_p	ζ	
p_1	-1.147e7	1.524e7	3.035MHz	0.6015	
p_2	-1.792e9	1.860e9	408.848MHz	0.6985	

The second noise-sensitive loop is highlighted by the red lines. This loop is physically time varying because a switch is in parallel with C5. Since there is no frequency translation, we can treat this loop as if it were an "LTI" loop. The phase margin of the second-order LTI feedback model of an opamp is related to its damping factor ζ [2]. A damping factor ζ of 0.7 corresponds to a phase margin of 65 degrees. A ζ of 0.69 leads to a phase margin very close to 65 degrees but less than it. We could increment the value of C1 to 600 fF to eliminate the second noise-sensitive loop.

B. A double-balance mixer with parasitic effects

The Gilbert cell double-balanced mixer in Fig. 3 has 500MHz sinusoidal local-oscillator signals V_{LO^+} and V_{LO^+} with a peak-to-peak value of 600mV. Our algorithm finds one noise-sensitive pole group with two poles as shown in Table II. p_1 exists mainly because of the series RLC path, which models the bond wires connecting to the package. p_2 is generated by the serially connected resistor R7 and capacitor C5, representing coupling parasitics between two nodes.



Fig. 3. A double-balanced mixer and its noise-sensitive loops.

Due to many possible combinations of frequency translation effects, 97 noise-sensitive loops are identified based on the same set of eight physical nodes. The most representative loop is highlighted in Fig. 3 and is divided into two parts. The red lines are noise-sensitive at natural frequency ω_{p1} , while the blue lines are noise-sensitive at natural frequency ω_{p2} . At node c, there is a frequency translation from ω_{p1} to ω_{p2} , and the signal frequency goes back to ω_{p1} at node d.

TABLE II The noise sensitive group in the mixer

Name	Re	Im	Natural Freq. ω_p	ζ
p_1	-9.0917e8	-5.9199e9	953.23MHz	0.1518
p_2	-4.6925e9	-7.8508e9	1.456GHz	0.5130

C. Verification of noise-sensitive loops in time domain

We use the double-balanced mixer and transient simulation to provide an empirical verification of the proposed algorithm. Fig. 4(a) shows the voltage response of node b when an 1mA sinusoidal current is injected to node a. When the input frequency is around $\omega_{p1} = 953.23MHz$, as expected, large voltage fluctuations are observed along the noise-sensitive loop shown in Fig. 3. When the noise frequency is far from $\omega_{p1} = 953.23MHz$ and $\omega_{p2} = 1.456GHz$, we have smaller voltage responses, as shown for the cases of nodes b and d in Fig. 4. Since the time-domain response contains all frequency components, the voltage difference at node d may not be obvious.



Fig. 4. Noisy time-domain responses: (a) node b, and (b) node d.

D. Algorithm runtimes

Table III reports the runtimes for checking noise-sensitive loops of the two circuits, for which the most time-consuming component of the algorithm is the impedance computation.

TABLE III Run times for two circuit examples.

Circuit name	node num.	sys. size	phase1 (s)	phase2 (s)	phase3 (s)	total (s)
Double-bal. mixer	19	510	7.249	141.191	0.008	148.448
Switch-cap. gain stage	13	306	1.265	16.86	0.001	18.126

VI. CONCLUSION

We present an efficient noise-sensitive loop identification algorithm that is able to find noise-sensitive loops in LPTV circuits while capturing the essential frequency translation effects. Our algorithm has been demonstrated using a mixer and a switched-cap gain stage both of which possess inherent time-varying behaviors.

ACKNOWLEDGMENT

This material is based upon work supported by the National Science Foundation under Grant No. ECCS-1405774. This publication was also made possible by NPRP grant # NPRP 8-274-2-107 from the Qatar National Research Fund (a member of Qatar Foundation). The statements made herein are solely the responsibility of the authors.

REFERENCES

- Fang, G. P., Burt, R., and Dong, N. (2010, September). Loop finder analysis for analog circuits. In Custom Integrated Circuits Conference (CICC), 2010 IEEE (pp. 1-4). IEEE.
- [2] Mukherjee, P., Fang, G. P., Burt, R., and Li, P. (2012). Efficient identification of unstable loops in large linear analog integrated circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 31(9), 1332-1345.
- [3] Mukherjee, P., Fang, G. P., Burt, R., and Li, P. (2011, June). Automatic stability checking for large linear analog integrated circuits. In IEEE/ACM Design Automation Conference, 2011 IEEE (pp. 304-309). IEEE.
- [4] Dorf, R. C., and Bishop, R. H. (1998). Modern control systems. Addison-Wesley, Menlo Park, CA.
- [5] Phillips, J. R. (1998, November). Model reduction of time-varying linear systems using approximate multipoint Krylov-subspace projectors. In Computer-Aided Design, 1998. ICCAD 98. Digest of Technical Papers. 1998 IEEE/ACM International Conference on (pp. 96-102). IEEE.
- [6] Roychowdhury, J. (1999). Reduced-order modeling of time-varying systems. IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, 46(10), 1273-1288.
- [7] Zadeh, L. A. (1950). Frequency analysis of variable networks. Proceedings of the IRE, 38(3), 291-299.
- [8] Liu, H., and Wang, J. (2006, February). A new way to enumerate cycles in graph. In AICT/ICIW (p. 57). IEEE.