Efficient Yield Optimization Method using a Variable K-Means Algorithm for Analog IC Sizing

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***Abstract*— This paper presents the study and implementation of a new efficient yield optimization technique for multi-objective optimization-based automatic analog integrated circuit sizing. The approach uses a commercial electrical simulator and standard process design kit (PDK) models to perform, during the optimization process, the same Monte Carlo (MC) simulations that designers use. The proposed yield estimation technique reduces the number of required MC simulations by using the k-means algorithm, with a variable number of clusters, to select only a handful potential solutions where the MC simulations are performed. Due to the use of a commercial simulator tool and foundry supplied PDK models the developed methodology provides the most accurate and reliable results, and also, the variable k-means algorithm is able to achieve 91% reduction in the total number of the MC simulations required for an optimization, when considering MC simulations for all solutions. Moreover, this new approach presents a 50% increase in speed performance when comparing to a previous yield optimization technique also using k-means and MC simulations.**

Keywords*— *Analog Integrated Circuits; Electronic Design Automation; Robust Design; Yield Optimization; Monte Carlo Simulations; Clustering; K-Means

I. INTRODUCTION

Electronic design automation (EDA) tools for analog and mixed-signal integrated circuits (IC) had always followed the development of the highly developed EDA tools for its digital counterpart. The adoption of digital design techniques in analog IC world may present some advantages in automation of IC design, but in several cases as in the search for more robust and reliable solutions those techniques may be insufficient. For several years IC designers considered only global variations and tried to predict the effects of these variations on the circuit performance by using corners analysis, which is not enough to ensure that circuit performances are met on die [1]. Analog ICs are also particularly sensitive to local variations, like devices mismatch effects, especially in the deep nanometer-scale integration technologies.

The unpredictable effects caused by global and local variations may result in a large number of circuits that fail to comply with the desired circuit specifications, which may lead to an expensive redesign and refactoring processes. In order to take into account local variations, IC designers adopted Monte Carlo (MC) analysis which revealed to be the most accurate and reliable method to estimate the circuit yield, since it is based on statistical device models developed and tested by the technologies' foundries. The main drawback of the MC approach is related to the high number of simulations needed in order to provide an accurate yield estimation. The considerable amount of time needed to perform the MC simulations represents a huge bottleneck in the overall circuit synthesis process, especially, when the desirable yield is not successfully achieved and re-design is necessary.

Several approaches, in order to reduce the impact of MC in the circuit-sizing optimization process, were developed by the academia. The most common and basic technique is the Infeasible Solution Elimination, that performs MC simulation only to solutions that already comply with the desired specifications and constraints [2]. Another speedup technique allocates a different number of MC iterations to each potential solution, which depends on the solution ranking [3]. This technique may save a lot of MC iterations on worst or non-critical potential solutions. In other speedup techniques, instead of using random or pseudo-random points sampling like in the typical MC, Low Discrepancy Sequences (LDS) were adopted. The adoption of LDS sampling methods, which is usually known as Quasi Monte Carlo (QMC) methods, reaches 2x to 8x speedup with a loss around 1% in accuracy when compared to the typical MC approach [4]. The drawback of the QMC approach is the performance degradation for higher dimensionality sampling spaces. Several other works try to define models that relate the circuit performance measures with the process parameters in order to estimate the variability effects. The adopted models can go from polynomial [5] to statistical, like Kriging [6]. The problem with model-based approaches is the large setup time and limited model (re)usability for different circuits and/or technology nodes.

The main goal of this work is to implement an approach that aims to reduce the impact of the MC simulations in the circuit-sizing optimization process. The innovative approach based on MC simulations for efficient yield estimation and optimization, allows using the most accurate yield estimation method inside the optimization loop, as it is based in the foundry-provided process design kit (PDK) variation models without any tweaking or removal of random parameters. Several techniques were studied and, to assess their impact in the execution time of the optimization loop and attained solutions, they were implemented in a state-of-the-art simulation-based circuit-sizing optimization tool [7, 8], which is based on an NSGA II [9] multi-objective optimization kernel. Although the proposed approach was tested and implemented over NSGA-II, it can easily be implemented on many others metaheuristic optimization algorithms. The final adopted technique, with a variable cluster number in the k-means clustering algorithm, reveals a reduction of 91% in the total number of MC simulations required for the optimization of the presented circuit example. Tests also revealed an increase in the speed performance of 50% when compared to the work in [10].

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This paper is organized as follows. In section II, an overview of the in loop MC based Yield optimization approach is presented. In section III the problem that this work addresses is explained. In section IV two new approaches for selecting the cluster representative element are discussed. In section V, the two new methods for varying the number of clusters in the k-means algorithm are presented. In Section VI, the new approaches are tested in a real circuit-sizing optimization problem. Finally, in section VII the conclusions are drawn.

II. In-loop Monte Carlo-based Yield Optimization Overview

Metaheuristic optimization strategies are, usually, iterative algorithms based on a large number of individuals that represent potential solutions, which explore the search space towards the optimization goal. In order to guide the exploration process the potential solutions must be evaluated, which allows the optimization algorithm to identify regions of the search space where the optimal solution(s) may reside. In order to accurately evaluate the potential solutions, many state-of-the-art metaheuristics-based circuit-sizing tools adopt an electrical circuit simulator as part of the evaluation process. The proposed in-loop MC-based Yield Optimization implements a two phase electrical simulation-based evaluation process in order to classify the potential solutions, as illustrated in Fig. 1.

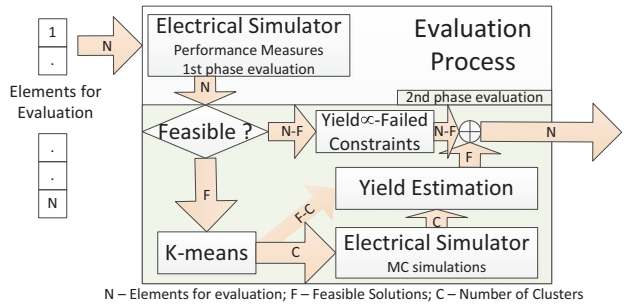

Fig. 1. Two phase simulation-based yield optimization evaluation process.

In the first phase of the evaluation process, the external electrical simulator is invoked in order to provide all electrical performance measures. Based on the performance values, the optimization problem constraints are assessed and solutions are classified as feasible or infeasible. In the second evaluation phase all infeasible solutions will have a negative yield value, which depends on how much the solution fails the problem's constraints. The assignment of a yield value, even for infeasible solutions, is essential in order to guide and accelerate the convergence of the optimization process.

Feasible solutions are clustered in the variable space by k-means [11] clustering algorithm, and each cluster representative element is sent to the electrical simulator to perform MC simulations, and therefore, estimate its yield value. Since all elements in a cluster are considered similar solutions, the optimizer will assume that all of them have the same yield value of the representative cluster element.

The implemented k-means clustering algorithm adopts the k-means++ [12] center initialization process. This method starts by randomly selecting a feasible population element as a first center. The other centers, are iteratively selected from the rest of the population elements based on a probability proportional to the distance between each element and the already selected centers. Also, the implemented k-means normalizes all the components of the clustering space, due to the nature of the circuit-sizing optimization problem where the optimization variables may have dimensions with different magnitudes.

The major difference between the implemented and the standard k-means algorithm is the choice of the cluster's representative element. In the typical k-means implementation, the representative element is usually the cluster center (or centroid), this approach was not adopted as the cluster center since it may not exist as a valid or feasible potential solution of the circuit-sizing problem. The next logical approach was choosing the closest element to each cluster center. This selection also presents a problem, as the selected element may have a higher yield value than all the other elements in the cluster, which results in the promotion of several solutions causing the appearance of a false better Pareto Optimal Front (POF). The false POF effect is shown in Fig. 2, where the blue stars represents the POF obtained by performing MC simulation in all elements of the population, while the red crosses define the POF of the same population when applying the MC simulation to the closest to cluster center solution for a 10 clusters k-means run. This effect is the result of assigning a better yield value to solutions with better objective values, i.e., better circuit performances, than the representative element.

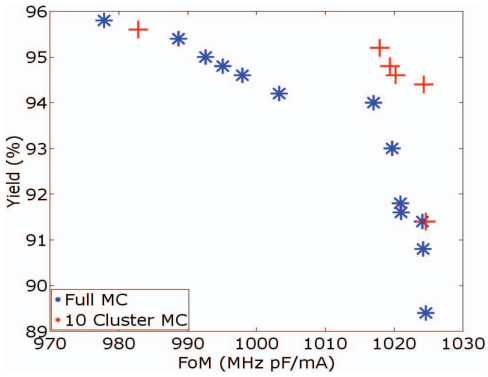

Fig. 2. False POF effect caused by selecting the element closest to the cluster center as the cluster representative element, tradeoff Yield (%) vs. Figure-of-merit (MHz.pf/mA).

In order to overcome the false POF effect, the cluster representative element considered was the one with the best objective(s) value(s). This choice assures that the selected representative element is the most likely to belong to the Pareto front, since it is the best in all objectives except the yield, since at this phase of the evaluation process the yield value is not yet available. However, selecting the dominant point as the representative element has a negative impact in the optimization, which will be addressed in the next section.

III. Problem Formulation

The adopted approach to select the cluster representative element, which was selecting the best solution in the cluster in terms of objectives, presents a problem when the specified

cluster number is relatively small compared with the number obtained by the Elbow method [13], and affects the optimization results. This problem is shown in Fig. 3, where the final POF obtained by the new approach is compared with the reference POF where all the solutions were submitted to MC simulations.

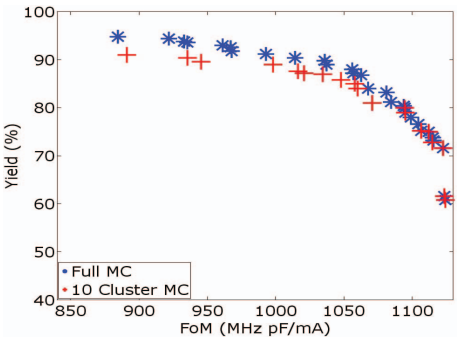

Fig. 3. Comparison between a 3-cluster yield optimization POF and the ideal POF where all the elements were submitted to MC, tradeoff Yield (%) vs. Figure-of-merit (MHz.pf/mA).

Fig. 3 reveals that in the higher yield region the two curves are moving apart, which indicates that using a smaller number of clusters in the optimization process causes that higher yield elements are discarded. The problem is caused by the projection of all the cluster elements into the yield line of the cluster representative element, since all elements in a cluster will have the same yield value of the cluster representative element. This effect is shown in Fig. 4.

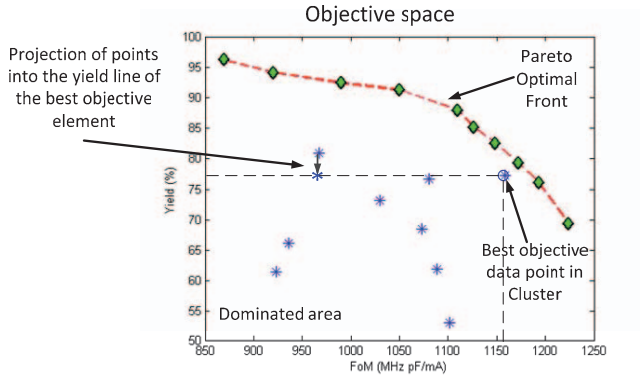

Fig. 4. Effect caused by the selection of the best objective solution as cluster representative element.

The graphic presented in Fig. 4 was extracted from an optimization run performed on the circuit presented later in the results section. The blue points represent a cluster of solutions with real yield values and the dashed red line with green diamonds defines the current POF. This example shows that when selecting the best objective data point as representative element, in this case the solution with best Figure-of-Merit (FoM), all the other data points of the cluster will be discarded by the NSGA-II since they are all dominated, even points with a better yield than the selected representative element. This fact explains the distance between the reference and the obtained POF when applying the new MC-based Yield optimization process. One solution for this problem is to increase the number of clusters, as it is shown in Fig. 5, but a large number of clusters degrade the optimization speed performance, since more MC simulations have to be performed.

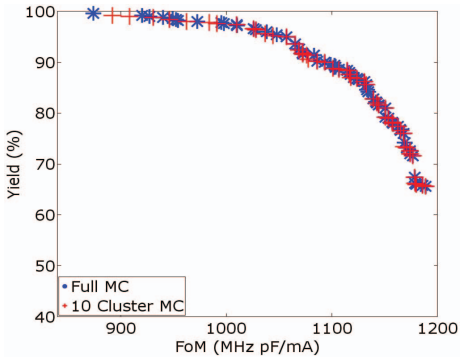

Fig. 5. Comparison between a 10-cluster yield optimization POF and the ideal POF where all the elements were submitted to MC, tradeoff Yield (%) vs. Figure-of-merit (MHz.pf/mA).

In order to solve this problem two approaches were implemented and studied. The first approach addresses the cluster representative element selection, where two new methodologies were studied, addressed in section IV. The second approach deals with the number of clusters used by the k-means algorithm, and is detailed in section V.

IV. Cluster Representative Element Selection

The first new method to cluster representative element selection is based on the idea that solutions farther from the limits that define the region of feasibility may present higher yield values. In order to implement this solution it was created a measure, which will be passed into the k-means algorithm. This new measure refers to the distance between the solution and the limits of the feasibility regions defined by the problem constraint conditions:

$$D = \sqrt{\sum_{j=1..\#\text{Constraints}} \left(m_j - G_j\right)^2} \quad (1)$$

where

- G_j is the limit value define by the j constraint of the optimization problem ($g_j(\bar{x}) \le G_j, j = 1..\#\text{Constraints}$);
- m_j is the measured value calculated by the electrical simulator that corresponds to constraint j.

Due to the fact that some constraint conditions may have a greater impact than others on (1), each measured constraint and limit value were normalized. Therefore, the cluster representative element is the solution per cluster that has the larger distance value.

An alternative method for cluster representative element selection combines the previous idea with the selection method where the best objective solution is selected as representative element. In this new method the k-means algorithm receives the optimization objective(s) values and the new distance measure (1). Those values defined an objective space with an additional dimension, defined by the distance measure. Using these values, it is possible to define an ideal point with coordinates that corresponds to the best values per objective

and larger distance measure, as illustrated in Fig. 6. Therefore, the cluster representative considered is the element closest to the ideal point.

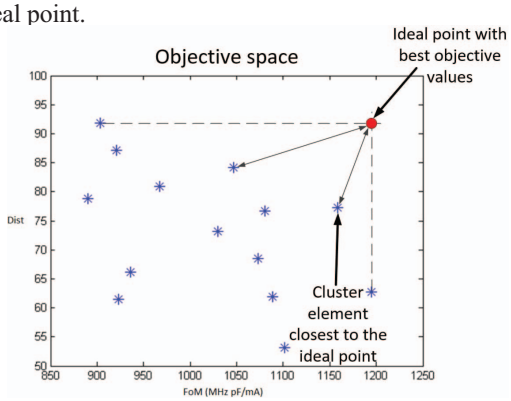

Fig. 6. Cluster representative element selection for multi-objective case.

V. K-means Variable Cluster Number Selection

One commonly used approach in order to define the best number of cluster to be applied by the k-means algorithm is the Elbow method [13]. This is a visual approach where some cost function is graphically represented against the number of clusters, and the desired number of clusters corresponds to a point where an increase in the cluster number do not correspond to a large decrease of the cost function. In this work the cost function corresponds to the cluster representation error, which is calculated as the total Euclidian distance between the points in a cluster to the cluster center.

The graphic in Fig. 7 shows the representation error for the cluster space defined by the optimization problem presented later in the results section. The cluster space dimensionality has the same size as the number of optimization variables considered in the circuit-sizing problem, which in this case is 18. Applying the Elbow method to the graphic in Fig. 7 the number of cluster is set to 10.

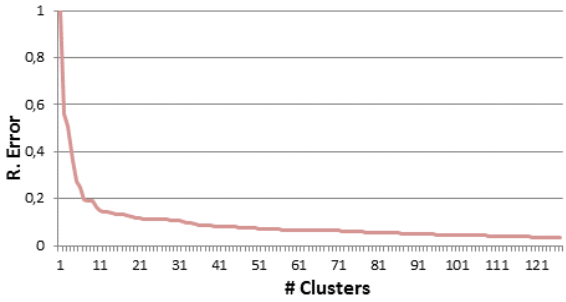

Fig. 7. Representation error as a function of the number of clusters.

Ten clusters were used in work [10], which results in savings of 75% in the total number of MC simulations. In order to decrease even further the number of MC simulations the cluster number should be lower. As it was shown in Fig. 3 a small cluster number can cause undesirable effects, so two experiments were conducted. In both approaches a variable number of clusters is defined during the optimization process, which is related to the current generation number and the maximum defined generations. These two variable cluster numbers methods are based on the same exponential function, in the first case an exponential cluster number decay (2) was used and in the second an exponential growth function (3) was adopted.

$$C_d(i) = \left\lceil C_{\max} e^{-\alpha \frac{i-f}{G-f}} \right\rceil \quad (2)$$

$$C_g(i) = C_{\max} + 2 - \left\lceil C_{\max} e^{-\alpha \frac{i-f}{G-f}} \right\rceil \quad (3)$$

where,

- $C_{\max}$ maximum number of cluster;
- α defines the rate of decay or growth;
- i current generation number;
- G maximum number of generation;
- f generation number where the first feasible solution appears;
- $\lceil x \rceil$ rounds x upward, returning the smallest integral value that is not less than x.

A graphical representation of both functions is depicted in Fig. 8.

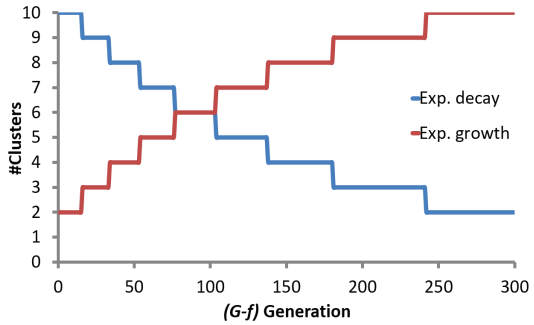

Fig. 8. Exponential decay and growth functions

The graphic of Fig. 8 assumes that the optimization process will run until the stopping criteria of 300 generations is reached (G=300) and that in the initial generation a feasible solution already exists (f=0). The other parameters are $C_{\max}=10$ due to the Elbow method and after some tests with values in the range [1, 5] the α parameter was set to 2. The approach described in this section with variable cluster number selects as the cluster representative the point with best objective(s), as described in section II.

VI. Tests and Results

In order to assess the quality of the results and compare the obtained solutions, it was necessary to define a measure that quantifies the distance between the obtained Pareto and the reference Pareto where all solutions were submitted to the MC simulations.

The new measure is the average distance between the two second order polynomial interpolation curves defined by the points in each POF. This measure corresponds to the difference of areas defined by the interpolation curve in the interval between the minimum and maximum x-values of the

interpolated points of both POF's, this idea is illustrated in Fig. 9, which is then divided by the integration range (4).

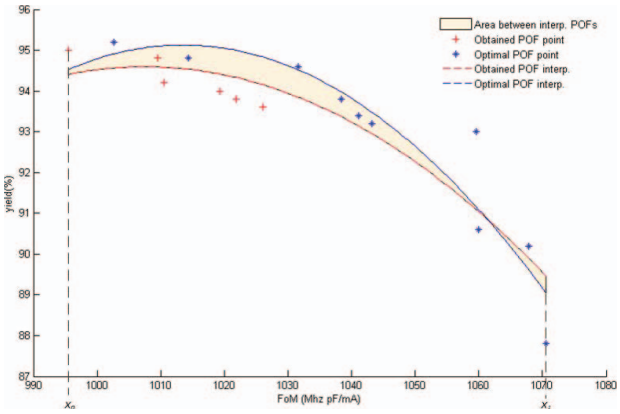

Fig. 9. Distance between two interpolated POF's

$$d_{av} = \frac{\int_{x_0}^{x_1} (p_1(x) - p_2(x))dx}{x_1 - x_0} \quad (4)$$

where,

- p_1 2nd order polynomial interpolation for the optimal POF;
- p_2 2nd order polynomial interpolation for the obtained POF;
- x_0 minimum x value between the optimal and obtained POF points;
- x_1 maximum x value between the optimal and obtained POF points;

In case (4) becomes negative ($d_{av} < 0$) the obtained and reference POF will be plotted in order to verify if the obtain solution dominates the reference POF, which only happens if the problem identified in Fig. 2 persists.

The total MC simulations reduction percentage by each method was also registered, which allows evaluating the approach in terms of computational speed.

The new approaches were evaluated in a real circuit-sizing optimization problem, i.e., a single-stage amplifier with enhanced DC gain circuit [14], whose circuit schematic is illustrated in Fig. 10. The UMC 130nm technology node was adopted for this circuit, and the two optimization goals for the circuit-sizing optimization problem, were the maximization of the Figure of Merit (5) and the yield value.

$$FoM = \frac{GBW \times C_{load}}{IDD}\left[\frac{MHz \times pF}{mA}\right] \quad (5)$$

where,

- GBW Gain-bandwidth product;
- C_{load} Load capacity;
- IDD Current consumption.

The circuit desired performance specifications and functional specifications constraints are presented in Table I. While the total 18 problem variables and respective ranges are presented in Table II.

TABLE I. PERFORMANCE AND FUNCTIONAL SPECIFICATIONS.

Performance specifications				
IDD [µA]	**GDC [dB]**	**GBW [MHz] @ C_{load} = 6 pF**	**PM [°]**	**FoM [MHz × pF / mA]**
≤ 350	≥ 55	≥ 30	≥ 65	≥ 850
Functional Specifications				
		$V_{DS} - V_{DSat}$ [mV]		**$V_{GS} - V_{TH}$ [mV]**
PMOS		≥ 70		≥ 100
NMOS		≥ 70		≥ 50

TABLE II. OPTIMIZATION VARIABLES AND RANGES

VAR	MIN	GRID UNIT	MAX
_w0, _w1, _w4, _w6, _w8, _w10	1.0e-6	1.0e-7	1.0e-4
_l0, _l1	3.0e-7	1.0e-8	9.0e-7
_nf0, _nf1, _nf4, _nf6, _nf8, _nf10	1.0	2.0	8.0
_l4, _l6, _l8, _l10	3.4e-7	1.0e-8	9.4e-7

The number of clusters for the new cluster representative element selection approaches was fixed to 10 and both variable cluster selection methods had a maximum of 10 clusters. The NSGA-II population was set to 256 individuals and the optimization process runs for 300 generations. The number of MC iterations per simulations was set to 500, considering both process and mismatch variations as defined by the foundry-provided PDK. The 500 MC iterations number results from (6) [15, 16], where the yield (Y) parameter was set to 90%, using a confidence level of 99.7% that corresponds to 3-sigma (C_σ =3) interval data model and an error of 4% (Ɛ).

$$N = \left(\frac{C_\sigma}{\varepsilon}\right)^2 Y(1-Y) \quad (6)$$

The tests were carried on virtual machine environment' running on an i7-3770 Intel© CPU with 16GB of RAM, which allows performing multiple and different optimization runs at the same time. At the end of the tests the best approach was selected to run on the standalone server, in order to assess execution times in a regular working environment.

The results for 5 runs on each approach are presented in Table III. All the approaches except the exponential decay presents negative values for the average distance, which potentially reveals the existence of the false POF error identified in Fig. 2. After plotting the POF's it is observed that only the "Large Distance" approach presents a great effect of the false Pareto, which led to abandon this method after 3 runs.

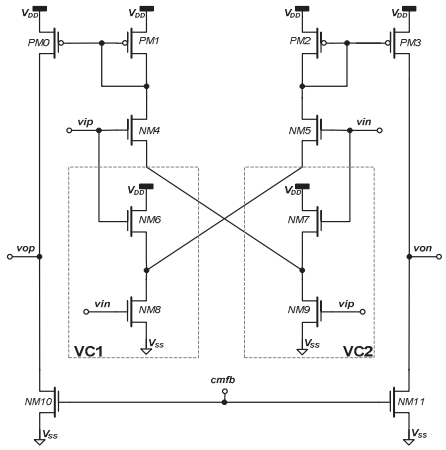

Fig. 10. Single-stage amplifier with enhanced DC gain schematics.

TABLE III. AVERAGE RESULTS FOR THE TESTED METHODOLOGIES.

Approach	Average Distance to ideal POF			Avg. MC reduction
	Min.	Avg.	Max.	
Best Objective	-0.0164	0.0307	0.0774	74.7%
Large distance	-4.393	-1.3263	1.7405	75.8%
Best Obj. + L. Dist.	-0.3898	0.1805	0.6577	75.5%
Exp. cluster decay	0.0424	0.0974	0.1277	91.5%
Exp. cluster growth	-0.2073	-0.0238	0.0511	72,1%

The results show that the variable exponential cluster number decay presents the best results considering the total number of MC simulations reduction rate, and also, the average distance to the ideal POF is quite close to the best objective approach. Based on the results, the exponential cluster number decay method was chosen to perform the final circuit-sizing optimization on the standalone working server in order to assess execution times.

The optimization process of the best approach, reached the solutions presented in Fig. 11. The optimization process run for 300 generations, and took almost 41 minutes, which is an increase in speed performance of 50%, when comparing to [10].

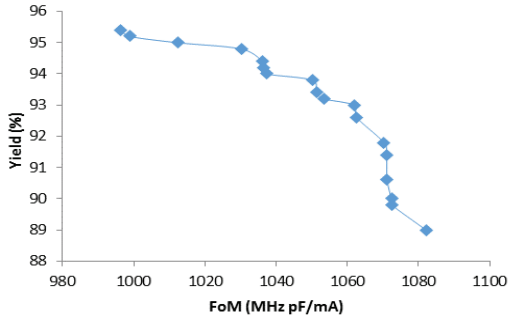

Fig. 11. Final Pareto front for the variable cluster yield optimization process.

The obtained POF shows a set of solutions that reached a maximum yield of 95.4% with a FoM of 996Mhz pF/mA and a minimum yield of 89% for a FoM of 1082 Mhz pF/mA. The final solution presents a POF with fewer points than the work in [10], but with higher values both in yield and FoM.

The new variable cluster number yield optimization process takes the same time as the 4-corners optimization process for the same circuit-sizing problem, and with the advantage of offering a more suitable approach to optimize and obtain more robust solutions for the analog circuit-sizing problem.

VII. CONCLUSION

In this work several different approaches were presented, in order to reduce the negative impact of the MC simulations in the optimization loop. The test results have shown that, by using the new implemented variable cluster exponential decay in the k-means algorithm, it was possible to achieve an average reduction of 91% in the total number of performed MC simulations needed to evaluate the full NSGA-II population, and furthermore, a speedup of 50% of the optimization process in comparison with a previous method. The low impact on the computational time of the traditional optimization-based sizing offers IC designers' the possibility of performing yield optimization with the most accurate yield estimation method, MC simulations using foundry statistical device models considering local and global variations.

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