

BISCC: Efficient Pre Through Post Silicon Validation of Mixed-Signal/RF Systems Using Built In State Consistency Checking

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Abstract: High levels of integration in SoCs and SoPs is making pre as well as post-silicon validation of mixed-signal systems increasingly difficult due to: (a) lack of automated pre and post-silicon design checking algorithms and (b) lack of controllability and observability of internal circuit nodes in post-silicon. While digital scan chains provide observability of internal digital circuit states, analog scan chains suffer from signal integrity, bandwidth and circuit loading issues. In this paper, we propose a novel technique based on *built-in state consistency checking* that allows both pre as well as post-silicon validation of mixed-signal/RF systems without the need to rely on manually generated checks. The method is supported by a design-for-validation (DfV) methodology which systematically inserts a minimum amount of circuitry into mixed-signal systems for design bug detection and diagnosis purposes. The core idea is to apply two *spectrally diverse* stimuli to the circuit under test (CUT) in such a way that *they result in the same circuit state* (observed voltage/current values at internal or external circuit nodes). By comparing the resulting state values, design bugs are detected efficiently *without the need for manually generated checks*. No assumption is made about the nature of the detected bugs; the stimulus applied is steered towards those that are the most likely to detect design bugs. Test cases for both pre and post-silicon design bug detection and diagnosis prove the viability of the proposed BISCC approach.

I. INTRODUCTION

Aggressive scaling of device technology has enabled massive integration in today's integrated circuits. Though large scale heterogeneous integration has helped in incorporating newer features and functionality in the same die area, state of the art SoC's pose daunting test and validation challenges. Pre-silicon, a key challenge is to identify design bugs rapidly without the need to rely on human generated assertions for design validation. Post-silicon, the low controllability and observability of internal circuit nodes in modern SoCs poses a significant challenge. Besides logical bugs, difficult-to-simulate electrical bugs that cause silicon malfunction pose major validation challenges as well. Such electrical bugs due to signal crosstalk and power supply-ground bounce for example, occur under rare input stimulus conditions and are difficult to detect and diagnose. Clearly, new pre and post-silicon design validation methods are urgently needed that are completely automated and do not require the use of manually generated assertion based design checking procedures. They must provide high design bug coverage, allow detection of design bugs with low latency and facilitate diagnosis of design bugs down to

subcircuits of a large design for rapid manual analysis and redesign.

II. PRIOR WORK

Pre-silicon verification methodologies for analog/mixed signal systems can be broadly classified into three groups: i) based on equivalence checking [1] ii) based on model checking [2] and iii) based on specification testing using SPICE simulation. SPICE simulation is computationally prohibitive for AMS system verification. The main drawbacks of the state of the art validation techniques employing i) and ii) are: (a) assertions for checking design correctness are hand crafted and require input from experienced analog designers, (b) only very simple properties and specifications of AMS circuits and systems can be handled. Fault isolation and diagnosis are not addressed adequately by state of the art AMS verification methodologies and is largely solved by manual simulation. Further pre-silicon verification techniques discussed above are not readily amenable to mixed-signal/RF post silicon validation.

With regard to post-silicon validation, scan chains are popular in digital design for providing state observability and controllability that aid circuit debugging. . Although the analog scan standard IEEE 1149.1/1149.4 [3, 4] is in practice for board level debugging, it has not found widespread application in circuit level testing of analog/RF IP blocks in SoCs. All the above scan based test methods suffer from the inability to test AMS circuits and systems at-speed, where they are most vulnerable to design bugs.

In contrast, analytical model based analog/RF post silicon validation has been proposed in [5, 6] and model learning based diagnosis in [7]. A key issue with model driven validation is that the nature of complex design bugs is generally not known a-priori and the "difficult" electrical bugs due to coupling and ground bounce, for example, cannot be easily simulated.

With regard to test stimulus generation, there has been research on test generation driven validation in the digital space [8, 9]. However, there is not much parallel work in the mixed-signal/RF domain. In [10, 11], the authors use *diverse programs* with the *same functionality* to detect design bugs in processor cores, uncore components and accelerators. A hardware design bug is detected if there is any inconsistency in the results obtained from the two functionally equivalent program streams. The test procedure does not make any assumption about the nature of design bugs and the extent of design bugs uncovered is limited only by the diversity of test programs deployed.

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In our proposed approach, a reference model of an AMS system is used to design spectrally diverse test stimulus for the system or module under test. The analogy to the work of [11], is that in the latter, program diversity is dictated by the instruction set architecture (ISA) of the processor being debugged (reference model). The diverse stimuli are designed to take the circuit under test from a known initial condition to the *same final state* (measured voltage/current values at specified circuit nodes). The final states reached by the two diverse stimuli, applied in sequence, are acquired using track-and-hold circuitry (see Figure 1, the comparison results are scanned out using digital scan chains). By checking for consistency between the final states reached by the diverse test stimuli, design bugs are detected with low latency and high coverage (see Figure 1). As in [11], no assumption is made about the nature of design bugs detected (models for hard design bugs are developed only *after* they are detected with considerable debug and bug modeling effort).

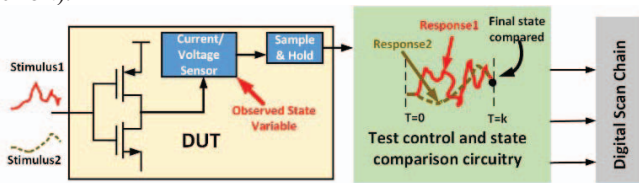


Figure 1: State Consistency Checking Based Validation of Mixed-Signal/RF Systems

The main contributions of this work are as follows:

1. *The proposed BISCC approach for design debug is a unified methodology for pre and post-silicon validation of AMS/RF systems and can be applied seamlessly through the design process with appropriate modifications.*
2. *The design validation approach of BISCC does not rely on the use of manually generated assertions in the AMS domain (that are prone to errors) for design checking. In contrast, it can automatically check for design bugs, even bugs whose effects are unknown prior to circuit debugging.*
3. *BISCC uses short test sequences for detecting bugs that require very low test application time.*
4. *For post-silicon debug, the BISCC methodology entails the use of minimal on-chip hardware (as compared with other analog/RF DFT techniques [4-6, 12]). Moreover, following from this simplicity, the use of multiple voltage and current test points allows localization of design bugs to specific design modules for system debug.*

The rest of the paper is organized as follows: section III describes the underlying basic principles of analog state consistency checking based debugging. DFX infrastructure placement algorithms are discussed in section IV. Analog signal capturing and comparing DFT circuits are explained in section V. Simulation results to corroborate the proposed claim are shown in section VI. Finally future possible work and conclusion are given in section VII.

III. DEBUGGING USING ANALOG STATE CONSISTENCY CHECKING

A. Analog State Space Model (ASSM) Representation

A formal definition of state variable and state consistency is given in Table 1. Intrinsic as well as parasitic

device/interconnect resistance, capacitance and inductance make any RF/Analog circuit a state machine. Number of possible states in such state machine is infinite as analog currents/voltages can take any values within the dynamic range. Here any branch current or node voltage can be thought of as state variable of the system.

Table 1: Formal Definitions of State Variable and State Consistency

	<i>Definition</i>
<i>State Variable (SV)</i>	<i>Any observed node voltage or branch current is a state variable. $SV \in \mathbb{R}$ and $R_{i1} < SV_i < R_{i2}$ Where (R_{i1}, R_{i2}) is the dynamic range of the observed current/voltage corresponding to state variable i.</i>
<i>State Consistency</i>	Temporal Consistency: <i>Two state values SV_i^1 and SV_i^2 of state variable SV_i will be consistent with each other if $SV_i^1 - SV_i^2 < \epsilon$ where ϵ is comparator offset voltage</i> Spatial Consistency: <i>Two state values SV_i^1 and SV_j^1 of state variables SV_i and SV_j will be consistent with each other if $SV_i^1 - SV_j^1 < \epsilon$ where ϵ is comparator offset voltage</i>

B. State Consistency Checking Approach:

Type I Test (Temporal State Consistency Checking): In our approach a piecewise linear stimulus of duration T is crafted across a time grid of spacing δ and N grid points where $T = N\delta$ (see Figure 2). At time $t=T$ the final value of the state variable SV in response to stimulus $S1$ is sampled and held using a sample and hold (S/H) circuit for additional time T . Between time $t=T$ to $t=2T$, a different stimulus $S2$ is applied to the DUT starting with the same initial condition as in $S1$. Final value of the state variable SV in response to $S2$ is acquired at $t=2T$ using a S/H circuit. Subsequently the sampled values of SV at $t=T$ and $t=2T$ in response to the applied stimuli $S1$ and $S2$ respectively, are compared. If they are consistent (see Table 1 for consistency definition) then a logic “0” is generated by the error triggering circuit (see Figure 1) else a logic “1” is generated.

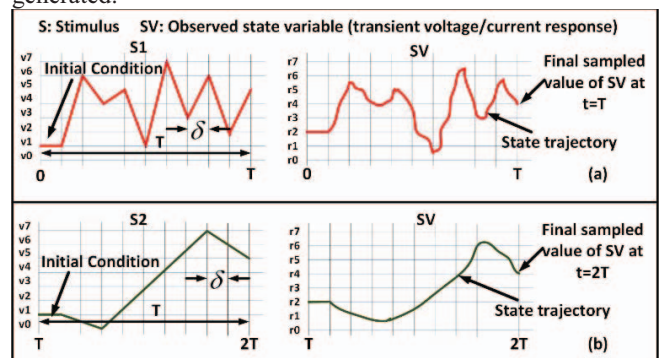


Figure 2: Temporal State Consistency

The core idea behind temporal state consistency checking is to design the stimuli $S1$ and $S2$ in such a way that they are diverse (exercise the analog/RF circuit through diverse state trajectories) but result in consistent final states sampled at $t=T$ and $t=2T$. This leads to the hypothesis that an arbitrary design bug or fault is unlikely to affect the state trajectories of SV in response to $S1$ and $S2$ identically and thereby results in inconsistent final state values.

Type II Test (Spatial State Consistency Checking): Type II tests are designed to check consistency across state variables at same sampling instant as opposed to type I test where state consistency of a state variable is checked between two different sampling instants. A stimulus will be generated so that the two observed state variables are consistent (see consistency definition in Table 1) for nominal circuit at sampling instant $t=T$ (see Figure 3). It is to be noted that two observed state variable pair may be having different dynamic ranges, so proper level shifting and gain compression are required before comparison. There are some pathological cases such as gain compression, DC offset where the faulty circuit may show state consistency under type I stimuli test. To catch these faults we introduce type II test, where state consistency across state variables are checked.

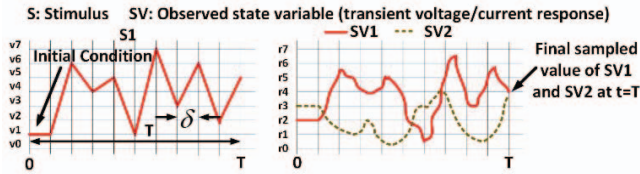


Figure 3: Spatial Consistency Checking

IV. DFX INFRASTRUCTURE PLACEMENT

How many state variables are needed to diagnose a system, and which ones to be cherry picked will be discussed in this section. Every state variable is observable in pre-silicon stage. DFX structures are to be placed in design to make selected state variables observable in post-silicon stage. In simulation we select all possible non-intrusive DFX sensor positions in the system, and for a long random stimulus collect sensor data from respective sensors. We will keep those sensors that are volatile based on a threshold volatility. Higher the volatility, richer the sensor is with information about the system. As the dynamic ranges of the all the sensors are not same, we have used a scale free volatility measure given in equation 1.

$$volatility = \frac{standard\ deviation}{mean} \quad (1)$$

Let's assume that the type I test set be SVS1 and is shown in equation 2.

$$SVS1 = \{SV_1, SV_2 \dots SV_k\} \quad (2)$$

For type II test we check state consistency between a pair of state variables at same sampling instant. From type I test set, we constitute pairwise variable set (as shown in equation 3) and compare cross correlation between every pair.

$$(SV_i, SV_j) \text{ s.t } i \neq j \text{ and } i, j = 1(1)k \quad (3)$$

In a circuit the observed state variable pair may be phase shifted. For cross correlation enumeration matlab function "xcorr" is used. $xcorr(x1, x2)$ finds cross correlation between $x1$ and $x2$ at every shifted position of $x1$ and $x2$. Maximum of all shifted cross correlation serve as a metric to pick state variable pair.

V. DEBUG HARDWARE

In post-silicon validation, internal current/voltages are accessed by signal capturing circuits. In RF transceiver envelop detector is used to capture low frequency signature from modulated voltage signal. For supply current sensing a small resistance R_{sense} is used to convert supply current to voltage (see Figure

4b). Further amplification and low pass filtering are done by the op-amp and low pass filter respectively.

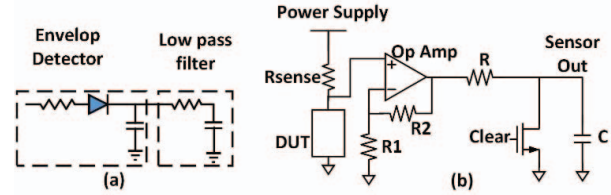


Figure 4: (a) Low Frequency Voltage Signal Capturing Circuit for RF Receiver (b) Supply Current Sensor

Two types of error trigger architectures are shown in Figure 5. Temporal architecture is used to compare between previously sampled value and present sampled value. A sample & hold circuit is used to hold the previously sampled value. For spatial comparison as the comparing signals are coming from two different circuit nodes, no such holding is required.

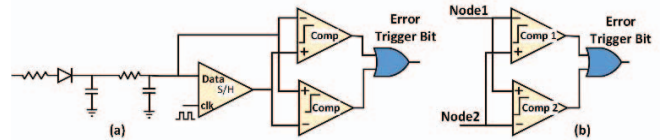


Figure 5: (a) Temporal Error Trigger DFT Architecture (b) Spatial Error Trigger DFT Architecture

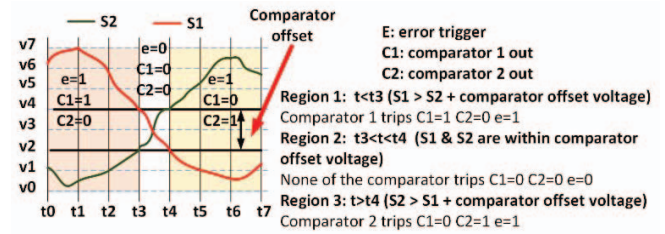


Figure 6: Error Trigger Operation

The error triggering mechanism is shown in Figure 6.

VI. SIMULATION RESULTS

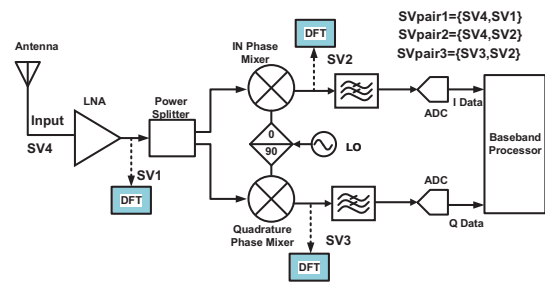


Figure 7: RF SISO Receiver

In this work RF receivers (SISO and MIMO) are used as test vehicles to corroborate the efficacy of the proposed state consistency checking based validation methodology for mixed signal/RF systems. RF quadrature receiver systems are designed in 130nm IBM process. The LO frequency of the designed receiver is 2.4GHz and the in phase and quadrature phase data rate is 1 MHz.

Pre-Silicon Test Cases (RF SISO Receiver):

Test Case 1 & 2: Faulty In Phase Mixer (Bias Voltage Variation): In AMS/RF systems bias voltages/currents are

generally controlled digitally. Two pathological test cases are created where bias voltage of the In Phase Mixer is varied (5% for test case 1 and 10% for test case 2) by supplying wrong digital codes. Other design and process parameters were not altered. Diagnostic results (see Table 2) shows that the state variables associated with In Phase Mixer causing more bit flips than the others.

Table 2: Pre-Silicon Validation Results of RF Receiver (*SV : State Variable)

	Percentage of bits flipped triggering error			
	Test Case 1	Test Case 2	Test Case 3	Test Case 4
Type I Test 1 (SV1)	5.1	5.3	11	12
Type I Test 2 (SV2)	52.1	68.0	83	25
Type I Test 3 (SV3)	23.1	30.1	80	34
Type I Test 4 (SV4)	4.8	5.0	13	15
Type II Test 1 (SV pair 1)	12.1	13.3	80	71
Type II Test 2 (SV pair 2)	14.8	13.8	83	68
Type II Test 3 (SV pair 3)	46.6	73.3	90	76

Test Case 3 & 4: DC offset and Gain Variation: We created two more pathological test cases 1) introduced DC offset in LNA output (test case 3) and 2) gain of In Phase Mixer is increased by changing design parameters (test case 4). Type I test fails in these two pathological cases. All type II tests catch these faults easily (see Table 2).

Post-Silicon Test Cases (RF MIMO Receiver): signal coupling, noise coupling and supply voltage variation form the majority of the electrical post-silicon bugs. Using two chains of RF receivers (shown in Figure 7), a 2x2 MIMO receiver is formed. As shown in Figure 8, a coupling fault is forced by introducing a capacitance between LNA outputs of the chains. Conventional specification testing (EVM testing) will not catch this bug, although it will show up in actual operation and will corrupt received MIMO data. If EVM testing is done in SISO mode sequentially, the coupling bug will not be activated. Even if the two chains tested concurrently (required two sets of costly RF test instruments), the bug will not show up unless the two chains carry different symbols. How BISCC catches this bug is shown in Table 3.

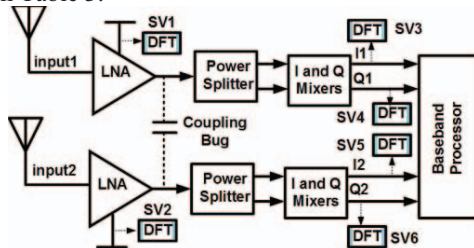


Figure 8: 2x2 MIMO Receiver

BISCC test methodology has been applied to various other kinds of circuits such as sigma delta ADC and DAC, analog biquad filter, analog comparator, sense amplifier etc. We could not show all the test cases in this paper due to limited space. We have considered variety of fault cases, process parameter variation, temperature variation, resistive/capacitive opens and shorts, electrical bugs, logical bugs. In almost all cases BISCC has uncovered the fault with great accuracy.

Table 3: Post-Silicon Validation Results of RF Receiver (*SV : State Variable)

	Percentage of bits flipped triggering error
Type I Test 1 (SV2)	89
Type I Test 2 (SV4)	91
Type I Test 3 (SV6)	92

VII. CONCLUSIONS AND FUTURE WORK

The authors have presented BISCC, a novel low cost, quick validation technique for embedded AMS/RF systems. Observability is a key issue in post-silicon debug of deeply embedded analog/RF system. With on chip signature capturing and temporal and spatial signature comparing infrastructure, the authors present a built in self-validate methodology for RF/analog systems. BISCC is equally applicable to pre-silicon hierarchical model equivalence checking between a high level design and a low level transistor netlist. Vdd ramping technique discussed in [12] for mixed-signal/RF validation is an orthogonal approach to the proposed scheme of this work. The authors would like to fuse Vdd ramping into the proposed scheme in future.

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