DATE BEST PAPER AWARDS

Each year the Design, Automation and Test in Europe Conference presents awards to the authors of the best papers. The selection is performed by the award committee.

The **DATE 2017** best papers are:

D Track

Automatic Place-and-Route of Emerging LED-Driven Wires within a Monolithically-Integrated CMOS+III-V Process

Tushar Krishn [3], Arya Balachandran[1], Siau Ben Chiah[2], Li Zhang[3], Bing Wang[3], Cong Wang[2], Kenneth Lee Eng Kian[3], Jurgen Michel[4], Li-Shiuan Peh[4]
1 Georgia Institute of Technology, 2 NTU, 3 SMART LEES, 4 National University of Singapore

A Track

CoSyn: Efficient Single-Cell Analysis Using a Hybrid Microfluidic Platform

Mohamed Ibrahim[1], Krishnendu Chakrabarty[1] , Ulf Schlichtmann[2]
1 Duke University, 2 Technical University of Munich

T Track

Fast and Waveform-Accurate Hazard-Aware SAT-Based TSOF ATPG

Jan Burchard[1], Dominik Erb[1], Adit D. Singh[2], Sudhakar M. Reddy[3], Bernd Becker[1]
1 University of Freiburg, 2 Auburn University, 3 University of Iowa

E Track

MoDNN: Local Distributed Mobile Computing System for Deep Neural Network

Jiachen Mao[1], Xiang Chen[2], Kent W. *Nixon[1], Christopher Krieger[3], Yiran Chen[1]*
1 University of Pittsburgh, 2 George Mason University, 3 University of Maryland

BEST PAPER AWARD NOMINATIONS

D track

Sampling-Based Binary-Level Cross-Platform Performance Estimation
Xinnian Zheng, Haris Vikalo, Shuang Song, Lizy K. John, Andreas Gerstlauer
The University of Texas at Austin

Optimizing Temperature Guardbands
Hussam Amrouch[1], Behnam Khaleghi[2], Joerg Henkel[1]
1 Karlsruhe Institute of Technology, 2 Sharif University of Technology

Performance Impacts and Limitations of Hardware Memory-Access Trace Collection
Nicholas C. Doyle[1], Eric Matthews[1], Graham Holland[1], Alexandra Fedorova[2], Lesley Shannon[1]
1 Simon Fraser University, 2 University of British Columbia

Reliability Assessment of Fault Tolerant Routing Algorithms in Networks-onChip: An Analytic Approach
Sadia Moriam and Gerhard Fettweis
TU Dresden

STAxCache: An Approximate, Energy Efficient STT -MRAM Cache
Ashish Ranjan[1], Swagath Venkataramani[1], Zoha Pajouhi[1], Rangharajan Venkatesan[2], Kaushik Roy[1], Anand Raghunathan[1]
1 Purdue University, 2 NVIDIA Research

Shared Last-level Cache Management for GPGPUs with Hybrid Main Memory
Guan Wang, Xiaojun Cai, Lei Ju, Chuanqi Zang, Mengying Zhao, Zhiping Jia
Shandong University

An Efficient Leakage-Aware Thermal Simulation Approach for 3D-ICs Using Corrected Linearized Model and Algebraic Multigrid
Chao Yan[1], Hengliang Zhu[1], Dian Zhou[2], Xuan Zeng[1]
1 Fudan University, 2 University of Texas at Dallas

Automating the Pipeline of Arithmetic Datapaths
Matei Istoan[1] and Florent de Dinechin[2]
1 INRIA, 2 INSA-Lyon

A Field Programmable Transistor Array Featuring Single-Cycle Partial/Full Dynamic Reconfiguration
Jingxiang Tian, Gaurav Rajavendra Reddy, Jiajia Wang, William Swartz Jr., Yiorgos Makris, Carl Sechen
The University of Texas at Dallas

Hybrid VC-MTJ/CMOS Non-volatile Stochastic Logic for Efficient Computing
Shaodi Wang, Saptadeep Pal, Tianmu Li, Andrew Pan, Cecile Grezes, Pedram Khalili-Amiri, Kang L. Wang, Puneet Gupta
University of California, Los Angeles

A track

Embracing Approximate Computing for Energy-Efficient Motion Estimation in High Efficiency Video Coding

Walaa EI-Harouni, Semeen Rehman[1], Bharath Srinivas Prabakaran[1], Akash Kumar[1], Rehan Hafiz[2], Muhammad Shafique[3]
1 TU Dresden, 2 National University of Science and Technology Islamabad,
3 Vienna University of Technology (TU Wien)

Adaptive Compressed Sensing at the Fingertip of Internet-of-Things Sensors: An Ultra-Low Power Activity Recognition

Ramin Fallahzadeh[1], Josue Pagan Ortis[2], Hassan Ghasemzadeh[1]
1 Washington State University, 2 Complutense University of Madrid

On Reducing Busy Waiting in AUTOSAR via Task-Release-Delta-based Runnable Reordering

Robert Höttger[1], Burkhard Igel[1], Olaf Spinczyk[2]
1 FH-Dortmund, 2 TU-Dortmund

Static Power Side-Channel Analysis of a Threshold Implementation Prototype Chip

Thorben Moos, Amir Morad, Bastian Richter
Ruhr-Universitat Bochum

T track

MVP ECC : Manufacturing Process Variation Aware Unequal Protection ECC for Memory Reliability

Seungyeob Lee and Joon-Sung Yang
Sungkyunkwan University

On the Limits of Machine Learning-Based Test: a Calibrated Mixed-Signal System Case Study

Manuel Barragan[1], Gildas Leger[2], Antonio Gines[2], Eduardo Peralias[2], Adoracion Rueda[2]
1 TIMA Laboratory, 2 CSIC - Universidad de Sevilla

E Track

Scalable Probabilistic Power Budgeting for Many-Cores

Anuj Pathania[1], Heba Khdr [1] -, Muhammad Shafique[2], Tulika Mitra [3], Joerg Henkel[1]
1 Karlsruhe Institute of Technology (KIT), 2 Vienna University of Technology (TU Wien), 3 National University of Singapore