Fading memory effects in a memristor for Cellular Nanoscale Network applications

A. Ascoli, R. Tetzlaff
Institut für Grundlagen der Elektrotechnik und Elektronik, TUD, Dresden, Germany

L. O. Chua
Department of Electrical Engineering and Computer Sciences, University of California Berkeley, Berkeley, CA 94720 USA

J. P. Strachan, and R. S. Williams
Hewlett Packard Labs, 3000 Hanover Street, Palo Alto, California 94304, USA

***Abstract*—CNN based analogic cellular computing is a unified paradigm for universal spatio–temporal computation with several applications in a large number of different fields of research. By endowing CNN with local memory, control, and communication circuitry, many different hardware architectures with stored programmability, showing an enormous computing power – trillion of operations per second may be executed on a single chip –, have been realized. The complex spatio-temporal dynamics emerging in certain CNN may lead to the development of more efficient information processing methods as compared to conventional strategies. Memristors exhibit a rich variety of nonlinear behaviours, occupy a negligible amount of integrated circuit area, consume very little power, are suited to a massively-parallel data flow, and may combine data storage with signal processing. As a result, the use of memristors in future CNN-based computing structures may improve and/or extend the functionalities of state-of-the art hardware architectures. This contribution provides a detailed analysis of the system-theoretic model of a tantalum oxide memristor, in view of its potential adoption for the implementation of synaptic operators in CNN architectures.**

I. Introduction

Memristors [1] are drawing considerable attention from the research community as well as from the industry. Essentially, they are state- and input-dependent resistors. Their most popular fields of applications lie in the design of nonvolatile memories and in the development of neuromorphic systems. But this is only the beginning of the story. Infact, the rich variety of nonlinear behaviours ([2],[3]) they support may be exploited to create circuit realizations of novel computational paradigms.

Memristors exhibit attractive features, including nanoscale dimensions, ultra-low power consumption, and high switching speed. Depending on the technology adopted for their fabrication, they may also excel for other capabilities, such as off-to-on resistance ratio, retention, endurance, and negative differential resistance (NDR) effect [4].

Further, memristors are ideally suited to a massively-parallel signal processing paradigm, given the classical multi-layer crossbar architecture which typically hosts them, naturally leading to 3D hardware structures combining CMOS and memristor technologies.

Very importantly, the use of memristors in integrated circuit design may resolve the performance bottleneck of the classical Von Neumann computer architecture [5], associated with the limited bandwidth of the data bus coupling the 2 physically-separated units responsible for data storage and signal processing, which limits the maximum operational speed of the computing engine.

Finally, the close similarity between passive memristors and biological synapses, as well as the capability of small circuits based upon locally-active memristors to reproduce the complex dynamics of neurons, are evident signatures for the potential of these devices to support the future development of bio-inspired computing architectures, including the Cellular Neural/Nonlinear/Nanoscale Network (CNN) [6].

In the CNN signal processing approach the nonlinear dynamics of identical locally-coupled cells, regularly spaced on a 2D grid[1], and ideally suited to a highly-parallel data flow, determines the time evolution of all signals in the network. CNN-based computing engines have been implemented using analog electronics from various companies, including AnaFocus, Eutecus, and Toshiba. These hardware realizations are endowed with stored programmability to enable the execution of large signal processing operations, and are usually referred to as CNN universal machines [7], since, at least in principle, may solve any problem, irrespective of its complexity. CNN are typically used in direct connection with sensor chips to enable on-line signal processing in time-critical applications, e.g. in the military sector, for industrial process control, in video-surveillance, and for bio-signal processing. The main limitation of state-of-the-art sensing-and-computing systems of this kind lies in the mismatch between the high and low resolution levels in sensor array, and CNN, respectively. In order to increase the number of cells in the CNN, smaller and lower-power devices should be employed. Memristors are therefore suitable candidates to make progress in this field. In order to unfold the full potential of these devices for CNN applications, it is necessary to gain a deep insight into their nonlinear dynamics. This manuscript presents a comprehensive analysis of the a system-theoretic model of a tantalum oxide memristor [8], in view of its potential use for the circuit realization of synaptic operators in CNN-based computing structures.

[1]A stack of 2D grids allows the accomplishment of more complex tasks, e.g. the processing of colour images.

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II. Fading memory: definition

The concept of *fading memory* was introduced by Boyd [9] back in 1985. Particularly, let us consider a n^{th}-order nonlinear system defined by

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}, u) \quad (1)$$
$$\mathbf{x}(0) = 0, \quad (2)$$

where $\mathbf{x} \in \mathbb{R}^n$ represents the state, $u \in \mathcal{C}(\mathbb{R}_+)$[2] denotes the input, and $\mathbf{f} : \mathbb{R}^n \times \mathbb{R} \to \mathbb{R}^n$ indicates the state evolution function. It is further assumed that equations (1)-(2) define an operator $\mathcal{N}$, defining how the input u applied to the given system produces a particular state response, mathematically expressed as $\mathbf{x} = \mathcal{N}u \in \mathbb{R}^n$. The operator $\mathcal{N}$ has fading memory (FM) on a set $\mathcal{K} \subset \mathcal{C}(\mathbb{R})$ if there exists a decreasing function $w : \mathbb{R}_+ \to (0, 1]$ – $\lim_{t\to+\infty} w(t) = 0$ – such that for each $u \in \mathcal{K}$ and $\varepsilon > 0$ there is a $\delta > 0$ such that for all $\tilde{u} \in \mathcal{K}$

$$\sup_{t\leq 0} |u(t) - \tilde{u}(t)| w(-t) < \delta \to |\mathcal{N}u(0) - \mathcal{N}\tilde{u}(0)| < \varepsilon \quad (3)$$

A. From fading memory to unique state solution

As explained in section II-A, the concept of FM relates the input u of nonlinear dynamical system (1) to its state x through a certain operator $\mathcal{N}$. Most interestingly, the notion of FM is strictly connected to the property of *unique steady state* for the dynamical system. In fact, it may be proved [9] that, defining the set $\mathcal{X}$ of all states corresponding to inputs in $\mathcal{K}$ as

$$\mathcal{X} = \{Nu(t) | u \in \mathcal{K}\}, . \quad (4)$$

the initial value problem (1)-(2) has a unique steady state for any input in $\mathcal{K}$ irrespective of the initial condition in $\mathcal{X}$. Denoting with $x_0\mathcal{X}$ and $\tilde{x}_0\mathcal{X}$ two distinct initial conditions, and with $x_u(t)$ and $\tilde{x}_u(t)$ the resulting solutions of equations (1)-(2) under a certain input $u \in \mathcal{K}$, the asymptotic independence of the initial condition is expressed by

$$\lim_{t\to\infty} |x_u(t) - \tilde{x}_u(t)| = 0. \quad (5)$$

III. The tantalum oxide memristor model

The tantalum oxide memristor fabricated at Hewlett Packard Labs is a voltage-controlled extended memristor [1]. Denoting with v_m and i_m the voltage across and current through the memristor, the ordinary differential equation governing the time evolution of the state x, associated to the fraction of the switching layer with higher conductivity, is given by[3] [8]:

$$\frac{d\mathbf{x}}{dt} = A \sinh\left(\frac{v_m}{\sigma_{off}}\right) \exp\left(-\frac{x_{off}^2}{x^2}\right) \exp\left(\frac{1}{1+\beta_m i_m v_m}\right) \text{step}(-v_m) + B \sinh\left(\frac{v_m}{\sigma_{on}}\right) \exp\left(-\frac{x^2}{x_{on}^2}\right) \exp\left(\frac{i_m v_m}{\sigma_p}\right) \text{step}(v_m), \quad (6)$$

if $x \in [0, 1]$, and by

$$\frac{d\mathbf{x}}{dt} = 0, \quad (7)$$

if $x \in (-\infty, 0) \cup (1, \infty)$.

Letting $u = v_m$, equations (6)-(7) are in the form established by (1)-(2). The state and input-dependent Ohm's law is expressed by

$$i_m = \left(G_m x + a \exp\left(b\sqrt{|v_m|}\right)(1 - x)\right) v_m. \quad (8)$$

where $|\cdot|$ denotes the modulus function. The presence of discontinuous and/or piecewise-differentiable functions may be at the origin of convergence issues in the numerical integration of differential algebraic equation (DAE) sets modelling memristor devices [10]. Taking this into account, robust simulations of the tantalum oxide memristor model may be obtained by introducing a continuous and differentiable approximation of the DAET set (6)-(7)-(8) [11]. Particularly, the discontinuous step function in state equation (6) is approximated by the following continuous kernel

$$l_k(v_m) = \frac{1}{1 + \exp(-k\ v_m)}, \quad (9)$$

while the piecewise-differentiable modulus function in the memductance expression within Ohm's law (8) is replaced by the differentiable kernel

$$h_\rho(v_m) = v_m \left(\frac{1}{1 + \exp(-\rho\ v_m)} - \frac{1}{1 + \exp(\rho\ v_m)}\right). \quad (10)$$

A large number of measurements covering multiple time scales and orders of magnitude were conducted on a sample device manufactured at Hewlett Packard Labs. Experimental data extracted from the measurements were used to tune the static parameters in Ohm's law (8), the dynamic parameters in state equation (6), and the kernel parameters in the exponential-based nonlinear functions given in equations (9) and (10).

IV. Memory loss effect

The tantalum oxide memristor exhibits fading memory. Stimulating the device with AC stimuli of common interest in electronics, the memory content embedded in its state progressively fades away, and, provided the excitation persists for a time interval longer than the duration of transients, is

[2] $\mathcal{C}(\mathbb{R}_+)$ is the space of bounded and continuous functions of $\mathbb{R}_+$.

[3] The signum function is denoted as $sign(\cdot)$, while $\text{step}(\cdot) = \frac{1+sign(\cdot)}{2}$ is the step function.

completely erased at steady state. In other words all solutions of the DAE model (6)-(7)-(8) have a unique asymptotic behaviour. In the recent past a considerable number of works [14] have pointed out the crucial role of the initial condition on the steady-state dynamics of ideal memristors. As a result, this history erase phenomenon in the tantalum oxide memristor, never observed earlier, is at the same time unexpected and interesting. We recently observed the emergence of fading memory effects in other non-ideal memristor devices. The conclusions of this study are reported elsewhere [15]. In this section we give evidence for the input-induced forgetting behaviour of the tantalum oxide memristor. Let us apply a voltage source of the form $v_{in} = v_{01}\sin(2\pi t) + v_{02}\cos(2\pi t)$ directly across the input terminals of the device ($v_m = vin$). In the first simulation we set $v_{01} = 0.175$ V, $f_1 = 20$ Hz, $v_{02} = -0.135$V, and $f_2 = 5$ Hz, and sweep the initial condition on the memristor state across its existence domain $[0, 1]$.

Fig. 1(a) shows the given excitation. The consequent time behaviour of the device state for initial conditions in $\{0, 0.0125, 0.0250, 0.0375, 0.0500, 0.0625\}$, and in $\{0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1\}$ are respectively reproduced in Figs. 2 and 3. After transients die out, any information contained in the initial state value $x(0)$ is lost. The system solutions differ only in the course of transients. Solutions departing from initial conditions close to the lower bound of the state existence domain are characterised by slower dynamics. Under initial state $x(0) = 0.05$, the memristor current and state response to the given input are respectively shown in Figs. 1(b) and (c), while the unique pinched hysteresis loop observed in the i_m–v_m plane is plotted in Fig. 1(d).

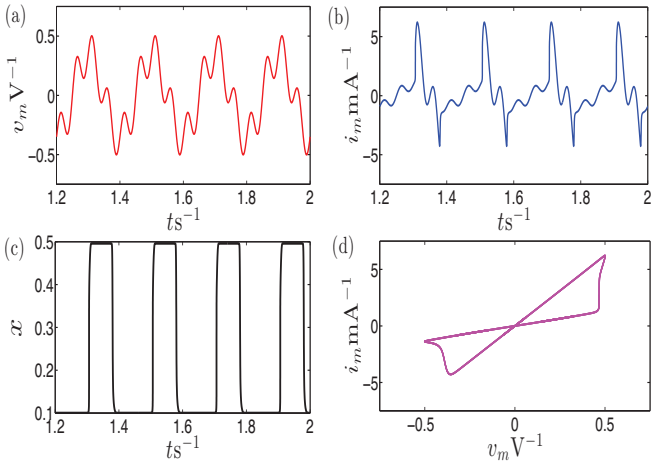

Figure 1. (a) Input voltage across the memristor, i.e. $v_{in} = v_m = v_{01}\sin(2\pi f_1 t) + v_{02}\cos(2\pi f_2 t)$, with $v_{01} = 0.175$ V, $f_1 = 20$ Hz, $v_{02} = -0.135$V, and $f_2 = 5$ Hz. Steady-state waveforms of memristor current (b), and state (c). Note that i_m and x converge to the same oscillating waveforms under all initial conditions, but the duration of transients depends on $x(0)$. (d) Unique steady-state pinched hysteresis loop in the i_m–v_m plane. Plots (b) and (c) were derived under $x(0) = 0.05$.

Let us consider another scenario. Here the voltage exciting

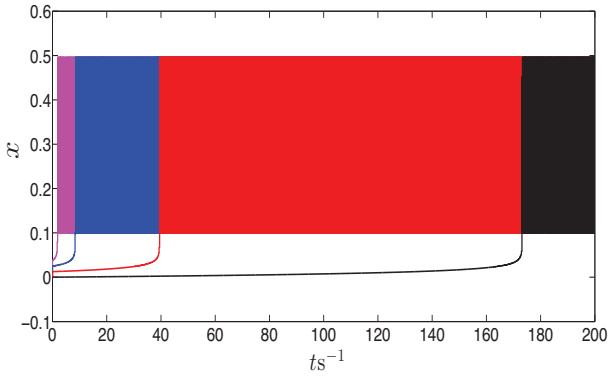

Figure 2. Slow state convergence to the unique asymptotic behaviour for $x(0)$ in $\{0, 0.0125, 0.0250, 0.0375\}$. The memory loss process is stimulated by the input of Fig. 1(a).

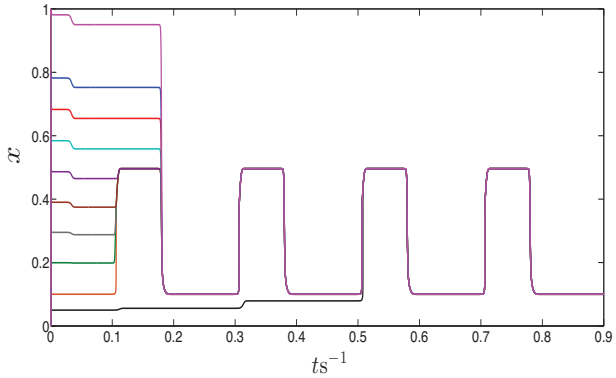

Figure 3. Fast input-induced forgetting behaviour: memristor state evolution towards a unique steady-state oscillatory solution for any initial condition $x(0)$ in $\{0.05, 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1\}$ under the input of Fig. 1(a).

the device has the same shape as in the first case study, i.e. $v_{in} = v_m = v_{01}\sin(2\pi t) + v_{02}\cos(2\pi t)$. However the parameters are now changed to $v_{01} = 0.3$ V, $f_1 = 0.3$ Hz, $v_{02} = 0.1$V, and $f_2 = 0.15$ Hz (see Fig. 4(a)). Under any initial state the given excitation leads to a progressive erase of the memory content of the device, as clear from the time evolution of the system solution, which, as observed in the first case study, is typically slower for initial conditions close to the lower bound of the state existence domain (see and compare Fig. 5 for $x(0)$ in $\{0, 0.0125, 0.025, 0.05\}$, and Fig. 6 for $x(0)$ in $\{0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1\}$. At steady state, irrespective of the initial condition, memristor current and state have unique time behaviours, as shown in Figs. 4(b) and (c), respectively. The pinched hysteresis loop observed in the i_m–v_m plane for all initial states is plotted in Fig. 4(d).

Fading memory effects appear also at high input frequencies. As an example, the input of Fig. 7(a), in the form $v_{in} = v_m = v_{01}\sin(2\pi t) + v_{02}\cos(2\pi t)$ with parameters $v_{01} = 0.175$ V, $f_1 = 600$ Hz, $v_{02} = 0.35$V, and $f_2 = 1200$ Hz, induces a progressive loss of the

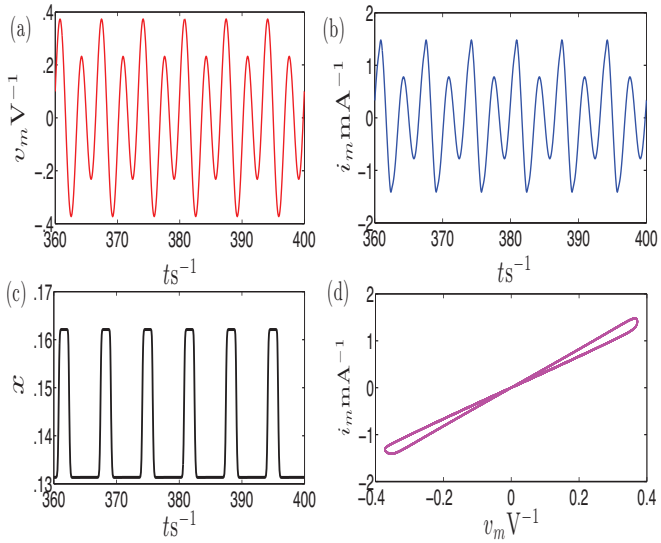

Figure 4. (a) Input inducing the memory loss effect, in the form $v_{in} = v_m = v_{01}\sin(2\pi t) + v_{02}\cos(2\pi t)$, with $v_{01} = 0.3$ V, $f_1 = 0.3$ Hz, $v_{02} = 0.1$V, and $f_2 = 0.15$ Hz. Unique asymptotic behaviour for the resulting memristor state (b) and current (c). (d) Steady-state pinched hysteresis loop observed in the i_m–v_m plane irrespective of the initial condition. Plots (b) and (c) were derived under $x(0) = 0.025$.

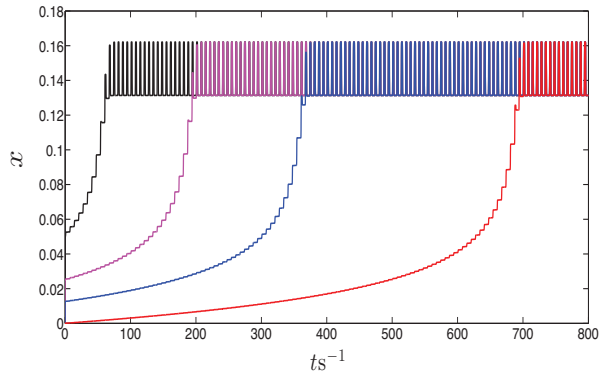

Figure 5. Slow evolution of the memristor state to the only oscillatory solution of the system for any initial condition in $\{0, 0.0125, 0.025, 0.05\}$. under the input of Fig. 4(a).

information contained in the memristor initial state. The memory erase phenomenon, slow (fast) under initial condition close to (far from) the lower bound of the state existence domain, as is evident from Fig. 8 (Fig. 9), referring to a sweep of $x(0)$ in $\{0.025, 0.0375, 0.05, 0.0625, 0.075\}$ ($\{0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1\}$), results into a unique asymptotic behaviour for memristor current and state (see Figs. 7(b) and (c), respectively). The memristor current-voltage loci recorded under any initial state is graphed in Fig. 7(d).

Experiments confirming the history erase phenomenon appearing in the tantalum oxide device were carried out at Hewlett Packard Labs. Details on these measurements are reported in [13].

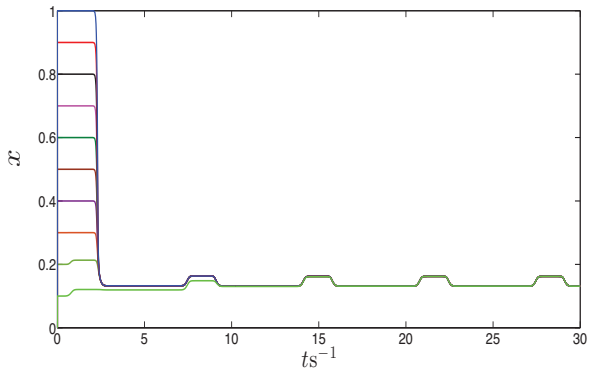

Figure 6. Fast input-induced memory loss. Memristor state convergence to a unique asymptotic behaviour for any initial condition in $\{0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1\}$. The input is reported in Fig. 4(a).

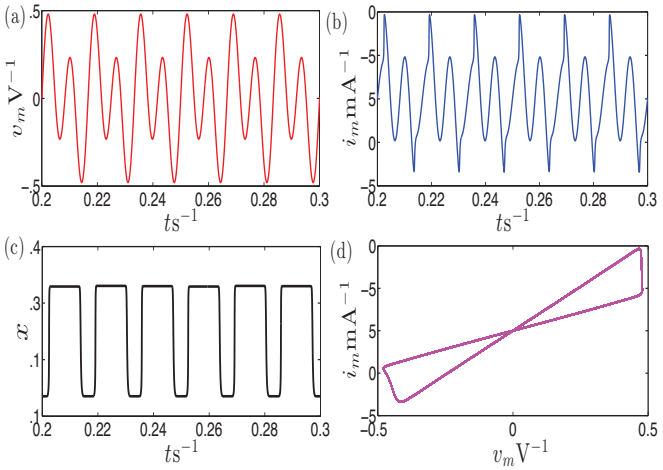

Figure 7. (a) Input voltage across the device, in the form $v_{in} = v_m = v_{01}\sin(2\pi t) + v_{02}\cos(2\pi t)$ where $v_{01} = 0.175$ V, $f_1 = 600$ Hz, $v_{02} = 0.35$V, and $f_2 = 1200$ Hz. Unique steady-state response of the device to the given input: current (b), state (c), and i_m–v_m pinched hysteresis loop (d). Plots (b) and (c) were obtained for an initial condition $x(0)$ equal to 0.1.

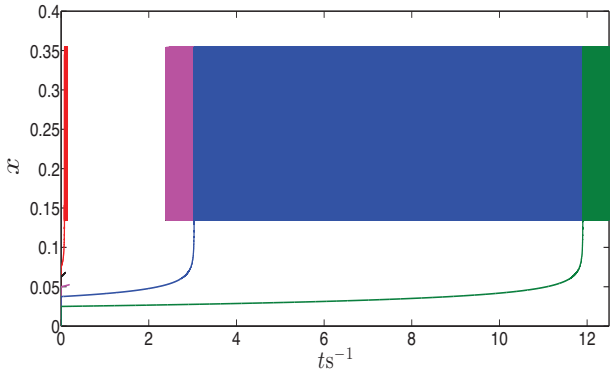

Figure 8. Fading memory in the tantalum oxide memristor under the input of Fig. 7(a). Slow dynamics for $x(0) \in \{0.025, 0.0375, 0.05, 0.0625, 0.075\}$.

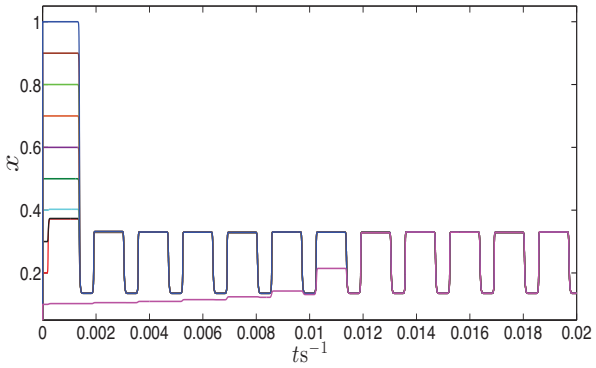

Figure 9. Fading memory in the tantalum oxide memristor under the input of Fig. 7(a). Fast dynamics for $x(0) \in \{0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1\}$.

V. Conclusions

Under AC excitation the tantalum oxide memristor state converges to a unique steady-state solution[4]. This means that the tantalum oxide memristor exhibits the fading memory property, i.e. it may be stimulated so as to forget its past history. The memory loss effect emerges in the memristor as long as the input is applied for a time interval larger than the settling time, which we may define as the duration of the transient behaviour. This is one of the major reasons why this history erase phenomenon, which is ubiquitous in real memristor devices [15], has not been noticed so far. In fact, in pulse-based programming schemes, where the device is typically driven by very short pulses of appropriate amplitude, the inputs are released before the device may attain a steady-state, thus the state perturbation depends on its initial condition. In other words the memory content stored in the two-terminal element fades away only partially, and the history erase phenomenon does not produce its full outcome. Further, despite, at least in principle, the memory erase phenomenon appears for any order of the input magnitude, under very low memristor voltages the settling time takes a very long time. Under these circumstances, we may conclude that memory loss may not be observed during the typical observation times. Finally, the frequency dependence of the history erase phenomenon needs to be commented: the effect is noticeable across the whole input frequency spectrum except at infinite frequency when the device behaves as a nonlinear resistor, and, consequently, has initial condition-dependent steady-state dynamics. It is important to point out that the fading memory property does not contradict the non-volatile memory capability. In fact, turning the device off, the memristor state abruptly stops changing, keeping the frozen value indefinitely thereafter. Therefore non volatility and fading memory coexist in the two-terminal element, which, furthermore, has all the fingerprints of a memristor, particularly

- Under any zero crossing of the voltage across the device, the current through it also has a zero crossing
- Under any periodic bipolar input, the steady-state current-voltage loci is a pinched hysteresis loop. Further
  1) As the input frequency is increased, the loop lobe area monotonically decreases
  2) As the input frequency tends to infinity, the loop lobe area converges to 0

Moreover, since in the last case, the current-voltage loci is found to be a single-valued curve, our device is an extended memristor [1]. This is further confirmed by the form of the model differential algebraic equation (DAE) set (6)-(7)-(8).

[4]Fading memory emerges also under DC input [13].

Acknowledgements

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References

[1] L. O. Chua, "Everything you wish to know about memristors but are afraid to ask," *Radioengineering*, 2015, DOI: 10.13164/re.2015.0319
[2] A. Ascoli and F. Corinto, "Memristor models in chaotic neural circuits," *Int. Journal of Bifurcation and Chaos in Applied Sciences and Engineering*, World Scientific, vol. 23, no. 3, pp. 1350052(28), 2013, ISSN: 0218-1274
[3] F. Corinto, A. Ascoli, and M. Gilli, "Nonlinear dynamics of Memristor Oscillators," *IEEE Trans. Circuits Syst.– I*, vol. 58, no. 6, pp. 1323-1336, June 2011, ISSN: 1549-8328, DOI: 10.1109/TCSI.2010.2097731
[4] A. Ascoli, S. Slesazeck, H. Mähne, R. Tetzlaff, and T. Mikolajick, "Nonlinear Dynamics of a Locally-Active Memristor," *IEEE Trans. on Circuits and Systems–I*, vol. 62, no. 4, pp. 1165–1174, 2015, DOI: 10.1109/TCSI.2015.2413152
[5] S. Kvatinsky, Y. H. Nacson, Y. Etsion, E. G. Friedman, A. Kolodny, U. C. Weiser, "Memristor-Based Multithreading," *IEEE Computer Architecture Letters*, vol.13, no. 1, pp. 41–44, 2014, DOI: 10.1109/L-CA.2013.3
[6] L. O. Chua and L. Yang, "Cellular Neural Networks: theory," *IEEE Trans. Circuits and Systems*, vol. 35, no. 10, pp. 1257-1272, 1988
[7] T. Roska, and L. O. Chua, "The CNN universal machine: an analogic array computer," *IEEE Trans. Circuits and Systems–II: Analog and Digital Signal Processing*, vol. 40, no. 3, pp. 163–173, 1993
[8] J. P. Strachan, A. C. Torrezan, F. Miao, M. D. Pickett, J. J. Yang, W. Yi, G. Medeiros-Ribeiro, and R. S. Williams, "State dynamics and modeling of Tantalum oxide memristors," *IEEE Transactions on Electron Devices*, vol. 60, no. 7, pp. 2194-2202, 2013
[9] S. Boyd, and L. O. Chua, "Fading memory and the problem of approximating nonlinear operators with Volterra series," *IEEE Trans. on Circuits and Systems*, vol. CAS-32, no. 11, pp. 1150–1161, 1985
[10] D. Biolek, M. Di Ventra, Y. V. Pershin "Reliable SPICE simulations of memristors, memcapacitors and meminductors," *Radioengineering*, vol. 22, no. 4, pp. 945-968, 2013, DOI: 10.13164/re.2013.0945
[11] A. Ascoli, R. Tetzlaff, and L. O. Chua, "Robust Simulation of a TaO Memristor Model," *Radioengineering*, 2015, DOI: 10.13164/re.2015.0001
[12] L. O. Chua, "Resistance switching memories are memristors," *Applied Physics A*, vol. 102, no. 4, pp. 765-783, 2011
[13] A. Ascoli, R. Tetzlaff, L. O. Chua, J. P. Strachan, and R. S. Williams, "History erase effect in a non-volatile memristor," *IEEE Trans. Circuits and Systems–I*, 2016
[14] F. Corinto, A. Ascoli, and M. Gilli, "Analysis of current-voltage characteristics for memristive elements in pattern recognition systems," *Int. J. Circuit Theory Appl.*, vol. 40, no. 12, pp. 1277-1320, 2012, DOI: 10.1002/cta.1804
[15] A. Ascoli, R. Tetzlaff, et al., "Fading memory in memristors," *IEEE Transactions on Circuits and Syst.*, submitted, 2015