Improving SRAM Test Quality by Leveraging Self-timed Circuits

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***Abstract*—As process technology continues to scale, SRAM test quality has become a growing concern in modern System-on-Chips. Ensuring high test quality while keeping costs low requires increasingly effective memory test solutions. This paper proposes the reuse of self-timing mechanisms that are integrated in many state-of-the-art SRAMs as a programmable DFT solution to improve the defect coverage of memory test algorithms. Its effectiveness is analyzed based on the injection of resistive-open defects inside SRAM core-cells. Simulation results of an industrial 28nm memory design show that the proposed test solution increases the coverage of studied defects by up to 30% dependent on their location, while not requiring extra circuitry inside the SRAM.**

I. Introduction

With the continuous scaling of semiconductor technology, process-parameter induced device variability and small manufacturing imperfections result in a growing number of intermittent or marginal defects in today's System-on-Chips (SoC) [1]. Static Random Access Memories (SRAMs) have highest integration densities consuming most of the transistors of a typical SoC [2] and are therefore especially sensitive to such defects.

In particular, random process parameter variations such as line edge roughness and random dopant fluctuation lead to increasing threshold voltage deviations within a SRAM core-cell and its corresponding IO circuitry. This causes asymmetric transistor strengths as well as significant variations in cell leakage currents and memory access delays, which in turn make the SRAMs more prone to parametric failures. In addition, the presence of device variability also degrades the defect coverage of various memory test sequences. For example, [3] shows that the minimum size of resistive-open defects which is detected with maximum probability doubles under variability. Hence, a large range of defects does not manifest itself as gross functional failures and might therefore escape standard tests under typical operating conditions. Thus, additional stress needs to be applied during test phase to guarantee the detection of these hard-to-detect marginal defects.

In [4]–[8], a number of DFT solutions have been proposed to detect unstable core-cells which do not fail under normal test and operating conditions but might cause failures under adverse environmental conditions or pose long-term reliability risks. They mainly rely on modifying word line and bit line voltage levels during test phase to screen out core-cells with insufficient stability margins. As these DFT solutions increase parametric test stress, they can also be applied to better sensitize marginal defects. However, these techniques have two major shortcomings. First, they do not consider that the detection of some marginal defects requires the memory to be stimulated dynamically with a test pattern such as shown for the dynamic fault class [9]. Moreover, they also disregard that the sensitization of some marginal defects depends on the state of several cells within the memory array and not solely on the core-cell under investigation. Examples for that behavior are coupling faults or the dynamic leakage read fault [10]. Thus, DFT solutions are desired which equip existing SRAM test sequences with additional parametric stresses. Second, these techniques require modifications of the SRAM design, dependent on the method even of some critical parts. For silicon area and performance reasons it is rather desirable to leverage existing on-chip circuitry for DFT purposes. These existing circuits can then impose further test stress without the need to have dedicated test circuitry in place.

In this paper, we propose and analyze a new test methodology which fulfills both of these requirements. It is based on leveraging the inherent functionality of self-timed memories to make basic read and write operations more sensitive to marginal defects during test phase. Furthermore, the proposed technique is digitally programmable allowing several stress settings to trade test quality for yield. We evaluate its effectiveness by injecting resistive-open defects in core-cells of a commercial low-power SRAM and show that it significantly improves their detection. Using this feature we then enhance the defect coverage of commonly used March test sequences to increase overall test efficiency.

The following sections start by introducing the SRAM self-timing circuitry and describing its overall impact on memory behavior. Section III presents an experimental setup to quantify its influence on resistive-open defect coverage while section IV analyzes the results. Section V shows how March test sequences can be augmented using that technique. Finally, section VI evaluates the whole methodology and concludes the paper.

II. Description of the SRAM self-timing behavior

Modern embedded memories increasingly need to operate in a wide range of supply-voltages as dynamic voltage scaling schemes are extensively employed to reduce active power consumption. This results in widely varying skews of the internal memory control signals which in turn might cause failures. To avoid overly pessimistic timing margins, memories need to automatically adapt to those timing variations. The internal

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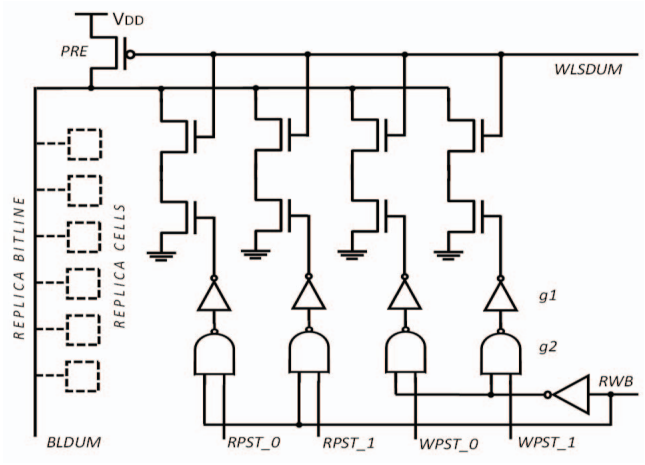

Fig. 1: A controllable SRAM self-timing circuit.

read and write control signals are therefore generated by self-timing circuits which accurately reflect changes in process, voltage and temperature (PVT) conditions. Virtually all high-performance memories are self-timed, as this technique allows for tighter timing margins while still guaranteeing robust operation. Moreover, to adapt the memory design margins depending on silicon results self-timing circuits have become configurable via the memory pins. Thus, the timing behavior of memories can also be dynamically modified at test stage and considered as a test parameter. The following section introduces these self-timing circuits and explains how they impact SRAM behavior.

A. SRAM self-timing circuits

Traditionally, internal SRAM timing signals were generated by inverter delay chains which are simple to design, however, do not accurately track the internal memory bit line discharge delay over a wide range of process and operating conditions [11]. This results in either too pessimistic timing margins or operation faults. For example, a too fast activation of the sense amplifier, i.e. before the bit lines have discharged to the desired differential level, causes read failures whereas a too slow activation leads to unnecessary longer read cycles and higher power dissipation. Simultaneously, during write operations the word line pulse also needs to be properly adjusted to trade-off write margin, performance and power.

To track the bit line discharge delay more tightly over various memory sizes and different PVT conditions, replica based self-timing techniques have been introduced [12]. They involve a so-called replica or dummy bit line mimicking the RC characteristics of conventional bit lines and have several dummy cells attached to it replicating SRAM cell load. This technique is based on the assumption that replica and conventional bit lines are equally affected by process and environmental variations. Nevertheless, the increasing effects of process variations in deep nanometer scale technologies require the flexibility to further fine-tune the memory design margins to the silicon centering. Therefore, SRAM self-timing circuits have become adjustable which allows to balance speed, power and yield.

Several implementations have been proposed [13], [14] which mainly rely on a configurable dummy bit line driver to adjust the discharge speed of the replica bit line. To understand its functioning consider Figure 1 depicting a programmable self-timing circuit as presented in [15]. It comprises a replica bit line with several replica core-cells attached to it and a programmable driver consisting of several branches of stacked NMOS transistors of different sizes to control the discharge current of the replica bit line. These devices represent the characteristics of core-cell access and pull down transistors. The PMOS device *PRE* charges the dummy bit line to V_{DD} before memory operations are performed, whereas the signal *RWB* allows to adopt its discharge time to read or write operation, respectively. Furthermore, gates *g1* and *g2* mimic the word line signal controlling the cell access transistors.

Memory operations are initiated by rising clock edges causing the SRAM control block to emit the respective control signals *WLEN* and *BLEN* (word line and bit line enable signals, respectively, which are not shown in Fig. 1 for simplicity). In case of read operations, BLEN disconnects the respective bit lines from the precharge logic, while it induces the pull-down of a bit line when the cell is written. In both cases, *WLEN* activates the corresponding word line to access the cell.

Self-timing circuits then time the end of memory operations. After emitting the *WLEN* and *BLEN* signals, the memory control block drives the *WLSDUM* signal high to initiate the discharge of the replica bit line. The *RPST* (read programmable self-timing) and *WPST* (write programmable self-timing) pins fine-tune the discharge time and make it adjustable to the respective memory operation as defined by the *RWB* signal. The *BLDUM* signal is fed back to the SRAM control block to close the timing loop. When its delayed discharged voltage reaches the target voltage level, the SRAM control block triggers the activation of the sense amplifier, the deselection of the word line and the activation of bit line pre-charge circuits. Thus, replica-based timing circuits form a closed-loop feedback control mechanism to accurately time SRAM operations which reduces their sensitivity to varying PVT conditions.

Please note that for clarity, Figure 1 depicts only four branches of stacked transistors. In practice, such circuits usually involve more branches which in turn consist of several parallel stacked transistors allowing a very accurate timing control.

B. The impact of self-timing behavior

As outlined above, the *RPST* and *WPST* pins allow a very accurate timing control of memory operations by regulating the discharge time of the replica bit line. During read operations, the *RPST* pins define the point when the sense amplifier is activated to sense the potential difference of the respective bit lines BL and BLB. A slow sense amplifier activation results in a higher differential voltage Δ BL between the bit lines which increases the longer they are exposed to the memory cell through the active word line WL. This is illustrated in Figure 2. The voltage difference Δ BL at the inputs of the sense amplifier relates directly to the reliability of the read operation and can therefore be interpreted as a measurement for the read margin of the memory. A fast sense

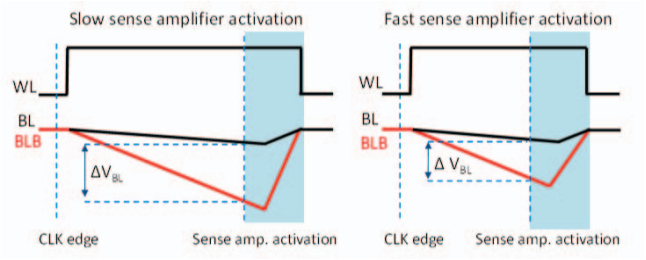

Fig. 2: The effect of the *RPST* pin setting.

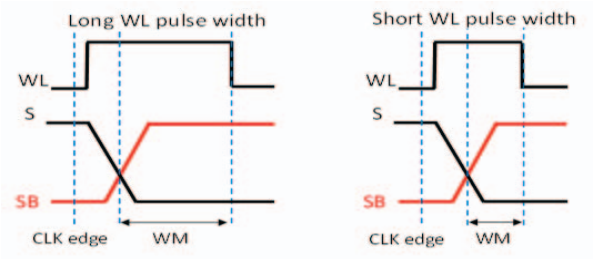

Fig. 3: The effect of the *WPST* pin setting.

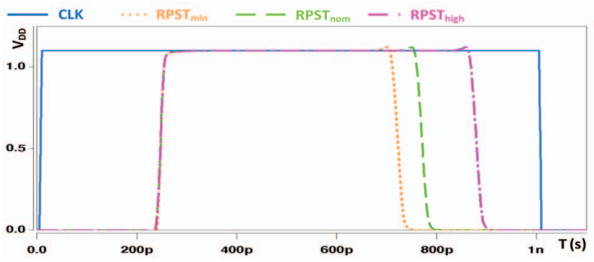

Fig. 4: A simulated word line signal under different *RPST* settings at V_{DD}=1.1V

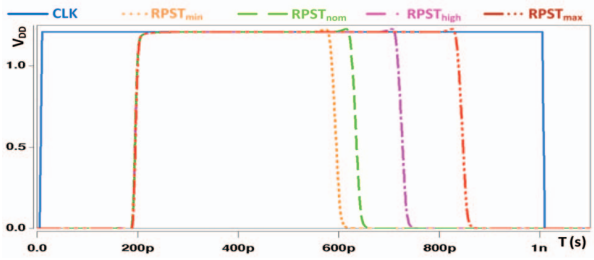

Fig. 5: A simulated word line signal under different *RPST* settings at V_{DD}=1.21V

amplifier activation reduces power dissipation as the bit lines are discharged to a lower voltage level and reduces memory access times. However, this comes at the expense of a higher risk of incorrect read faults. On the other hand, a faster sense amplifier activation reduces cell disturbances during reads, i.e. the cell is less susceptible to stability faults as less current traverses through the access transistors into the cell.

Similarly, the *WPST* pins define how long the word line WL is maintained active during a write operations. It sets the time duration in which the bit cell is exposed to the desired charged bit lines to make it flip. Based on that, the write margin (WM) is defined as the time difference between the point when the cell flip occurs and the falling edge of word line as illustrated in Figure 3. Obviously, shorter word line pulses degrade write margins and cause memory cells to be more susceptible to transition faults. However, the current flowing through the so-called half-selected cells (i.e. those on the same word line) is also lowered which in turn reduces power dissipation.

This makes clear that the *RPST* and *WPST* settings greatly impact performance, power dissipation and yield. In order to balance these conflicting requirements, the *RPST* and *WPST* settings are adjustable via pins to fine-tune the read and write margins of the memory. Using these pins, the functional memory margins are dynamically controllable. How this can be used for test purposes is further studied in the next section.

III. Experimental Setup

The setting of the self-timing circuit pins is defined based on silicon measurements during the memory characterization process and then left unchanged in the final product. In this section we consider it as an additional test parameter and analyze how and to what extend its configuration can be leveraged to enhance SRAM test efficiency.

A. Preliminaries

To better understand how the SRAM self-timing behavior can be used for test purposes, consider Figure 4. It depicts the memory clock signal and the word line signal of a core-cell for different *RPST* settings which time the activation of the sense amplifier and the subsequent deselection of the word line. Any *RPST* configuration deviating from $RPST_{nom}$ either shortens or lengthens the word line activation window by controlling its falling edge. Please note that the rising edge of the word line signal is fixed and depends on other factors such as gate delays in the row decoder.

Changing the *RPST* configuration from its nominal value $RPST_{nom}$ to $RPST_{high}$ exposes the core-cell longer to the pre-charged bit lines. This causes a higher read disturbance which in turn further stresses cell stability. On the other hand, setting the *RPST* configuration to $RPST_{min}$ decreases the internal memory cycle length and lowers the discharge time of the bit lines. This reduces the potential difference between bit line pairs making the memories more susceptible to incorrect read faults. These faults can be caused by defects within the core-cell itself as well as delays in the memory peripheral circuitry such as the sense amplifier.

To ensure correct functioning, SRAMs need to be tested at-speed i.e. at the maximum clock frequency the corresponding subsystem accesses the memory. In the case study of Figure 4, the SRAM is accessed at a frequency of 500 MHz and a supply voltage of 1.1 Volt. It can be seen that there is still margin to push the falling clock edge further towards its limit set by the internal memory cycle under $RPST_{nom}$ setting. This shows that the SRAM frequency can still be increased or, equivalently, there is still room to extend the word line activation window during test phase. On the other hand, it might be well the

case that the SRAM itself operates at its maximum speed and constrains the operating frequency of the whole subsystem. In that case the *RPST* setting cannot further stress cell stability under nominal operation conditions.

However, in test phase extensive voltage guard-bands are applied to account for variations in test equipment and to ensure reliable chip functioning throughout its lifetime. The inherent property of the self-timing circuit to automatically adjust the internal memory cycle to higher voltages gives then again sufficient margin to widen the word line activation window. This is illustrated in Figure 5. It depicts the clock and word line signals of a core-cell during a read operation. The *RPST* settings are identical as in Figure 4, but the memory is subjected to a 10% higher than nominal voltage which is typically applied at test stage. Comparing both figures shows that a higher supply voltage causes the memory control block to end the read operation around 100 ps earlier than under nominal conditions. Thus, even when the memory operates at its limits this behavior provides additional margin to configure the dummy bit line driver to $RPST_{max}$ during high-voltage tests.

Please note that the SRAM operation frequency only restricts extending the word line activation window but does not constrain reducing it. Moreover, above analysis equally applies to the WPRST pins for modifying the word line activation window during write operations. However, as read operations are typically slower and thus determine the internal memory cycle length, that case is less critical.

B. Fault injection

During test phase, voltage guard-bands are applied for both minimum V_{DD} as well as maximum V_{DD} tests, whereas the latter one is considered as more critical owing to the quadratic dependence of dynamic power consumption on supply voltage. Higher test voltages might therefore reduce the number of memory instances that can be tested in parallel due to constraints on the chip's power network. Simultaneously, it is well known that higher test voltages are required for reliable detection of resistive-opens defects which were reported as the main contributor to test escapes in deep submicron technologies [16] due to the growing number of interconnects and vias. We therefore evaluate the proposed methodology as a test solution to enhance the detection of (marginal) resistive-open defects without having to further increase voltage guard-bands.

Nevertheless, as the method controls the functional margins of SRAMs it can equivalently be applied to improve the detection of cells subjected to parametric failures (read, write, access) which become more prevalent with shrinking device size [17]. A fast sense amplifier activation makes parametric read faults more susceptible to occur while delaying the sense amplifier activation imposes higher stress on cell access faults. Similarly, during write operations a shorter word line pulse lowers write margins which makes parametric write faults easier to detect. The sensitization of these parametric faults can also be improved by lowering the supply voltage which, however, does not allow to impose particular stress on either read or access faults.

To quantify effectiveness of this technique, we employ the general defect injection and fault modeling framework. The underlying memory used for this study is an industrial

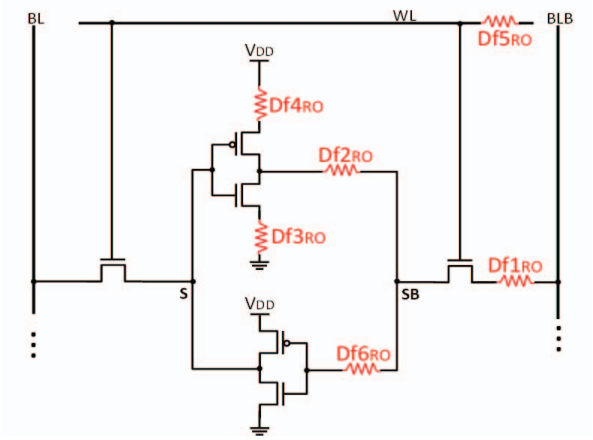

Fig. 6: Resistive open-defects inside a SRAM core-cell.

SRAM design fabricated at 28nm process technology. First, we inject the resistive-open defects *Df1-Df6* into a core-cell as depicted in Figure 6. Due to symmetry effects *Df1-Df6* allow an exhaustive analysis of all resistive-open defects inside SRAM cell structures [18]. Next, the faulty behavior induced by these defect is modeled at the functional level by the following fault models which were shown to capture the injected defects [18]:

- **Transition fault (TF)** [19]: A core-cell is said to have a TF if it fails to undergo a transition ($1 \rightarrow 0$ or $0 \rightarrow 1$) when a write operation is performed on it.
- **Incorrect read fault** [19]: A core-cell is said to have an IRF if a read operation performed on such core-cell returns the incorrect logic value while keeping the correct data stored previously.
- **Read destructive fault (RDF)** [19]: A core-cell is said to have a RDF if a read operation performed on the core-cell changes its contents and returns an incorrect logic value.
- **Deceptive RDF (DRDF)** [19]: A core-cell is said to have a DRDF if a read operation performed on it returns the correct logic value but changes the contents of the core-cell.
- **Dynamic RDF (dRDF)** [9]: A core-cell is said to have a dRDF if a write operation immediately followed by m read operations cause the core-cell to flip its content and the incorrect logic value is observed at the SRAM output.
- **Dynamic deceptive RDF (dDRDF)** [9]: A core-cell is said to have a dDRDF if a write operation immediately followed by m read operations causes the core-cell to flip its contents and the correct logic value is observed at the SRAM output.

In the subsequent section we analyze how the detection of these fault models is affected by different *RPST/WPST* pin settings and based on that we evaluate the whole methodology.

IV. Experimental results

To evaluate the influence of the self-timing circuit configuration on the coverage of resistive-open defects, we simulate defect resistance values ranging from 0 Ω to 1 GΩ at a temperature of 25° C. In order to reduce simulation time, an iterative simulation approach was applied which starts with

interval sizes of 100 MΩ and divides at each step the interval of interest into smaller ones. We then determine for different *RPST/WPST* settings the lowest detectable resistance values.

Table I summarizes the minimum detectable defect sizes for each fault model under nominal test conditions (V_{DD} = 1.1V), whereby the self-timing circuit configuration which maximizes defect coverage is highlighted in bold. The symbol '-' indicates that a setting has no or insignificant impact on the defect coverage of the corresponding fault model. We applied the *RPST* settings of Figure 4. The influence of the *WPST* setting on the word line window length is not depicted, however the $WPST_{min}$ setting was measured to shorten it by 70 ps with respect to $WPST_{nom}$. The $WPST_{max}$ configuration is not further considered as it was found not to improve test efficiency.

The simulation results show that a longer word line activation window during read operations improves the detection of faults caused by *Df2* or *Df3* by 15% and 12% , respectively, whereas in case of *Df4* it even amounts to 22%. Since both static and dynamic RDF/DRDF capture cell stability, a higher read disturbance as imposed by the $RPST_{max}$ setting eases their detection. On the contrary, a shorter word line window increases considerably the coverage of incorrect read faults as shown at the example of *Df5*. The $WPST_{min}$ pin setting reduces the write margin of the memory and thus enhances the detection of transition faults. An increase of 21% and 19% was observed for the defect coverage of *Df5* and *Df6*, respectively, whereas it has little impact on the detection of *Df1*.

Table II lists the minimum detectable resistance values of the same experiment but subjected to a 10% higher voltages stress as typically applied at test stage. The corresponding word line signals during read operations are depicted in Figure 5. During write operations the $WPRST_{min}$ setting was measured to shorten the word line window by 60 ps with respect to $WPRST_{nom}$. Comparing the simulations results of Table I and II proves once more the effectiveness of higher supply voltages for the detection of resistive-open defects but also reveals that the proposed test solution improves the defect coverage in both setups similarly. Moreover, analyzing the defect coverage of *Df2-Df4* shows that even when the memory operates at its frequency limit (indicated by $RPST_{high}$), the proposed methodology still significantly increases cell stability stress during test stage as the $RPST_{max}$ configuration can be applied. In general, the experimental results show that the proposed test solution increases the detectable size of resistive-open defects by up to 30% dependent on their location. Furthermore, they point out that the improvement in terms of cell stability faults is largely related to the available margin between the memories internal cycle and the applied clock frequency. The sensitization of incorrect read faults and transition faults is thereby not affected.

The above results show that the configuration of the self timing circuitry greatly impacts the defect coverage of functional test patterns. How this behavior can be leveraged to increase the efficiency of commonly applied March algorithms is analyzed next.

V. March test solution

As the *RPST* and *WPST* settings are dynamically modifiable via the memory pins, they can be set accordingly to maximize the detection of functional fault models (FFMs). From Table I and II, we infer that applying $WPST_{min}$ improves the detection of TF and that the $RPST_{max}$ setting enhances the defect coverage of both static as well as dynamic RDF and DRDF. Whereas on the contrary, IRF are better sensitized using the $RPST_{min}$ configuration. This further highlights the inherent trade-off between stressing cell stability and sensitizing incorrect read faults. Thus, the self-timing circuit cannot augment a single read operation to better stress stability faults without simultaneously losing coverage on incorrect read faults. State-of-the-art test algorithms are highly optimized and designed to maximize the coverage of single cell as well as coupling cell fault models while also reducing the number of memory operations. The *RPST/WPST* values must therefore be carefully chosen for non-trivial algorithms.

Nevertheless, industrial memory test sets include also a large number of test patterns which were not developed based on fault model coverage such as Hammer or Scan [20]. The proposed method can be easily integrated into those sequences to make them more effective. We exemplify this using the PMOVI algorithm [21] which is shown in Figure 7. In the first March element the algorithm writes the cell array to the all zero state. Each of the remaining March elements is composed of a write operation surrounded by two read accesses. This ensures that all write operations function correctly and no cell state is disturbed by a write or read operation on another cell.

PMOVI algorithm:	**Pin configuration:**	**Sensitized FFMs:**
⇓(w0)	$WPST_{nom}$	-
⇑(r0, w1, r1)	$RPST_{min}$, $WPST_{min}$	IRF, TF
⇑(r1, w0, r0)	$RPST_{max}$, $WPST_{nom}$	(d)RDF, (d)DRDF
⇓(r0, w1, r1)	$RPST_{max}$, $WPST_{nom}$	(d)RDF, (d)DRDF
⇓(r1, w0, r0)	$RPST_{min}$, $WPST_{min}$	IRF, TF

Fig. 7: The specification of the PMOVI algorithm, and its *RPST/WPST* settings to improve the sensitization of FFMs.

The effectiveness of the PMOVI algorithm can be significantly improved by adjusting the margins of its read and write operations using the proposed methodology. A potential configuration of *WPST/RPST* pins that equips every memory operation with additional parametric stress is shown in Figure 7. The setting in the first, initializing march element is irrelevant. IRF as well as TF of both data values 0 and 1 are better detected by the second and fifth march elements. The third and fourth march elements target cell stability faults. By executing the algorithm in fast-column addressing order, read equivalent stress [22] ensures the detection of read destructive and dynamic fault behavior. As a result, the above enhanced algorithm checks that every cell operates reliably under adverse operation conditions degrading read and write margins and that no cell state is disturbed by higher read disturbance or lower functional margins of another cell.

VI. Conclusions and summary

We presented and analyzed a novel test technique which allows to make memory read and write operations more

TABLE I: The maximum detectable resistance values at V_{DD}=1.1V.

Defect	Fault model	$WPST_{min}$	$WPST_{nom}$	$RPST_{min}$	$RPST_{nom}$	$RPST_{high}$
Df1	TF	**86K (+2%)**	88K	-	-	-
Df2	RDF/DRDF	-	-	822K (-17%)	702K	**597K (+15%)**
Df3	RDF/DRDF	-	-	270K (-11%)	243K	**214K (+12%)**
Df4	dRDF/dDRDF (m=5)	-	-	177M (-16%)	153M	**119M (+22%)**
Df5	TF	**3.1M (+21%)**	3.9M	-	-	-
	IRF	-	-	**5.7M (+19%)**	7.0M	9.6M (-37%)
Df6	TF	**3.9M (+19%)**	4.8M	-	-	-

TABLE II: The maximum detectable resistance values at V_{DD}=1.21V.

Defect	Fault model	$WPST_{min}$	$WPST_{nom}$	$RPST_{min}$	$RPST_{nom}$	$RPST_{high}$	$RPST_{max}$
Df1	TF	**73K (+3%)**	75K	-	-	-	-
Df2	RDF/DRDF	-	-	214K (-8%)	198K	179K (+10%)	**168K (+15%)**
Df3	RDF/DRDF	-	-	81K (-7%)	76K	73K (+4%)	**69K (+9%)**
Df4	dRDF/dDRDF (m=5)	-	-	119M (-16%)	103M	89M (+14%)	**72M (+30%)**
Df5	TF	**2.8M (+20%)**	3.5M	-	-	-	-
	IRF	-	-	**4.7M (+29%)**	6.6M	9.2M (-39%)	13.1M (-98%)
Df6	TF	**3.3M (+18%)**	4.0M	-	-	-	-

sensitive to (marginal) manufacturing defects by controlling the behavior of the internal SRAM self-timing circuitry. The proposed technique comes with no memory area overhead. The amount of additional parametric test stress can be digitally fine-tuned, however might be limited by the internal cycle length of the memory. It is therefore especially effective for memories which are not pushed to their design limits by the applied clock frequency. Furthermore, the technique can be easily integrated into non fault-model based test sequences. Including such an augmented test sequence in a memory test set ensures high memory noise margins exceeding those established by V_{DD} guard-banding. Whether such enhanced algorithms can reduce the overall test set size by sensitizing a large part of marginal defects still needs to be worked out based on silicon experiments.

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