Pre-Bond Testing of the Silicon Interposer in 2.5D ICs*

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***Abstract*—In interposer-based 2.5D integrated circuits, the passive silicon interposer is the least expensive component in the chip. Thus, it is desirable to test the interposer before bonding to ensure that more expensive and defect-free dies are not stacked on a faulty interposer. We present an efficient method to locate defects in a passive interposer before stacking. The proposed test architecture uses e-fuses that can be programmed to connect or disconnect functional paths inside the interposer. The concept of die footprint is utilized for interconnect testing, and the overall assembly and test flow is described. In order to reduce test time, the concept of weighted critical area is defined and utilized. We present HSPICE simulation results to demonstrate the effectiveness of the pre-bond test solution. The benefit of using weighted critical area is demonstrated using a commercial interposer from GLOBALFOUNDRIES.**

I. Introduction

Continued scaling of integrated circuits has resulted in increased interconnect delay being a major performance bottleneck. A potential solution to this problem lies in the combination of chip-scale wires and through-silicon-vias (TSVs). This solution is being incorporated in 2.5D ICs [1], which are recognized as a precursor to 3D integration, but with lower fabrication cost and less design complexity.

The fabrication of 2.5D ICs involves the introduction of a passive silicon interposer that is placed between the package substrate and the dies. A cross-sectional view of an interposer example with functional paths is shown in Fig. 1. The interposer contains both horizontal and vertical interconnects [2]. These interconnects are fabricated using the same processes as the interconnects in the silicon dies. As a result, with the high-density interconnects, 2.5D ICs can provide enhanced system performance, reduced power consumption, and support for heterogeneous integration [3].

In a 2.5D IC, testing of the interposer before die stacking is essential to minimize the yield loss that results from the stacking of good dies on a defective interposer. This need is especially critical since the interposer is the least expensive component in the entire stack. In the worst case, a cheap, but faulty, interposer will render the expensive 2.5D IC unusable. Therefore, pre-bond testing of the silicon interposer is needed to avoid the stacking of known good dies on a faulty interposer.

The interposer cannot be tested easily before it is stacked with other dies due to several reasons [4]. Pre-bond testing of interposer targets both horizontal and vertical interconnects, which requires double-sided probing. However, double-sided probing is not feasible today and innovations are needed in the assembly process and test flow. In addition, it is difficult to probe the micro-bumps on the top side of the interposer due to their high density. Moreover, interconnects are separated from each other at the pre-bond stage, and no test loops can be formed at this stage. Therefore, new and innovative solutions are needed for pre-bond testing.

In this paper, we present an efficient solution to locate defects in the passive interposer at the pre-bond stage. The proposed test architecture uses e-fuses that can be programmed to connect or disconnect separated interconnects inside the interposer. Therefore, the functionality of the interposer is not affected once the dies are stacked on it. We also describe an assembly and test flow that facilitates pre-bond interposer test. This assembly and test flow has been validated in a production environment. In order to reduce test time, the concept of a weighted critical area is introduced. The proposed solution therefore obviates the need for a more expensive active interposer. We present HSPICE simulation results to demonstrate the effectiveness of the pre-bond test solution. The advantage of using the weighted critical area is also analyzed.

The reminder of this paper is organized as follows. Section II presents previous pre-bond test solutions and describes the structure of e-fuses. Section III first defines a "die footprint" and presents the proposed test architecture. Next, the assembly/test flow and test procedures are discussed. Finally, the concept of weighted critical area is introduced. In Section IV, we present HSPICE simulation results and analyze the benefits of using the weighted critical area for an interposer from GLOBALFOUNDRIES. Section V concludes the paper.

II. Related prior work

In this section, we describe recently published work on pre-bond interposer testing and provide an overview of e-fuses.

A. Pre-Bond Testing of Interposers: State-of-the-Art

Prior methods for post-bond interposer testing are described in [2], [5]. For pre-bond testing, Christo et al. proposed a method that employs a test probe and an electrically conductive glass handler [6]. The conductive glass handler is used to connect two separated interconnects, which then permits same-sided probe testing. However, the structure of their interposer is different from that used in industry. Li et al. proposed the use of a test interposer that is in contact with the interposer under test [7]. Combining these two interposers provides access to nets that are not normally accessible. However, this method is costly because it requires a customized design of the tested interposer for each interposer design.

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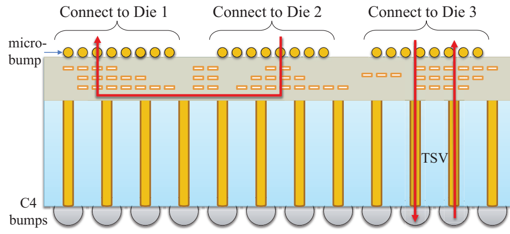


Fig. 1. Illustration of an interposer example with functional paths.

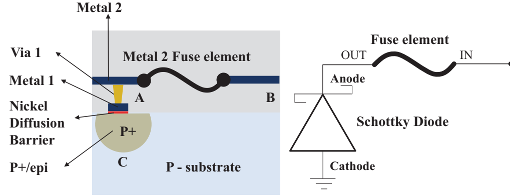


Fig. 2. Illustration of the structure of an e-fuse based on a Schottky contact.

A case study on pre-bond testing was presented in [4]. Additional dummy metal is used to form test loops. However, the specific micro-bump/TSV structure, wherein a set of TSVs and micro-bumps are connected together for testing, does not correspond to actual interconnect structures in a 2.5D IC. Another approach for pre-bond testing was recently proposed in [8]; it aims to improve production yield by proposing a contactless testing mechanism. This method attempts to detect a defective interposer using a thermal image taken after the interposer has been heated. However, neither the types nor the locations of the defects can be identified in this approach.

B. Structure of an E-fuse

E-fuses have been used in a variety of applications due to their programmability [9]. The schematic of an e-fuse is shown in Fig. 2. OUT is connected to the anode of the Schottky contact [10]. When testing the interconnects/TSVs, the e-fuse is not programmed and signals flow through it. After testing, a high current pulse is applied at IN to the e-fuse such that it is programmed open at OUT and the current is discharged through the cathode of the Schottky contact into the silicon substrate [11]. With the use of Schottky contact, the interposer is still passive after the inclusion of e-fuses. It is especially important to enable the pre-bond testing of passive interposers since active interposers increase production cost. Our proposed method is therefore targeted at passive interposers.

There are three kinds of e-fuse devices: (i) formed with a silicide gate poly-Si electrode material (gate-electrode-fuse); (ii) constructed from Cu wire (Cu-fuse); (iii) consisting of a Cu-via (via-fuse) [12]–[14]. GLOBALFOUNDRIES reports that the resistance of the Cu-fuse is as small as 25 Ω before programming and several GΩs after programming. The low on-off resistance ratio of the Cu-fuse makes it an excellent candidate for the proposed test method. As a result, we consider a Cu-fuse in this work.

III. Proposed Test Architecture and Procedures

In this section, we define the concept of die footprint and introduce the proposed test architecture. The test flow is described and test procedures are listed. Finally, the weighted critical area is introduced to save test time.

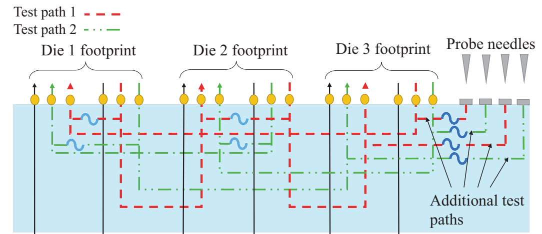


Fig. 3. Illustration of test paths for targeting horizontal interconnects.

A. Definition of Die Footprint

Although the dies have not been mounted on the interposer at the pre-bond stage, the design and fabrication of the interposer interconnects is typically based on the information (i.e., layout) of dies that will later be placed on the interposer [15]. Therefore, each die has a corresponding footprint on the interposer for subsequent bonding. The die footprint refers to the micro-pillar area to which the top-die connects to on an interposer. It contains all interconnects to and from the specific die. The directionality of interconnects is not taken into consideration because they are typically just back-end of line (BEOL)/metal lines and can be treated as direction-independent before the top-die is assembled. As a result, although dies are not considered in the pre-bond stage, the corresponding die footprint should be taken into consideration.

Before the dies are stacked on the interposer, each interconnect in the interposer connects two separate die footprints. In the proposed method, separated interconnects are connected via e-fuses. Based on Fig. 1, it is clear that interposer testing requires the following: (1) testing of horizontal interconnects; (2) testing of vertical interconnects. Since it is difficult to probe both sides of the interposer simultaneously, these two types of interconnects are tested separately in the proposed method.

The length of each e-fuse is restricted in order to save space. In particular, for horizontal die-to-die interconnects, consider a test through four die footprints as $2 \rightarrow 1 \rightarrow 4 \rightarrow 3$. Since the interconnect $2 \rightarrow 1$ ends at Die 1 footprint and interconnect $1 \rightarrow 4$ starts at Die 1 footprint, connecting them using an e-fuse within the Die 1 footprint involves less interconnect length than doing it outside the die footprint. Therefore, each e-fuse can only be located within a single die footprint for testing horizontal interconnects; thus, for two horizontal interconnects to be connected by an e-fuse, they must share at least one die footprint. For vertical interconnects, the TSVs are spread out through the interposer. Connecting them through e-fuses outside the die footprint is a cheaper option.

B. Test Architecture

The general test architecture to target horizontal interconnects is shown in Fig. 3. An interposer example is utilized to illustrate the proposed test architecture. E-fuses are inserted inside the interposer, and horizontal interconnects, which are not connected in functional mode, are now connected for testing. In Fig. 3, two test paths are formed that start from the I/O ports in Die 3 footprint, pass through all three die footprints, and end in Die 3 footprint. It can be seen that the e-fuses are only located within a single die footprint; there are no e-fuses that span two die footprints. Test Path 1 starts from

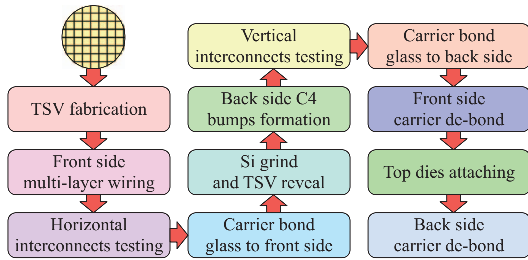


Fig. 4. Assembly and test flow for pre-bond testing.

Die 3 footprint, passes through Die 1 footprint and then Die 2 footprint, and ends in Die 3 footprint. Similarly, Test Path 2 starts from Die 3 footprint, passes through Die 2 footprint and then Die 1 footprint, and ends in Die 3 footprint. Once the test paths are formed, test patterns are applied to the test paths and the horizontal interconnects can be tested. After all horizontal interconnects are tested, the e-fuses will be programmed and their resistance will increase to a significantly large value. As a result, the e-fuses can be viewed as opens in the interposer. When the dies are later mounted on the interposer, these programmed e-fuses will not affect chip functionality.

Because the micro-bumps on the top of the interposer have very high density, it is difficult to use them to probe the interposer. Therefore, additional test paths are inserted into the interposer for probing purposes. As shown in Fig. 3, each additional test path is composed of a probe pad and an e-fuse. These probe pads and e-fuses are referred to as additional pads and additional e-fuses, respectively. In order to probe the interposer using standard probe needles, additional pads are fabricated with a larger pitch. Because they have different control signals, the additional e-fuses are different from the e-fuses that connect the functional interconnects. Thus, these two types of e-fuses are represented in different ways in Fig. 3. The additional e-fuses are also programmed after horizontal interconnect testing is complete so that the functionality of the 2.5D IC is not affected once the dies are stacked.

The test architecture for vertical interconnects is similar. E-fuses are inserted inside the interposer, and separated vertical interconnects are then connected. Once the test paths are formed between vertical interconnects, test patterns can be applied to these test paths from the bottom of the interposer. Since C4 bumps at the bottom of the interposer can be probed directly with standard probe needles, no additional test paths are required to test vertical interconnects. Once all vertical interconnects have been tested, e-fuses will be programmed and treated as opens, once again disconnecting separate functional interconnects inside the interposer.

C. Assembly and Test Flow

In contrast to 2D ICs, which require only one wafer-level test insertion, we need both final thick-wafer test and thinned-wafer test steps in order to determine a known good interposer (KGI) for 2.5D ICs. The assembly process flow is shown in Fig. 4. Thick-wafer test is used to test horizontal interconnects. The BEOL layers such as Cu and Al are first plated on the thick wafer; then the horizontal interconnects are tested prior to wafer fab-out. If standard probe cards are used, then additional probe pads are required. However, a fine-pitch probe card with compliant probes can be used to test directly on the micro-bump pads having a NiAu finish. Research is currently underway and progress has been reported on such fine-pitch probe cards [16]. This eliminates the need for additional probe pads and access to program the e-fuses that is used to form longer test paths. Afterwards, wafers are bonded to temporary glass carriers from the front.

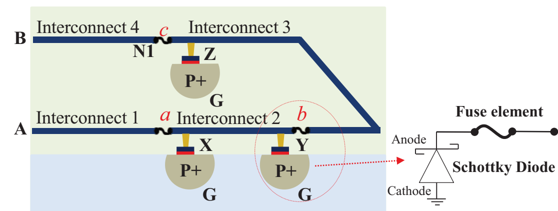


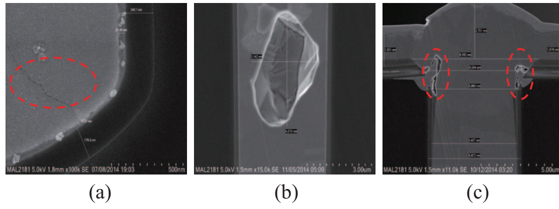
Fig. 5. Illustration of a test path.

The testing of thinned wafers is a significant challenge but it can be addressed using techniques that are currently deployed in industry [4], [6], [7]. Compared to methods mentioned in Section II, e-fuses are less costly and thereby can be used more easily to form test paths. Thin-wafer test is implemented after TSV-reveal to test vertical interconnects. The C4 bumps are completed prior to thin-wafer test to prevent probing on backside Cu pads. Then vertical interconnects are tested via e-fuses; afterwards, thinned wafers are bonded to another temporary glass carrier from the back. This approach has been verified and implemented in a production environment [17]. Finally, two glass carriers are de-bonded separately; top dies are attached to the front side of the interposer and the stack is assembled on to a package substrate. In order to support this two-sided test for interposers, the preferred assembly process would be with a wafer support system so that the interposers are on a carrier wafer and can be probed on either side.

D. Test Procedures

Three types of faults can typically occur in the horizontal interconnects: open faults, inter-bridge faults, and inner-bridge faults. *Open faults* refer to any hard or resistive opens, regardless of the fault location. *Inter-bridge faults* refer to bridge faults that occur between two test paths; e.g., an interconnect in one test path is shorted with another interconnect in a different test path. *Inner-bridge faults* refer to bridge faults that occur inside a single test path; e.g., an interconnect in a test path is shorted with another interconnect from the same test path. In order to identify the type and location of these faults, specific test procedures are required.

Since each test path can be viewed as a single interconnect, a traditional interconnect test algorithm (True/Complement Algorithm) [18] is used here. Similarly, the detection of open faults and inter-bridge faults does not depend on whether a test path or a functional interconnect is viewed as a single interconnect. Therefore, open faults and inter-bridge faults can also be detected by the True/Complement Algorithm. With this algorithm, test patterns are applied to one end of a test path and test responses are observed at the other end. However, this method is not applicable for the detection of inner-bridge faults. For example, suppose a logic 1 is applied to a test path at one end. No matter whether the test-path is fault free or



(a) (b) (c)

Fig. 6. TSV defects: (a) break, (b) void, (c) pin-hole

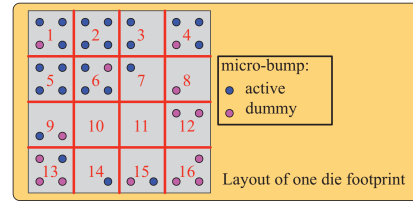


Fig. 7. Illustration of the subarea division for a die footprint.

contains inner-bridge faults, a logic 1 will be observed at the other end. Therefore, the faulty response is identical to the correct response. As a result, a new test procedure has been developed for inner-bridge faults.

A test path is shown in Fig. 5. This test path is composed of four functional interconnects, and these interconnects are connected by e-fuses a, b, and c. To detect the inner-bridge faults, the e-fuse that is closest to point A is different from the other e-fuses; specifically, its diode is at the end rather than at the head. The proposed test procedures are listed:

1) Apply logic 1 at point A and observe the response at point B. If there are no faults in the test path, a logic 1 will be observed at point B.

2) Program the e-fuse a so that the test path is open at a's position. Apply logic 1 at point A and interconnect 2 is discharged through point X. If a logic 1 is observed at point B, it indicates that an inner-bridge fault exists between interconnect 1 and the remaining interconnects. Otherwise, point B is grounded via point X and interconnect 1 does not have an inner-bridge fault.

3) Apply logic 1 to point B and program the e-fuse b so that the test path is open at b's position. Interconnect 2 is discharged through point Y. Then point B is taken as an observation point and the voltage level is measured at point B. If logic 0 is observed at point B, it indicates that an inner-bridge fault exists between interconnect 2 and the remaining interconnects. Otherwise, the charge in the remaining interconnects should remain high and a weak logic 1 should be observed at point B with a slow discharging rate.

4) Apply logic 1 to point B and program e-fuse c so that the test path is open at c's position. Interconnect 3 is discharged through point Z. Then the voltage level is measured at point B. The same method used in step 3 is utilized to detect whether there is an inner-bridge fault between interconnect 3 and interconnect 4.

Based on data from GLOBALFOUNDIRES, the pitch of the vertical interconnects is large (100 μm). Therefore, bridge faults are unlikely to occur in vertical interconnects and thus the True/Complement Algorithm is not necessary for vertical interconnect testing. During the TSV processing, there are three types of faults that can occur in vertical interconnects: break faults, void faults, and pin-hole faults. Fig. 6 shows images of the three faults. The physical mechanisms underlying these three faults are discussed in [19]. Break faults and void faults increase the TSV resistance by different amounts based on the defect dimensions. Pin-holes create a conduction path from the TSV to the substrate, resulting in a leakage fault. In order to detect these faults, a high voltage is applied to the vertical test paths. The three types of faults can be detected and identified based on the differences in response voltage.

E. Weighted Critical Area

Because the interconnects are not uniformly distributed on the interposer, some areas of the interposer may have a higher density of interconnects. An area with more interconnects, which can be flagged based on technology, process, and yield considerations, is referred to as weighted critical area. If a test path contains functional interconnects that connect to the same weighted critical area, it is referred to as a dense test path; otherwise, it is called a non-dense test path. In non-dense test paths, no two interconnects are in the same area and hence inner-bridge faults are less likely to occur; thus, it is not necessary to program e-fuses in that test path serially and programming time is reduced.

In a typical interposer, the location of micro-bumps can be easily tracked from the design netlist. Some micro-bumps (dummy micro-bumps) are not connected to any interconnect. Therefore, a weighted critical area is only determined by the information of active micro-bumps. We have developed a systematic method to determine a weighted critical area. Let the length and the width of an interposer be L_{int} and W_{int}. The interposer is divided into $n \times n$ subareas, where n is defined as the division resolution of the interposer. The number of active micro-bumps is accounted for each subareas (num_i); the average value (avg) and standard deviation (σ) are calculated. If num_i is greater or equal to $avg + \sigma$, then the subarea i is defined as a weighted critical area. As shown in Fig. 7, the interposer is divided into 16 subareas; avg and σ are calculated as 1.5 and 1.414. Therefore, subareas 1, 2, 4, 5, 6 are determined to constitute the weighted critical area.

In order to analyze the influence of weighted critical area, we use the acronym "WCA" to refer to the testing approach that considers the weighted critical area; "nWCA" refers to the testing approach that does not consider weighted critical area. In nWCA, since bridge faults may exist between any two interconnects, all test-paths must be tested for inner-bridge faults. In contrast, only dense test paths are tested for inner-bridge faults in WCA. Therefore, the use of WCA can help us to reduce the testing time.

IV. Experimental Results

In this section, we present simulation results and an evaluation of the benefits provided by the weighted critical area. The simulations are carried out using HSPICE. The parameters (Table I) reflect the state-of-the-art interposer technology.

A. Testing the Horizontal Interconnects

The circuit model of Fig. 8(a) is simulated in order to analyze the effectiveness of the e-fuses. Two 1700 μm-length horizontal interconnects are connected by an e-fuse and a sequence of signals is applied to N1, shown as V(N1) in Fig.

TABLE I
TECHNOLOGY PARAMETERS USED FOR SIMULATION.

	Diameter	Height	Pitch	t_{ox}
TSV	10 μm	100 μm	100 μm	230 nm
	Width	Thickness	Resistance	Capacitance
M1	45 nm	105 nm	9.435 Ω/μm	0.2173 fF$/\mu$m
M2	45 nm	100 nm	9.467 Ω/μm	0.2035 fF$/\mu$m

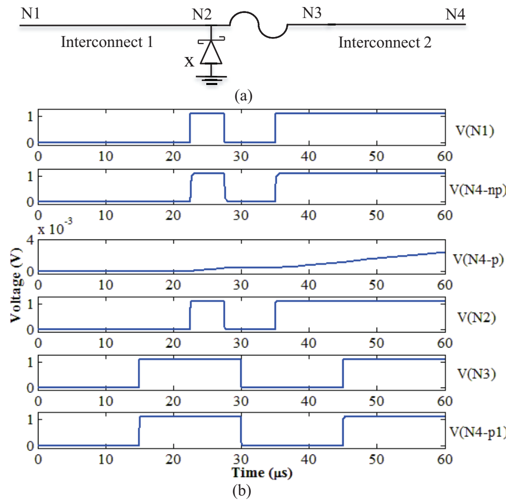


Fig. 8. Horizontal interconnects with an e-fuse: (a) circuit model, (b) simulation results.

8(b). Before the e-fuse is programmed, its resistance is as small as 25 Ω. Therefore, the e-fuse can be viewed as a short circuit and Interconnect 1 and Interconnect 2 are connected together. As a result, the signals applied to N1 are transmitted through the interconnects and are observed at N4, shown as V(N4-np) in Fig. 8(b). After the e-fuse is programmed, its resistance is as large as 4 GΩ. Therefore, the e-fuse can be viewed as an open circuit and Interconnect 1 is separated from Interconnect 2. As a result, no signals are transmitted to N4 and N4 is dangling, shown as V(N4-p) in Fig. 8(b).

Another set of simulations is carried out to verify that the programmed e-fuse does not affect the functionality of the interposer. Specifically, signals from N1 are applied to Interconnect 1 and signals from N3 are applied to Interconnect 2. With the programmed e-fuse, the responses from N1 are observed at N2, shown as V(N2) in Fig. 8(b), and the responses of N3 are observed at N4, shown as V(N4-p1) in Fig. 8(b). It can be seen that the two interconnects can operate independently. Therefore, the programmed e-fuse does not affect the normal functionality of the interposer.

We next simulate the test procedure for inner-bridge faults. The schematic in Fig. 5 is simulated. In the simulated condition, e-fuse a has already been programmed. Point X is grounded and point Z is isolated from the ground. Fig. 9 shows the responses at the observation point N1, which is one end of Interconnect 3. Meanwhile, a logic 1 is applied to B until 45 μs. If there is no inner-bridge fault between Interconnect 2 and the remaining interconnects, the responses at N1 are shown as V(N1-T) in Fig. 9. In region 1, the N1 voltage is slightly lower than 1.1 V because the circuit is shorted to ground through point X. Then, the e-fuse b is programmed in region 2. In this region, since a discharge path is temporarily formed through point Y, N1 voltage decreases slightly. After e-

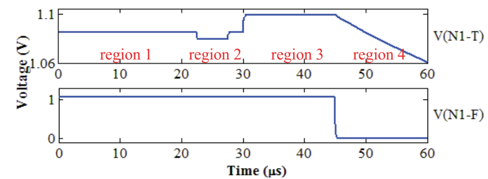


Fig. 9. Simulation results for inner-bridge fault testing.

fuse b is completely programmed, the circuit is open at position b. Since there is no path between "Interconnect 3−e-fuse c−Interconnect 4" circuitry and ground, N1 voltage increases to 1.1 V in region 3. At 45 μs, no signal is applied to B and B is dangling. Then, N1 voltage decreases slowly in region 4 due to discharge through capacitors.

If there is an inner-bridge fault between Interconnect 2 and the remaining interconnects, the responses at N1 are shown as V(N1-F) in Fig. 9. In this situation, regardless of whether e-fuse b is programmed, there is always a path between N1 and ground. Therefore, once B is dangling, N1 voltage drops to zero quickly. Based on the difference between V(N1-T) and V(N1-F), it can be seen that the proposed test procedure for inner-bridge faults is effective.

B. Testing for Vertical Interconnects

The circuit model in Fig. 10(a), which has two vertical interconnects connects by an e-fuse, is simulated. Each vertical interconnect is composed of a TSV, M1, and V1 vias. The length of M1 is 4.5 μm; the via V1 is typically 45 nm in diameter and 80 nm in height. Each M1 is connected to 6 V1s in parallel. In addition, each vertical interconnect is connected to an input or output driver through a horizontal interconnect. Since the effectiveness of e-fuse is verified in Section IV. A, it is not discussed for vertical interconnects.

The three TSV fault models are analyzed. The break fault models a full-open defect, as shown in Fig. 10(b), and the TSV resistance is modeled as extra resistance, which can be as large as 1 GΩ. The void fault is modeled in a manner similar to the break fault. Instead of imposing the significant resistance change as used in the break model, the resistance increase in the void model is caused by a reduction of the effective conducting area. As a result, it is significantly smaller than the output resistance of a typical driving gate. Therefore, the void faults can be neglected in interposer pre-bond testing.

The pin-hole fault is modeled as leakage, as shown in Fig. 10(c). A leakage resistance $\mathrm{R_{leak}}$ is placed in parallel with the TSV capacitance. Meanwhile, the TSV capacitance is also affected by the leakage, resulting in a decreased capacitance. The simulation results for the fault-free and faulty cases are shown in Fig. 11. A low to high transition is applied to N2, and the responses are observed at N5. At 40 ns, the fault-free response is 0.881 V. The responses of the pin-hole and break faults are 0.615 V and 0.007 V, respectively. Therefore, these two faults can be easily detected.

C. Evaluation of Weighted Critical Area

We have analyzed a commercial interposer from GLOBALFOUNDRIES; this interposer is referred to as X5. Five dies are stacked on the interposer: one ASIC die and four high-band-memory (HBM) dies. Interconnects are between the ASIC die

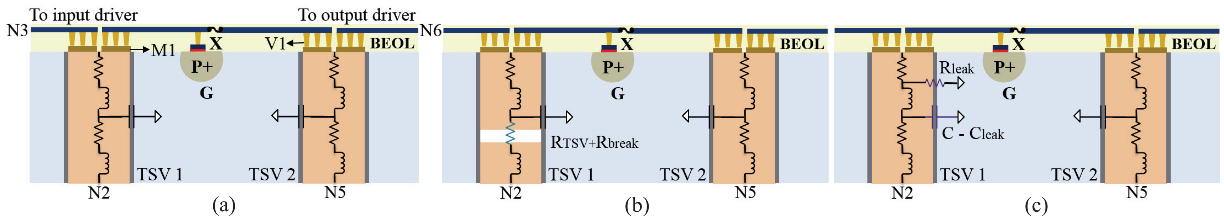


Fig. 10. Circuit models: (a) fault-free, (b) break faults, and (c) pin-hole faults.

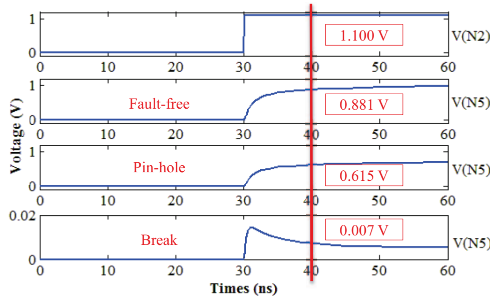


Fig. 11. Simulation results for the testing of TSV defects.

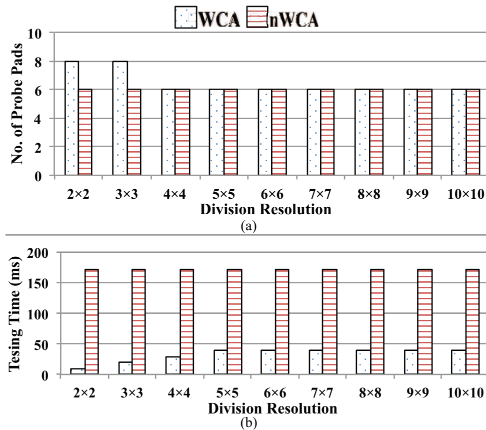


Fig. 12. Experimental results with different division resolutions.

and each HBM die. Based on data from the manufacturer, the time from applying a test pattern to observing the test response is 25 μs; the time to program e-fuse (t_e) is 7.5 μs.

The influence of weighted critical area is analyzed, where division resolution (n) is varied from 2 to 10. Therefore, the interposer is divided from 2×2 to 10×10 subareas. Then the pre-bond testing is implemented on them. The experimental results are shown in Fig. 12. The number of probe pads for WCA is larger than those for nWCA when n is small because WCA introduces more constraints when test paths are formed. With an increase in n, the constraint is weaker because functional interconnects that are originally in the same area at low resolution are in different areas now; the number of probe pad finally reach the same value for WCA and nWCA. In Fig. 12(b), WCA can significantly reduce the testing time, which is at most 20% of that in nWCA. Therefore, it is advisable to include weighted critical area for pre-bond testing.

V. Conclusion

A new test architecture for pre-bond interposer testing has been introduced. When the interposer is under test, e-fuses are used to connect separated interconnects to test both horizontal and vertical interconnects. After testing and interposer qualification, e-fuses are programmed to disconnect interconnects. The concept of die footprint is utilized for interconnect testing, and the overall assembly and test flow has been described. In order to reduce test time, the concept of weighted critical area has been defined and utilized. We have presented HSPICE simulation results to demonstrate the effectiveness of the pre-bond test solution. The benefit of using the weighted critical area has been demonstrated using a commercial interposer as a realistic test case.

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