Design of Latches and Flip-Flops using Emerging Tunneling Devices

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***Abstract*—Tunneling field-effect transistors (TFETs) stand out among novel device technologies for low-power circuits and systems. While some TFETs exhibits behavior similar to MOSFETs, a group of emerging tunneling devices including symmetric tunneling FETs (SymFETs) and interlayer tunnel FETs (IFETs) demonstrate a bell-shaped I-V characteristic dissimilar to that of MOSFETs. They have shown the potential for image processing and nontraditional computing in analog applications and the design of Boolean gates with SymFETs has also been explored. This paper uses a SymFET as a proxy to design sequential circuits comprised of devices with bell-shaped I-V characteristics. Said circuits are essential as practically any application requires the indefinite storage of data and control modules during computation. We show that the negative differential resistance (NDR) behavior of SymFET transistors can be employed to build compact and low power latches and flip-flops. The relationship of SymFET with another well-known tunneling device, namely resonant tunneling diode (RTD), is investigated. We illustrate how previous research on RTD-based circuits – such as monostable-bistable (MOBILE) self-latching circuits and highly compact MOBILE-based D flip-flop circuits – can be adopted to SymFETs. Our paper provides a novel path of circuit designs based on devices that have characteristics similar to SymFETs and shows that SymFETs are a promising option for image processing applications in terms of power and area.**

I. Introduction

Over the past few decades, many new devices have been proposed for low-power nano-scale signal processing [1]. Properties of these post-CMOS devices are completely dissimilar to today's MOSFETs. A class of emerging transistor technologies that operate via tunneling have bell-shaped I-V characteristics. More specifically, recent publications on double-layer graphene transistors [2], symmetric tunneling field-effect transistors (SymFET) [3], bi-layer pseudo-spin FETs (BiSFET) [4], and interlayer tunnel FETs (ITFET) [5] all report bell-shaped I-V curves. This behavior is also exhibited in molecular transistors [6] and single-electron transistors [7] as well. Ultimately, the ability to design compact, high-performance, and/or energy efficient circuits and systems with the aforementioned transistor technologies – that are superior to CMOS and/or the current state-of-the-art – will determine the utility of said devices. In this work, we consider how sequential circuit elements can be realized with devices that exhibit bell-shaped I-V characteristics.

To the best of our knowledge, work related to the design of digital circuits comprised of emerging transistor technologies with non-traditional I-V characteristics is rather limited, let alone storage elements/sequential circuits. The authors of [8] considered how logic gates may be designed with BiSFET devices. (This work assumes a 25 mV supply, which could be problematic since the ripple on the supply rails is often on the order of 10s of mV.) An SRAM cell without access transistors was presented in [9], which used negative differential resistance (NDR) to build a bistable circuit with only two transistors (as opposed to four in a typical CMOS SRAM). Recently, SymFET devices have been explored for both analog and digital circuits/applications. SymFETs are studied as for improving hardware security [10], and for realizing conventional digital logic with enhanced functionality (e.g., inverters with Schmitt-trigger behavior, 3-device majority voters, etc.) [11]). In the context of non-Von Neumann computer architectures, [12] considered using SymFETs to realize circuitry required for cellular neural networks (CNNs). Notably, the authors present SymFET-based anisotropic diffusion hardware, useful for edge preserving, image denoising, etc., common steps in image processing pipelines. SymFET-based hardware is passive and requires just 1-device/node (compared to 30+ devices in CMOS hardware) in an RC network. However, per [13], [14], other digital hardware and storage elements are required to actually use diffusion hardware. While it might be possible to develop hybrid CMOS-SymFET systems by leveraging CMOS for the digital part, such an approach presents significant integration challenges. Fulfilling the needs for SymFET storage elements will pave the way for designing SymFET digital and mixed-signal circuits for image processing as well as other applications.

The focus of this paper is on designing flip-flops (FF) and latches with devices exhibiting bell-shaped I-V characteristics, specifically with SymFET as the representative device. DFFs and latches are basic sequential logic elements required for effectively every circuit/application described above. We propose several new latch circuits that have topologies different from those of CMOS designs. We study the relationship between SymFETs and resonant tunneling diodes (RTDs) to verify the feasibility of adopting RTD-based circuits. Specifically, monostable–bistable transition logic element (MOBILE) circuits, proposed for RTDs in [15], are redesigned using SymFETs. Inspired by MOBILE and latch circuits proposed above, we further introduce SymFET-based D flip-flops (DFFs) with lower device counts. We then evaluate the performance of SymFET-based gates to investigate their potential benefits.

II. Background

Below, we first describe the relevant SymFET characteristics and the device model. We then briefly review the use of SymFET to motivate the needs for SymFET-based sequential circuit elements. We finally give a short review of a RTD MOBILE circuit which inspired our SymFET DFF designs.

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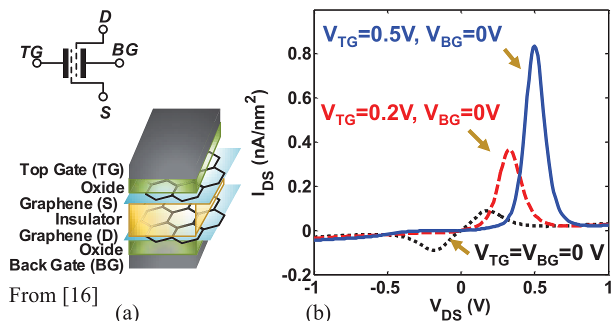

Fig. 1. (a) Physical structure and symbol of a SymFET. (b) Its characteristics.

A. SymFET device description and usage

The physical structure of a SymFET and its I-V characteristics are illustrated in Fig. 1. Tunneling occurs between two graphene sheets separated by a thin insulator. The top-gate (TG) and back-gate (BG) voltages change the carrier type and sheet density of the drain (D) and source (S) graphene layers by electrostatic field. In this device, the tunneling probability depends on the availability of occupied/empty states on both sides of the tunneling barrier. The gate voltages can modulate the drain-source current I_{DS}. The I_{DS}-V_{DS} curve has a peak current. Per Fig. 1(b), both the value and position of the peak depend on the gate voltages. Note that the device is symmetric. If $V_{TG} - V_{BG}$ were set to a negative value, then the peak current would have appeared at a negative V_{DS}. (In other words, the role of TG and D are interchangable with that of BG and S). SymFET I-V characteristics have also been observed experimentally [2], and recent experiments suggest strong differential conductance even at room temperature [16]. While beyond the scope of this paper, more detailed analyses of the device can be found in [3], [17]–[19][1].

For the work to be discussed here, as in [11] we employ the analytical model in [3], [19] to find I_{DS} via the terminal voltages, for a device with an effective oxide thickness of 1.2 nm, and 1.34 nm of boron nitride (4 layers of h-BN) insulator between undoped graphene sheets. The active device area is assumed to be a square and the coherence length is 0.75 times the square side. (Coherence length determines what percentage of the graphene sheets is structurally perfect; see [18] for more details.) As current research works are mostly limited to large graphene sheets, the minimum size transistor is conservatively selected to be 100 nm-by-100 nm in all simulations. Data is used to build a (tabular) Verilog-A model. This allows us to do SPICE simulations with this 4 terminal device. Model capacitors are based on planar capacitance between TG and S, BG and D, and also between D and S. No quantum capacitance or fringe capacitance is considered. We believe that these initial assumptions are reasonable even as the actual device structure may evolve.

The unique I-V characteristics of SymFETs open the door for novel use of these devices to drastically simplify circuits in a number of applications. For example, [12] suggested that SymFET-based CNNs could solve problems with fewer computational steps (or template operations) as compared to conventional, MOSFET-based CNNs. SymFETs have also been considered in CNN-inspired architectures – specifically diffusion networks and other Gaussian-function processing that are currently used to do image denoising, etc. as a pre-processing step [20]. The authors of [20] suggest that a SymFET-based approach could reduce device count of a diffusion network by a factor of 30. Moreover, in a CMOS-based version, resistive-fuses would be active circuits, whereas the SymFET-based nonlinear element is fully passive, resulting in no extra power dissipation in the cell. However, SymFET-based diffusion network requires external logic control and storage/sequential elements to achieve the complete application as like [13], [14]. Integrating CMOS digital logic with SymFET diffusion network presents not only significant fabrication challenge but also could significantly lower the benefit of SymFET diffusion network. Pure-SymFET implementations without performance and power degradation would be much more desirable for such applications.

[1] Also, note that devices such as the interlayer tunnel FET (ITFET) [5] have a similar behavior to a SymFET. Furthermore, recent graphene-based tunnel FETs also have similarities with structures first proposed in the 1990s [21]. We use SymFETs as a proxy for all these types of devices.

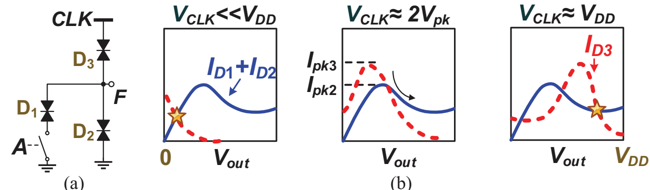

Fig. 2. (a) RTD-based MOBILE inverter. (b) Its operation (for a low A) as CLK gradually increases.

B. RTD MOBILE inverter

Some features of SymFETs resemble those of RTDs, which can shed light on how to design SymFET-based logic elements. There has been a significant amount of research on developing logic circuits using RTDs [22]. While we do not intend to revisit this entire body of work here, we do review one key RTD design concept, MOBILE, perhaps the most popular RTD-based logic element [15].

MOBILE structures have a *self-latching* property. More specifically, the RTD-based circuit in Fig. 2(a) works both as an inverter and edge-triggered flip-flop (DFF). The circuits has one switch (implemented by a transistor) and three RTDs which should be properly sized such that their peak currents satisfy the criteria in Eq.(1).

$$I_{pk2} < I_{pk3} \quad \text{and} \quad I_{pk1} + I_{pk2} > I_{pk3}. \tag{1}$$

The operation of the gate relies heavily on the NDR region of RTDs (see Fig. 2(b)). When the CLK signal is at a low voltage, the circuit is monostable and the output F is low. As the CLK signal increases, the driving current curve ($I_{D1} + I_{D2}$) intersects with the load current curve (I_{D3}) in the NDR region of the driving current, resulting in metastability. When the CLK signal becomes sufficiently large, the output reaches one of the two stable points. The example shown in Fig. 2(b) assumes that A is low ($I_{D1} = 0$), and the final output voltage is high. Similar operation applies for a high level A.

It can be readily seen that the RTD MOBILE inverter exhibits edge-triggered, self-latching properties. Unfortunately, the output of the mobile inverter returns to zero when CLK becomes low. However, by combining such a mobile inverter

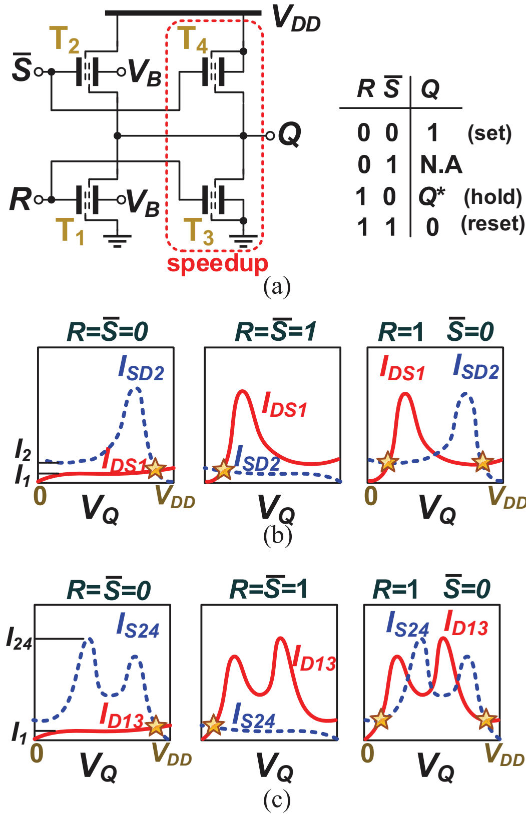

Fig. 3. (a) A latch and its truth table. (b) The I-V curve of transistors T1 and T2 when there is no speedup transistor. (c) The I-V curve of transistors where $I_{D13} = I_{DS1} + I_{DS3}$ and $I_{S24} = I_{SD2} + I_{SD4}$.

with a set/reset latch, the complete functionality of DFF can be realized [23].

III. SymFET Latches

In this section, we present several SymFET latch designs that exploit the unique I-V characteristics of SymFETs. While a latch could be useful in and of itself, the work discussed in this section can also be used as a starting point for SymFET flip-flops (to be discussed in Sec. IV-B).

A. Latch based on bell-shaped I-V curve

We first introduce a latch design in Fig. 3(a). Transistors T1 and T2 form the core part of the latch, whereas transistors T3 and T4, referred to as speedup transistors, are only used to improve circuit speed. The latch has three valid input combinations. ($R = 0$ and $\bar{S} = 1$ is not allowed since T1 and T2 are both off in this case.) The operation of the latch (without T3 and T4) can be explained using Fig. 3(b). For example if $R = \bar{S} = 0$, then T1 is off and T2 is on. Consequently the output capacitance is charged and the final output voltage is close to V_{DD}. In $R = 1$ and $\bar{S} = 0$, the circuit is bistable and, depending on the previous Q, the output voltage can be either low or high.

Transient simulation results of the circuit without transistors T3 and T4 are shown in the middle of Fig. 4. The rise and fall times are relatively large, which are due to the small charge and discharge current. Consider the case where the output is initially low, and the input is then set to $R = \bar{S} = 0$. The

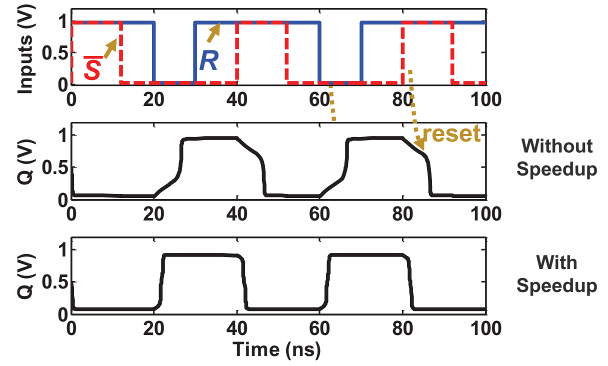

Fig. 4. Input/output waveforms of the latch in Fig. 3 with and without speedup transistors T3 and T4 (V_{DD} =1V, V_B =0.5V, all transistors are minimum size and load is an FO4 inverter).

output capacitance is charged, but the charging current – which is the difference between the currents of T1 and T2 ($I_2 - I_1$ in Fig. 3(b)) – is small for a large range of output voltages.

To improve the transient response of the circuit, transistors T3 and T4 are employed. The BG of T3 (and T4) is connected to its source terminal, and therefore $V_{TG3} - V_{BG3}$ is larger than $V_{TG1} - V_{BG1}$ for a high-level R. This shifts the peak current of the $I_{DS} - V_{DS}$ curve of T3 to a higher V_{DS}. Current summations $I_{DS1} + I_{DS3}$ and $I_{SD2} + I_{SD4}$ have two peaks as seen in Fig. 3(c). Comparing Fig. 3(b) and Fig. 3(c) shows that in principle, the logical functionality of the circuit does not change after adding T3 and T4. The main difference is that charge and discharge currents become higher. In the aforementioned example, if the output node is supposed to be charged, adding T4 increases the charging current from $I_2 - I_1$ to $I_{24} - I_1$ at certain output voltages (where $I_{24} = I_2 + I_4$). On average, the charge current is significantly larger. The effect of employing transistors T3 and T4 can be seen in Fig. 4. The rise time of the circuit is reduced from 5.1 ns to 0.83 ns.

B. Latch based on non-linear resistance of SymFET

The latch in Sec.III-A has only 4 transistors compared with conventional RS latch which has 8 transistors, but the high supply voltage (1V) makes the power consumption not good as desired. We then consider a SymFET RS latch that starts from the simple two-transistor circuit shown in Fig. 5(a). Here, two SymFETs of the same size are used as nonlinear resistors per Fig. 5(b). If inputs A and B have the same logic level, output F will have the same level, independent of whether the resistors are linear or nonlinear. If one input is low and the other input is high, the circuit is bistable and has two stable quiescent points. As shown in Fig. 5(c), the I-V curves of the two transistors have three intersections, one of which is not stable because it lies on the NDR region of the curves. As a result, F can be either low or high when one and only one of the two inputs is high, and is determined by its previous state.

The truth table of the circuit is captured in Fig. 5(d), which clearly shows the resemblance with that of a latch. In fact, adding an inverter (e.g., the SymFET inverter in [11]) to the circuit results in the well-known RS latch as shown in Fig. 6(a). It should be added that the truth table of the new RS latch is slightly different from that of Fig. 6(b) as the input combination of '11' is not allowed in the conventional design.

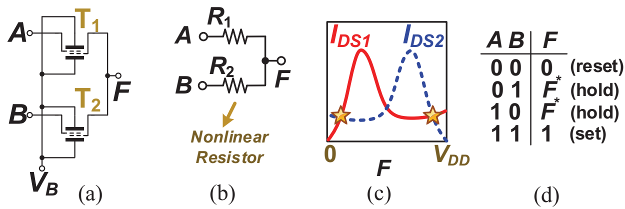

Fig. 5. (a) Two-transistor latch. (b) Model of the circuit. (c) The current of T1 and T2 versus output voltage, when A =0 and $B = V_{DD}$. The stable quiescent points are marked with star. (d) Truth table of the circuit ($F^{\star}$ means the previous F).

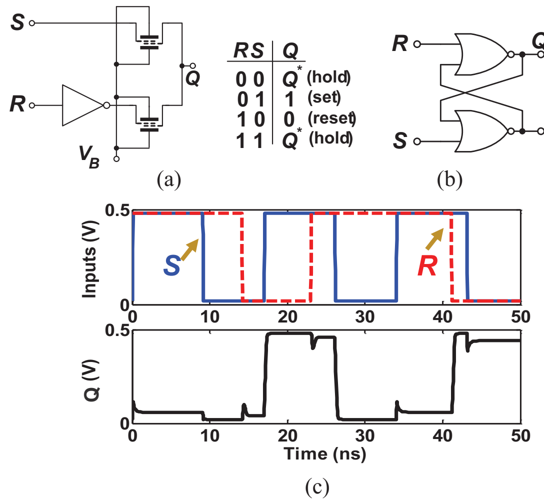

Fig. 6. (a) 4-transistor RS latch and its truth table. (b) Conventional RS latch. (c) Simulation results (V_{DD} =0.5V, $V_B = V_{DD}/2$, all transistors are minimum size and load is an FO4 inverter).

The simulated transient response of the new circuit is shown in Fig. 6(c). The rise time (10%-to-90%) is 0.8 ns.

IV. SymFET MOBILE and DFF

In this section, we consider the design of SymFET DFF. A straightforward way to achieve this is to use NAND gates, inverters, and an RS-latch element described in Sec. III to realize a "conventional" DFF schematic with SymFETs. Though this design requires fewer devices than a conventional CMOS DFF, the final circuit area and power consumption are not as desirable. Another way is based on MOBILE gate which could lead to more efficient design. Below, we first discuss SymFET MOBILE inverter/buffer which forms the basis of DFF, then propose the SymFET MOBILE-based DFF.

A. SymFET MOBILE inverter and buffer

To build MOBILE inverter/buffer, one way is using SymFETs to mimic an RTD. Fig. 7(a) shows a circuit built by placing two SymFETs in parallel. The current passing through the element is the sum of the currents in T1 and T2. As shown in Fig. 7(b), each transistor contributes to one peak in the total current and the N shape curve expected from an RTD is obtained for a properly designated voltage range. Note that the shape of the curve can be tuned by adjusting the bias voltages. By replacing each RTD in Fig. 2 with the SymFET construct in Fig. 7(a), one can obtain a 7 device SymFET mobile inverter with self-latching properties. However, it is possible to design

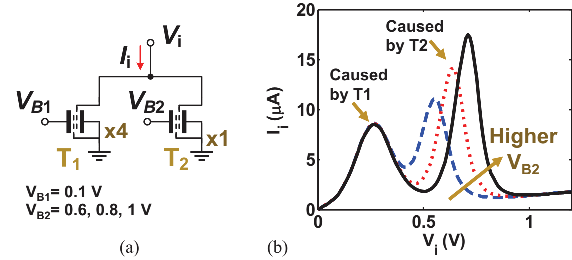

Fig. 7. A circuit (a) to realize RTD-like characteristics (b) with SymFETs.

even more compact MOBILE circuits with SymFETs, which we will elaborate on below. We introduce a 3-device SymFET mobile inverter design as shown in Fig. 8(a). Here, T1 acts as both the switch and D1 while T2 and T3 act as D2 and D3, respectively, in Fig. 2(a). The correct operation of the circuit depends on the sizing of T1-3 and also the bias voltage V_B, which is selected to satisfy the criteria specified for the mobile inverter design in Eq. (1).

The operation of the circuit is summarized below. When input A is low, I_{DS1} is negligible. The size of T3 is twice that of T2 and therefore the peak current of T3 is higher than that of T2 as desired per Eq. (1), resulting in a high-level output. V_B is selected to be 0.4V so that the gate voltage difference of T1 is positive, making the peak current of T1 and T2 higher than that of T3. This ensures that a high-level input will result in a low-level output. Transistor currents are shown in Fig. 8(b) for a high CLK (equal to 0.6V). The circuit is bistable for both input logic levels. Fig. 8(c) illustrates the input/output waveforms of the circuits. Input levels are selected to be 0 and 0.6V, similar to the worst case of output levels. Note that altering A does not change the output, even when CLK is high. However, similar to the RTD mobile inverter, the SymFET mobile inverter cannot hold the output when CLK returns to a low level. As such, the complete functionality of a DFF is not realized.

It is also possible to build a MOBILE buffer following a similar idea to MOBILE inverter. In this case the driving capabilities of the pull-up and pull-down transistors are reversed. Fig. 8(d) shows the schematic of the MOBILE buffer. The operating principles of the SymFET MOBILE buffer is analogous to the MOBILE inverter and we omit the discussion.

B. SymFET D-Type flip-flop

Now we consider the design of SymFET DFF by using the MOBILE buffer/inverter introduced above. Fig. 9(a) shows the schematic of this MOBILE-based DFF. This design uses one MOBILE buffer, an inverter with V_{DD} replaced by CLK, and an RS latch, leading to only 9 devices. The circuit operates as follows. At the rising edge of CLK, in accordance with the data input, the clocked inverter generates a reset pulse, and the MOBILE buffer generates a set pulse. These pulses then switch the RS latch, and the data is stored at the latch output. Even though CLK's falling edge drives the output of the MOBILE gate to a low level, the DFF retains the output value, thus achieving the full DFF operation. Fig. 9(b) shows the waveforms obtained from simulation.

Below, we elaborate on a few unique points related to the MOBILE-based DFF. First, note that when CLK transitions

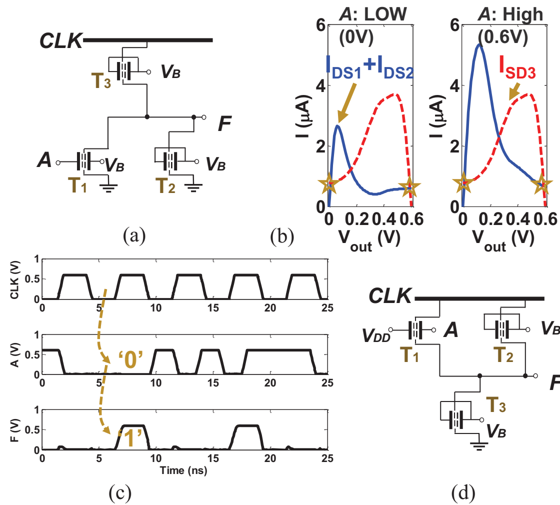

Fig. 8. (a) SymFET MOBILE inverter. (b) Currents of transistors versus output voltage when clock has reached its final value (0.6V); note that for both low and high input levels, the circuit is bistable. (c) Transient simulation of the inverter; F is high, only if A is low at the rising edge of CLK. (d) SymFET MOBILE buffer. V_B=0.4V.

from high to low, the output of the clocked inverter is cut off from the power supply. Astute readers may be concerned with the state of the DFF. However, careful analysis shows that the DFF functions exactly as expected. Specifically, if the output of the clocked inverter is low (and thus the output of the MOBILE buffer is high) before CLK transitions from high to low, the output of the clocked inverter remains at a low level after the transition. Hence, the state of the RS latch transits from set to $hold$ (as both R and S are at low). Now if the output of the clocked inverter is high (and thus the output of the MOBILE buffer is low) before CLK transitions from high to low, the output of the MOBILE buffer remains at a low level and hence the RS latch either goes to $hold$ or remains in $reset$. (Recall that the previous state of the RS latch is $reset$ since the output of the clocked inverter is high.)

Another point pertains to the edge-trigger property. Though changing the input after a rising edge of CLK may change the state of the clocked inverter, the self-latching property of MOBILE buffer guarantees an unchanged output of the latch. As demonstrated in the simulation results in Fig. 9(b), the circuit in Fig. 9(a) indeed realizes the DFF functionality.

V. Evaluation

In this section, we present the performance and power study of the SymFET storage elements introduced in the previous sections. The metrics considered include voltage supply (V_{DD}), peak-to-peak output swing ($V_{o,pp}$), propagation delay (T_d), average dynamic energy for an output switching (E_{DYN}), static power dissipation (P_{STAT}) and total power consumption (P_{TOT}). All data are obtained from HSPICE simulations using the SymFET model discussed in Sec. II-A.

Table I summarizes the values of the considered metrics for the latches and MOBILEs. Note that two different dynamic energy values, depending on whether the circuit is adiabatic (the smaller number) or not (the larger one), are given in Table I for the MOBILE inverter and MOBILE buffer. When CLK goes low, the charge stored at the load capacitance

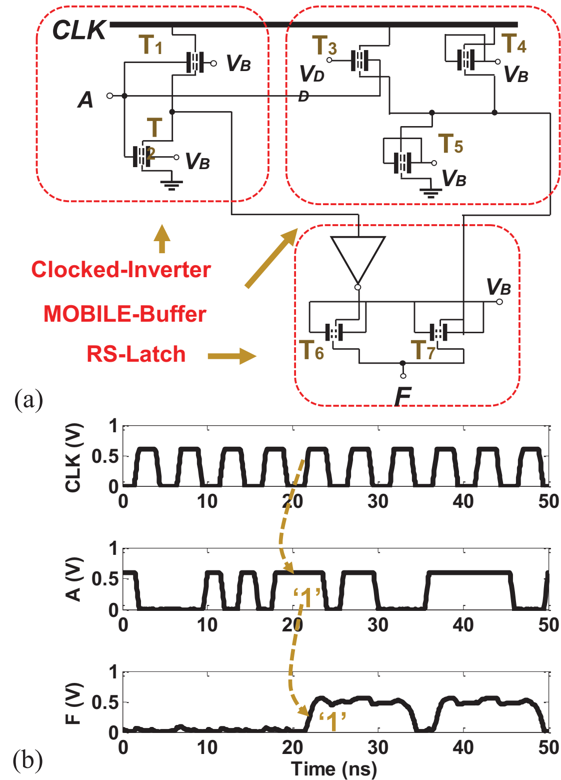

Fig. 9. (a) SymFET MOBILE-based DFF. (b) Simulation results with a FO4 inverter as the load.

returns back to the CLK node. If the CLK generation circuitry is capable of absorbing this charge, the circuit is adiabatic and consumes less energy. On the other hand, the CLK circuit might direct the charge to ground and there will not be any charge recovery. From Table I, one can see that the latch design in Fig. 6 consumes 3X lower power than the latch in Fig. 3. This is mainly due to the fact that the design in Fig. 3 requires a higher supply voltage and has higher static power.

In Table II, the performance, power and area of SymFET DFF based on the conventional topology (built by SymFET Boolean logic gates introduced in [11] and the SymFET latch in Fig. 6(a)) and MOBILE gate in Section IV-B are shown. As a comparison, we also include the corresponding values for a CMOS DFF. The CMOS data are based on the DFF design from [24] and implemented in the 90 nm CMOS technology (ASU predictive technology model [25]). Since we assume the SymFET device with a 100nm-by-100nm size, we opt to compare our SymFET designs with 90 nm CMOS technology. Comparing with 90 nm CMOS technology is also supported by the fact that the SymFET storage elements are likely to be used in a mixed-signal environment (per the diffusion network application discussed in Sec. II-A), where 90 nm CMOS technology is considered to be an advanced technology node. As shown in Table II, SymFET MOBILE-based DFF is slower but consumes less power and area than the CMOS DFF. The power-area efficiency of SymFET DFF could reach $330X$ over CMOS DFF. We should point out that SymFET DFF does consume higher static power, around one order of magnitude, but it is more efficient in terms of dynamic energy.

In applications where diffusion networks or other Gaussian-

TABLE I
PERFORMANCE AND POWER OF LATCHES/MOBILE/DFF

	V_{DD} (V)	$V_{o,pp}$ (V)	T_d (ns)	E_{DYN} (fJ)	P_{STAT} (μW)	P_{TOT} (μW)
Latch Fig.3(a)	1	0.84	$1.2^{\dagger}$	2.2	0.67	0.78
Latch Fig.6(a)	0.6	0.55	$0.41^{\dagger}$	0.37	0.17	0.21
MOBILE Fig.8(a)	$0.6^{\star}$	0.59	0.34	$1.4/0.6^{\ddagger}$	0.21	0.34
MOBILE Fig.8(d)	$0.6^{\star}$	0.59	0.23	$1.2/0.4^{\ddagger}$	0.22	0.29

$\star$: high level of CLK. †: from input to output (from CLK to output for others).
‡: depends on capability of CLK generation circuitry to absorb charge.
Note: All simulations are done with a FO4 inverter as load.

TABLE II
PERFORMANCE AND POWER OF SYMFET DFFS

	V_{DD} (V)	$V_{o,pp}$ (V)	T_d (ns)	P_{TOT} (μW)	PDP (fJ)	$Area^*$ (μm^2)
Conventional SymFET	0.6	0.53	1.44	1.97	2.84	0.68
MOBILE SymFET	$0.6^{\star}$	0.56	1.13	0.54	0.61	0.24
CMOS	1	1	0.21	1.74	0.36	24.9

$*$: assuming total area (including wirings) is twice the area of transistors
$\star$: high level of CLK.
Note: In SPICE simulation, a 100MHz signal is applied to CLK. All simulations are done with a FO4 inverter as load.

function type of processing are called for (e.g., many image processing ones), given the benefit of SymFET based analog circuits has over CMOS (e.g., those reported in [20]), plus the efficiency offered by SymFET DFF as the supporting control module circuitry, SymFET-based systems could offer better power-area-performance tradeoff than CMOS, if desired delay is not demanding. Furthermore, such a SymFET-only system would eliminate the needs for integrating SymFET devices with CMOS devices.

VI. CONCLUSION

We exploited the unique properties of SymFET devices and RTD-like I-V behavior to build sequential gates in several novel topologies. These latches and DFFs are more compact and more efficient in terms of power consumption and area compared with CMOS equivalents. Moreover, this work leads to the possible design of pure-SymFET circuits/applications wherein sequential gates are necessary such as image processing, etc. Though new design methodologies and new benchmarkings will be worked out as emerging tunneling devices (not only SymFETs) continue to evolve and mature with respects to fabrication, models and device structure, this work can still provide insights to both device physicists developing emerging tunneling devices and circuit/system designers investigating new applications based on post-CMOS devices.

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