Behavioral Modeling of Timing Slack Variation in Digital Circuits Due to Power Supply Noise

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***Abstract*—Timing error due to power supply noise (PSN) is a key challenge for design of digital systems. This paper presents an accurate time-domain behavioral model of timing slack variation due to the PSN while accounting for the clock-data compensation (CDC). The accuracy of the model is verified against SPICE for complex designs including AES engine and LEON3 processor. As a case study, the model is used for time-domain co-simulation of power distribution network (PDN) and LEON3 processor with circuit-based noise tolerance techniques. The analysis shows that the model helps reduce pessimism in estimated timing slack by considering effects of PSN and CDC.**

I. Introduction

Energy efficient system design has emerged as a key design challenge due to ever-diminishing power budget. To this end, it is desired to operate such devices with the minimum voltage or timing margin in order to reduce wasted power. It is critical to choose proper voltage margin based on timing slack, the difference between clock period and critical path delay, for energy efficient digital system design.

Static timing analysis (STA) is used to predict timing slack given peak voltage droop based on the worst case workload condition. This worst case based approach has long been used to guarantee safe operation adding enough margins additively in every levels of PDN design stages [1], [2]. Such an additive margin approach might result in over-design (energy inefficient design) since peak voltage droop does not necessarily mean long enough DC voltage droop which produces timing error. More detailed analysis from circuit level transient simulation is necessary to avoid over-design.

However, increasing design complexity limits circuit-level transient power supply noise (PSN) simulation due to considerable simulation time, therefore, necessitate behavioral simulation of timing slack variation due to transient PSN. This paper presents an accurate time-domain behavioral model of timing slack variation under transient PSN. The proposed model accounts for the non-linear delay sensitivity to supply voltage to estimate effects of large PSN. The methodology allows cascaded models for sub-circuit blocks to handle the time varying input delay and clock period. This functionality enables us to model heterogeneous design with components having different delay sensitivity to supply voltage as well as experiencing different PSN waveforms. The cascading capability also helps consider the effect of jitter in the clock source. The model is integrated with the design flow and applied to large designs - LEON3 processor [3] and AES encryption engine [4]. The analysis shows less than 4% error compared to SPICE simulation over a wide noise frequency range when 20% peak to peak noise is applied. As a case study, the model is used to simulate LEON3 processor with/without PSN tolerance techniques (time-borrowing) given supply voltage waveform from PDN while sweeping on-chip decoupling capacitor value. The simulation shows the ability of model to consider effects of design methods like decoupling capacitor selection, time borrowing, and pulsed clocking [1], [2], [5-8]. The case study demonstrates that the model helps reduce pessimism in high-level estimation of timing slack by considering effects of PSN and CDC.

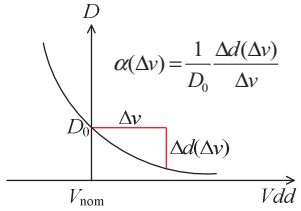

Fig. 1. Circuit delay (D) vs. supply voltage (Vdd) plot.

The rest of the paper is organized as follows: Section II presents the modeling method; Section III shows the modeling accuracy; Section IV presents the application of the model for co-simulation; and Section V summarizes the paper.

II. PSN Induced Timing Slack Modeling

A. PSN Induced Jitter Model

Recent work by X. Wang and A. Martin [9] introduced alpha model for behavioral jitter simulation. In their work, delay variation (Δd), function of supply voltage difference (Δv) from nominal voltage is obtained from circuit level simulation. The delay sensitivity to supply voltage (α) can be calculated by:

$$\alpha = \frac{1}{D_0}\lim_{\Delta v\to 0}\frac{\Delta d(\Delta v)}{\Delta v} \quad (1)$$

where, D_0 is circuit delay at the nominal voltage.

PSN induced jitter (PSNIJ), referred to as $J(t)$, now can be obtained by integration of the supply difference ($\Delta v(t)$) over the delay period (D_0) multiplied by the delay sensitivity to supply voltage (α) as shown below:

$$J(t) = J\big(t;\alpha,D_0,\Delta v(t)\big) = \alpha\int_{t-D_0}^{t}\Delta v(\tau)d\tau. \quad (2)$$

As in (2), we define PSNIJ as a function of t parameterized by α and D_0 given $\Delta v(t)$. α and D_0 are the process and circuit dependent parameters and $\Delta v(t)$ should be given by the engineers from circuit level simulation with PDN under PSN.

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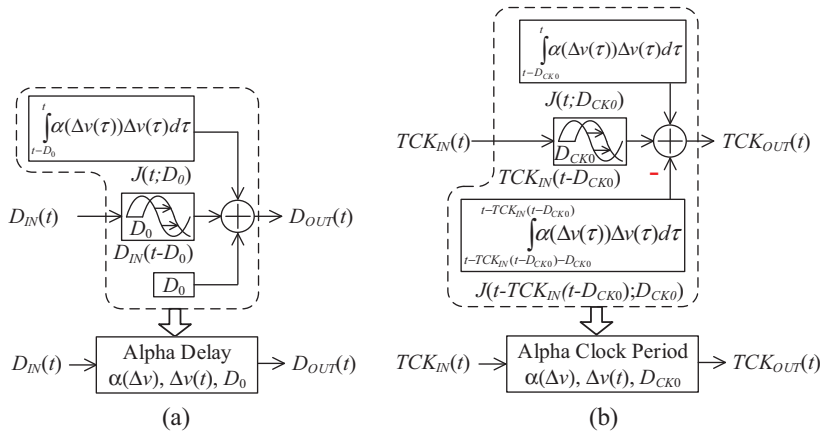

Fig. 2. Behavioral model of (a) PSNID and (b) PSNICP

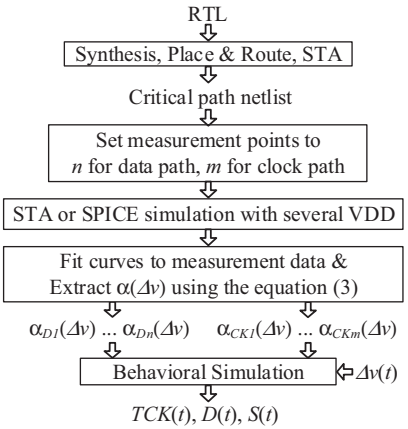

Fig. 3. Design flow for the behavioral simulation

B. Modeling for Large PSN

The linearity assumption for α in [9] is valid only when $\Delta v(t)$ is sufficiently smaller than nominal voltage over the entire time period. To account for the large voltage changes, we propose a non-linear delay sensitivity ($\alpha(\Delta v)$) as:

$$\alpha(\Delta v) = \begin{cases} \frac{1}{D_0}\lim_{\Delta v\to 0}\frac{\Delta d(\Delta v)}{\Delta v}, & \Delta v = 0 \\ \frac{1}{D_0}\frac{\Delta d(\Delta v)}{\Delta v}, & otherwise. \end{cases} \quad (3)$$

Since $\alpha(\Delta v)$ is now a voltage dependent variable, new PSIJ ($J(t)$) considering large power supply noise has to have $\alpha(\Delta v)$ inside the integral as follows:

$$J\big(t;\alpha(\Delta v),D_0,\Delta v(t)\big) = \int_{t-D_0}^{t}\alpha(\Delta v(\tau))\Delta v(\tau)d\tau. \quad (4)$$

Note, that $\alpha(\Delta v)$ in (3) is not the derivatives of Δd at Δv, but the slope between Δv and 0 instead as shown in Fig. 1. This is because PSNIJ is calculated using the integration over the fixed period D_0 which is the circuit delay from nominal voltage when Δv=0. This can be easily understood by setting $\Delta v(t)$ =C, where C is a constant. When DC voltage shift (C) occurs, PSNIJ becomes Δd(C) as shown in Fig. 1 and this value should be the same with the result obtained from (3) and (4) as follows:

$$J(t;\alpha(C),D_0,C) = \int_{t-D_0}^{t}\alpha(C)C d\tau = D_0\alpha(C)\mathrm{C} = D_0\frac{1}{D_0}\frac{\Delta d(C)}{C}C = \Delta d(C).$$

. In the following section, we denote $J(t;\ \alpha(\Delta v),\ D_0,\ \Delta v(t))$ as $J(t;\ D_0)$ for brevity.

C. PSN Induced Delay Model

PSN induced delay (PSNID) can be obtained by adding nominal delay and PSNIJ. To enable cascading, we also consider the input delay propagation. Therefore, PSNID considering input delay propagation will be the addition of PSNIJ ($J(t;\ D_0)$), propagation of the input delay ($D_{IN}(t)$) and nominal delay (D_0):

$$D_{OUT}(t) = J(t;D_0) + D_{IN}(t-D_0) + D_0 \quad (5)$$

Block diagram view of this model is illustrated in Fig. 2(a).

D. PSN Induced Clock Period Model

Clock period is the delay difference from the current rising edge to the previous rising edge of the clock. Since clock distribution delay is not negligible in today's digital design, clock period ($TCK(t)$) of the clock sink net can be seen as the input clock period ($TCK_{IN}(t)$) shifted by the clock distribution delay (D_{CK0}) as follows:

$$TCK_{OUT}(t) = TCK_{IN}(t-D_{CK0}). \quad (6)$$

In existence of PSN, PSNIJ of the current rising edge elongates clock period and PSNIJ of the previous rising edge contracts clock period. Thus, PSN induced clock period (PSNICP) can be written as:

$$TCK_{OUT}(t) = TCK_{IN}(t-D_{CK0}) + J(t;D_{CK0}) - J(t-TCK_{IN}(t-D_{CK0});D_{CK0}). \quad (7)$$

$J(t;\ D_{CK0})$ is PSNIJ term at current time t and $J(t\text{-}\ TCK_{IN}(t\text{-}D_{CK0});\ D_{CK0})$ is PSNIJ term at previous rising edge of the clock. Note that the last term in (7) should not be obtained by simple function shift operation as $TCK_{IN}(t)$ does not need to be a constant value. For example, clock period generated by the PLL having jitter is not the constant value. Block diagram view for PSNICP model is illustrated in Fig. 2(b).

E. PSN Induced Timing Slack Model

Using our proposed PSNID and PSNICP model, we can calculate accurate timing slack variation under PSN. PSN induced slack (PSNIS) $S(t)$ can be written as follows:

$$S(t) = TCK_{OUT}(t) - D_{OUT}(t) \quad (8)$$

III. Validation

A. Integration of Models in the Design Flow

We have integrated the PSNID, PSNICP and PSNIS models in the standard design flow (Fig. 3). Given a design, after the RTL, synthesis, and place & route steps, we obtain the gate-level netlist. Based on static timing analysis (STA) results, we obtain simplified version of gate level netlists containing critical path and clock tree. We set the delay measurement points to n for the critical path and m for the clock tree.

There are 2 options for the delay measurements. First, we can run several STAs with different supply voltage timing

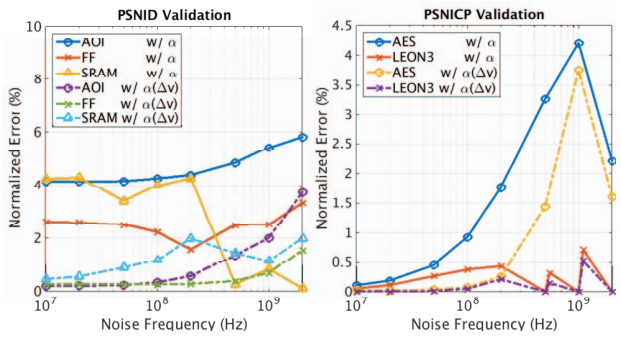

Fig. 4. (a) PSNID and (b) PSNICP validation with SPICE simulation

libraries. If PDK provider does not provide fine grain supply voltage timing libraries, simulation accuracy might be degraded in return for the convenience. Another option is to run SPICE simulation. The size of the critical path netlist is small and one or two cycles transient simulation is necessary for each supply voltage, hence, the overhead is very small.

Once we have all the delay measurement points for several voltage levels that we are interested in, we fit curves to the data (delay vs. supply voltage plot) and obtain $\alpha(\Delta v)$ for all sub-circuit blocks using (3). Then, we can perform behavioral simulation given PSN waveforms. The input for the behavioral simulation will be the time-domain PSN waveforms, input clock period, $\alpha(\Delta v)$ parameters and nominal delays for both critical path and clock tree, and the outputs are the time-domain PSNID, PSNICP and PSNIS. For the exhaustive simulation, one might include several critical paths at different temperature corners.

B. Model Validation

We use AES (Verilog) and LEON3 (VHDL) as example designs and generate gate level netlists after performing P & R. 1.0V 45nm Predictive Technology Model based library and 1.5V 130nm Global Foundries PDK are used for AES and LEON3, respectively. For the verification, we apply sinusoidal noise with varying peak-to-peak noise amplitude and compare the values (PSNID and PSNICP) from our behavioral simulation and that from SPICE simulation. The error increases with higher noise magnitude and the normalized peak percent error for the 20% variation case is reported for validation. The errors for smaller noise magnitudes are even less and omitted for brevity.

1) PSNID Validation: As examples of PSNID validation, we consider the AOI standard cell, flip-flop and SRAM as examples. Fig. 4(a) shows good correlation between our method and SPICE simulation. Behavioral simulation using linear α is shown as a reference. The proposed method using non-linear $\alpha(\Delta v)$ has smaller error than the case of using linear α. The percentage error increases marginally at higher noise frequency but remains within 4%.

2) PSNID Validation: For PSNICP validation, we use clock tree from AES and LEON3 design. Clock period (TCK_{IN}) of 625ps and 2ns, and clock distribution delay (D_{CK0}) 338ps and 518ps are used for AES and LEON3, respectively.

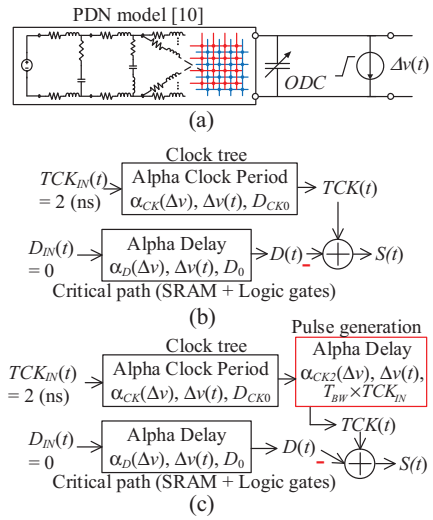

Fig. 5. (a) Step response simulation model with PDN. Behavioral simulation models for (b) LEON3, (c) LEON3 with time borrowing using locally generated pulse

Fig. 4(b) proves effectiveness of PSNICP modeling which generates at most 4% error.

C. Run Time Comparison

Run time of our model depends on simulation time step and desired simulation time. Rule of thumb of choosing simulation time step is to set the parameter around 1/1000 of minimum nominal delay among behavioral modeling set-up. For the comparison, we set the simulation time step to be 1ps for both AES and LEON3 behavioral simulation. Table I summarizes CPU run time of a transient simulation for SPICE and the proposed behavioral method implemented in MATLAB. As expected, the run time is 10,000x faster compared to SPICE simulation for our case study.

IV. Case Study

We apply our model to simulate LEON3 processor with/without PSN tolerance techniques (time-borrowing) given supply voltage waveform from PDN while sweeping on-chip decoupling capacitor value. As an example PDN, we consider the model described in [10] (Fig. 5(a)). The used the same parameters except the on-die capacitor (ODC) value. We obtain supply voltage difference waveform $\Delta v(t)$ by applying step current flow at the on-chip PDN. We perform simulations considering different ODC values and use these waveforms as inputs for behavioral simulation of the timing slack for the LEON3 design.

We perform behavioral simulations for two different LEON3 design. First, we consider the behavioral model for the

TABLE I
CPU Run Time Comparison

(# Transistors)	AES(3354)		LEON3(61383)	
Transient simulation time	130 ns	40 ns	130 ns	40 ns
SPICE	1370 s	642 s	11255 s	5364 s
Proposed model in MATLAB	0.97 s	0.30 s	0.97 s	0.30 s

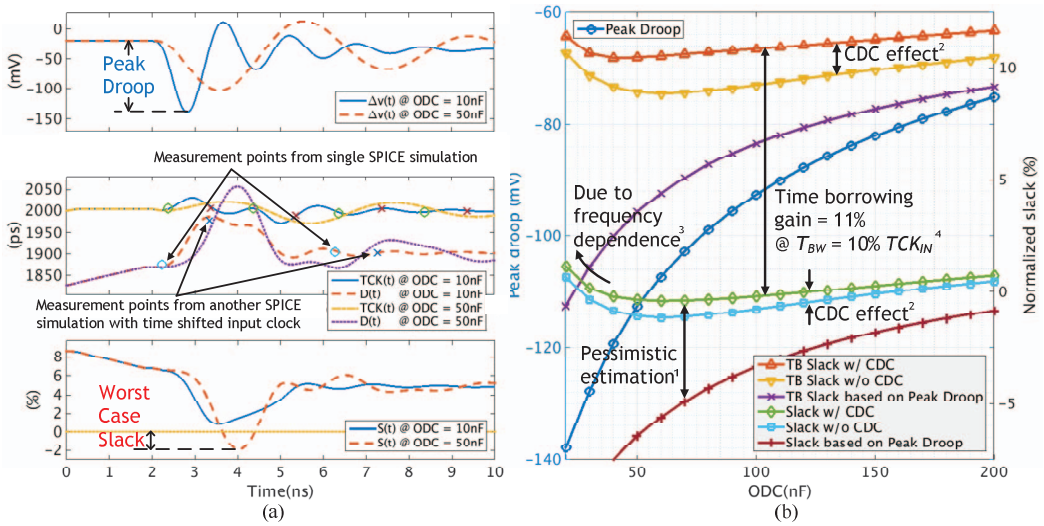

Fig. 6. (a) Behavioral simulation waveform for LEON3 at ODC = 10nF. (b) Peak droop voltage on left axis and normalized worst slack on right axis.

default LEON3 design as shown in Fig. 5(b). Alpha clock period block represents PSNICP of the clock tree and alpha delay block represents PSNID of the critical path delay. Next, we consider a well-known PSN tolerance technique to the LEON3 design – time-borrowing (TB) using pulsed latches[5-7]. In TB, the pulsed latches are used in the timing critical path to allow data transition even after a clock edge. This allows a pipeline stage to borrow time (pulse width of the clock) from the following stage to eliminate timing errors under PSN.

We consider the pulsed-clock is generated locally by using pulse-generation circuits within the clock network [8]. As shown in Fig. 5(c), the locally generated pulse width is modeled as alpha delay model with nominal delay of T_{BW}*TCK_{IN}, where T_{BW} is the TB window and TCK_{IN} is the input clock period.

For all simulations, input clock period (TCK_{IN}) of 2ns and clock distribution delay (D_{CK0}) of 518ps, critical path delay (D_0) of 1827ps, and time borrowing window (T_{BW}) of 10% clock period are used. Fig. 6(a) shows sample waveforms of PSNICP $TCK(t)$, PSNID $D(t)$ and PSNIS $S(t)$ generated from this behavioral simulation for different ODC values. Peak supply voltage droop and the worst case (minimum) slack of $S(t)$ are measured from the waveforms (more positive slack is better).

Fig. 6(b) shows the estimated timing slacks for different ODC. Four meaningful phenomena are observed from this simulation. First, we see the timing slack based on the peak droop voltage provides a very pessimistic estimation. As shown in this figure, the gap between the slack with CDC and slack based on peak droop is huge and becomes large as ODC value decreases. Second, PSNIS considering CDC (with both PSNID and PSNICP) is more positive than PSNIS without CDC (only with PSNID) showing the helpful effect of CDC (similar observation as in [2]). Third, we can see that at low ODC range, increasing ODC can reduce timing slack even if the peak voltage droop reduces. This is because increasing ODC reduces the noise frequency (see Fig. 6(a)) making slack more sensitive to PSN. If ODC is increased further, the reduced peak droop helps increase the slack again. This shows the need to consider the accurate timing slack model to better optimize PDN, specially, under tight ODC budget. Finally, we observe performance improvement through circuit techniques like time borrowing can be estimated using our behavioral model.

V. Conclusion

This paper presents an accurate behavioral modeling method for transient timing slack variation under power supply noise. The accuracy improvement comes from considerations of both delay variation and clock period modulation under PSN, and the use of non-linear delay sensitivity over the supply voltage. The proposed model is integrated within a standard design flow and showed less than 4% error when compared with SPICE simulation. The application of the behavioral model for co-simulation of PDN and LEON3 processor demonstrate the ability of the model to capture effects of PDN or circuit design choices on timing slack. In particular, we observe the proposed model helps reduce pessimism. As PSN is becoming a limiting factor for voltage/timing margin, the proposed model can help accurately control design margin and improve energy-efficiency.

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