A Digital Processor Architecture for Combined EEG/EMG Falling Risk Prediction

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***Abstract* — The brain signal anticipates the voluntary movement with patterns that can be detected even 500ms before the occurrence. This paper presents a digital signal processing unit which implements a real-time algorithm for falling risk prediction. The system architecture is designed to operate with digitized data samples from 8 EMG (limbs) and 8 EEG (motor-cortex) channels and, through their combining, provides 1 bit outputs for the early detection of unintentional movements. The digital architecture is validated on an FPGA to determine resources utilization, related timing constraints and performance figures of a dedicated real-time ASIC implementation for wearable applications. The system occupies 85.95% ALMs, 43283 ALUTs, 73.0% registers, 9.9% block memory of an Altera Cyclone V FPGA for a processing latency lower than 1ms. Outputs are available in 56ms, within the time limit of 300ms, enabling decision taking for active control. Comparisons between Matlab (used as golden reference) and measured FPGA outputs outline a very low residual numerical error of about 0.012% (worst case) despite the higher float precision of Matlab simulations and losses due to mandatory dataset conversion for validation.**

Keywords—Fall prevention, EEG, EMG, MRPs, FPGA.

I. INTRODUCTION

Although walking may seem to be a simple task, it is actually a complex motor activity, which requires muscular strength, joint mobility and coordination of the central nervous system. Due to neurological diseases, muscular deformities, ageing and further numerous factors, normal gait frequently tends to degenerate into gait disorders, which constitute a contributive intrinsic falling cause, heavily increasing the risk of falling. Fallings are currently an important problem for public health: 28–35% of people aged 65 years and above fall and, as consequence, each year more than 424000 fall events are fatal [1]. Approximately 1 out of 10 falls results in a serious injury, which can lead (among the others) to hip fractures, subdural hematoma and further serious soft tissue, or head injuries [2]. Moreover, the economic impact of this phenomenon is impressive: 43.8 billion dollars are estimated to be used in fall-related medical care expenditures by 2020 [3].

The monitoring, the analysis and the early detection of these gait disorders and even the prediction of fault movements represent a breakthrough in the field of the fall prevention during gait. Despite the extensive research in this field, the developed tools for fall risk have not been successful in predicting and preventing falls [4]. Indeed, although fall detection technology is now mature (detectors for domestic use can be implemented using artificial vision techniques, tri-axial gyroscopes and accelerators, Microsoft Kinect's infrared sensors, floor vibrations and sounds and numerous others) [3], fall prevention solutions are still far to be implemented.. According to the fall prevention and detection, surveyed by Y.S. Delahoz (2014) [3], remarkable alternative solutions involve pulse-Doppler range control radar, Microsoft Kinect, load distribution sensors and clinical fall-risk assessment tools (TUG, POMA, PPA, etc.) for low-invasivity tools while laser rangefinders combined with exoskeletons, 3D accelerometers and gyroscopes, force sensor and pressure sensors are exploited for higher obtrusive applications. Those systems are invasive with respect to the everyday life and not enough precise (precision depends on the person health).

In the last ten years from neurological studies it came out that the most accurate method for fall prediction is based on real time monitoring of EEG and EMG signals and, in particular, on the combined analysis of muscular movement and its brain processing. This analysis can be performed by checking EEG Movement Related Potentials (MRP, detectable in particular frequency bands) anticipating muscle activations [5-7]. However, currently none of the above remarked solutions enable such analysis: only partial solutions have been proposed in literature. Some systems measure individually EEG or EMG; others measure both of them, but only on a few EEG/EMG electrodes without relative synchronization, using an external clock and delivering filtered data to be post-processed and not handled in real time [8]. The system presented in this work is the first hardware implementation of a fall prediction (and prevention) algorithm based on the combination of EEG and EMG bio signals.

This paper, presents the design, testing and validation of a complete and autonomous digital back-end architecture for fall prediction in the everyday life, based on the combination of synchronized EEG and EMG. The architecture combines both brain and muscular signals within a time limit of 300ms to take decision for processing and eventual corrective actions on the muscles. In the aim of a future ASIC implementation, the architecture has been validated on FPGA (Altera Cyclone V), resulting in a latency performance of 56ms using a system clock frequency of 8MHz, enough to meet application-specific real-time constraints. The paper is structured as follows. Sec. II introduces the basic principle for fall prevention and the high-level description of the algorithm. Sec. III, discusses the FPGA hardware implementation. Sec. IV presents experimental data from testing and validation of the algorithm using EEG/EMG data recorded with commercial wireless systems over 10 young men and women, with special care to timing, numerical precision and resources utilization, which are crucial points in this application.

II. Fall Risk Prediction

A. Principle of Operation

The cortical implication during gait is still unclear and it is far to be elucidated. This is mainly due to the complexity of the gait, which involves a multitude of muscles in a largely automatic and natural way. Nevertheless, literature studies [9, 10] and experimental analysis [5, 11] demonstrate the presence of EEG Movement Related Potentials (MRPs) detectable in the motor cortex and coupled to the intentional movement. In this contribution, we mainly focus on three premotor potentials: Bereitschaftspotential (BP), μ and β rhythms that can be detected in the motor-cortex area even one second before the muscle activation in the band of 2–5Hz, 7–12Hz, and 13–30Hz respectively. In movement disorders, mobility impairment is indicated by an altered modulation of the MRPs as well as a mismatch between the MRPs and the movement: MRPs represent a walking pattern of the voluntary movements. Fig. 1 briefly presents the architecture of the proposed digital processor, underlining the main sub-system blocks for the highly parallelized processing of the EEG and EMG signals. The subsystem used to perform this analysis is based on the real-time combination of synchronous EEG and EMG wireless data. Once a movement is detected, a time-frequency analysis is performed on the EEG data preceding the movement (typically 500ms before the muscle contraction) in order to compute the EEG and EMG signal correlation. In this regard, the EMG data is considered for the parallel calculation of the co-contraction index among agonist-antagonist muscles: indeed, high EMG co-contraction time during gait (larger than 500/600ms depending on the subject) is a further significant index of unbalance and instability. On the other hand, MRPs detection can be implemented through a threshold based time-frequency approach. Using these three results in parallel, the system automatically determines critical situations. According to [12], where a study on 125 subjects is presented (45 "fallers" and 80 "non-fallers" with an average age of 74 years old), it was found that a reaction time of 300ms or lower returns a probability $p <$ 0.01 of falling. Therefore, if the system reacts within this time limit and delivers a corrective action, the fall can be avoided. Our idea is to electrically stimulate the antagonist limb muscles in order to favor the postural correction, drastically reducing the probability of fall. The electrostimulation sub-system (including a semantic reasoner) is part of our future works.

B. Algorithm Description

Eight EEG (according to the international 10-20 system T_3, T_4, C_3, C_4, C_Z, P_3, P_4, O_2, – 500Hz and 24bit resolution) and as many EMG channels (Gastrocnemius, Tibialis, Rectus and Biceps Femoralis of both the legs – 500Hz sampling rate and 16bit resolution) are synchronously collected by a wireless and wearable recording systems. Once both bio-signals are available for processing, EMG and EEG follow two different processing branches.

In the present application all EMG signal samples are not necessary but it is enough to consider the part regarding muscle contraction. For this aim, a trigger signal is extracted from EMG raw data using a dynamic-threshold approach. The trigger signal is computed as follows. First, the EMG signal is rectified,

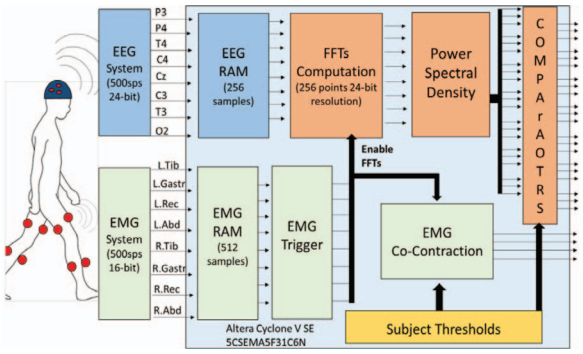

Fig. 1. Architecture of the proposed digital processor. EEG and EMG signals are wirelessly collected by a central unit which includes an implementation of the proposed architecture, here validated on an FPGA.

squared and stored in an M samples shift-register (in our algorithm M = 512, that is 1s data). The mean value of all register samples (global average) is therefore directly the EMG power in the M samples window and it is used as threshold. A second mean value (local average) is computed on the last N samples (i.e., corresponding to just a part of the complete M samples shift register, being $N<M$, in our design N = 128) and compared with the threshold.

As a new EMG sample arrives from an external wireless receiver, both global and local average are refreshed, making the thresholding scheme dynamic. The EMG trigger rises and stays high only if the local power is larger than the dynamic global average threshold. The main advantage of this approach is that action signal is heavily compressed and unambiguous (only a single bit trigger signal per muscle) and at the same time the EMG data samples and trend are not lost.

For the EEG part running in parallel with respect to the EMG one, the time-frequency analysis is run on seven motor-cortex channels only (T_3, T_4, C_3, C_4, C_Z, P_3, P_4), while the occipital one (O_2) is used for noise reduction. As soon as new EEG samples arrive, data are stored in a 256 samples register. When a coupled EMG rising edge is detected, a 256 points 24bit resolution Fast Fourier Transform (FFT) is computed on the previous 256 EEG samples stored into the register. The cortical involvement is opposite with respect to the movement performed: if a right limb movement is detected (right Gastrocnemius), the analysis is performed on left motor-cortex channels (C_z, C_3, T_7, P_3) and vice versa (left Gastrocnemius triggers C_z, C_4, T_8, P_4, note that since C_z is a central channel is triggered by both). The FFT output data are processed to compute the square magnitude and the appropriate frequency components summed in order to calculate the spectral powers in the MRPs bands. When the EMG trigger arrives, the EEG power levels in the MRPs band are referred to approximately 500ms before the movement occurs.

The obtained power levels for each EEG channels are then compared to fixed thresholds (which need to be trimmed on the subject) in order to evaluate the voluntariness of the EMG contraction. Thresholds are customized on the individual after a period of learning (the subjects were asked to rest for 1 minute). Fig. 2 further schematizes the algorithm through a two steps example.

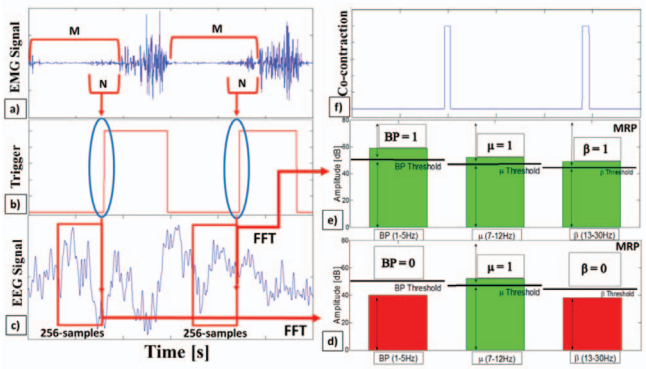

Fig. 2. Example operation of the algorithm for a two step recording: from EMG data (right Gastroc., 2.a), the trigger is exctracted (2.b). When an EMG trigger rising edges occur, the 256 points FFT is computed on cross channels (i.e., C_3, 2.c) for the extraction of MRPs (2.d and 2.e). The EMG co-contraction (2.f) is calculated through the agonist limb muscle (right Tibialis).

First, the EMG raw data (i.e. right Gastrocnemius Fig 2.a) are processed to generate the trigger (Fig. 2.b). When a trigger rising edge is detected, the EEG raw data referring to the contra-lateral motor cortex hemisphere (i.e., C_3, Fig. 2.c) are processed. The FFT is computed in the 500ms window preceding the muscle contraction and the MRPs are extracted. Fig. 2.d and 2.e show the MRP power levels referring to the first muscle activation and compare them to fixed thresholds. In parallel, the co-contraction exploiting the agonist limb muscle (i.e., right Tibialis) is calculated (Fig. 2.e). In [6-8] a more detailed description including experimental setup, signal processing and testing on Matlab is presented.

III. FPGA Architecture

This section is devoted to the implementation of the above algorithm on the Altera Cyclone V SE 5CSEMA5F31C6N FPGA, in order to validate it towards a portable and efficient ASIC platform performing fall prediction during gait. The algorithm has been implemented using the VHDL code through the Altera Quartus II development studio, and a positive logic.

A. Processor System-level Design

The input-output interface of our design was introduced in Fig.1. It is characterized by 16 bio-signals inputs (eight 16bit EMG and eight 24bit EEG) and 25 outputs (BP, μ and β 1bit flags for the seven EEG motor-cortex channels and 4 co-contraction 1bit signals). Fig. 3 shows a simplified block scheme of the system. The system clock is set to 8.19209MHz (signal `8 MHz CLK`), obtained with an on-chip Phase-Locked Loop (PLL, block named `PLL`) from the embedded 50MHz oscillator (`50 MHz CLK`). The direct use of the embedded 50MHz clock was declined because the propagation delay of 64bit adders used to compute EMG thresholds were larger than the clock period. All the computations are run assuming a two's complement notation. Four global signals are used: i) `Reset`, an asynchronous reset (derived from the `Reset KEY` input), ii) `Enable SW`, an enable signal which freezes the processing, iii) `500Hz CLK`, an input data clock signal from the EMG and EEG channels (500Hz frequency), iv) `8 MHz CLK`, a 8.19209MHz system clock obtained by the on-chip PLL. Due to the limited register resources and to the huge amount of data to be processed, it was impossible to use shift registers in the implementation. Indeed, considering that for each couple of EMG and EEG channels three registers are necessary respectively of 128 (32bit words), 256 (64bit words) and 512 (32bit words) rows only for processing, 36864 1bit register would be required only for one EEG/EMG chain, resulting in approximately 295k 1bit registers overall, largely beyond the limits of the FPGA. Moreover, the unfeasibility of this solution is strengthened by the necessary additional memory for the testing and validation phase in order to load offline known data and to save the results. Consequently, the shift registers, FIFO and temporary storage, have been implemented using RAM and related address counters. In the complete system, eight EMG and seven EEG processing branches are parallely replicated on the FPGA, as this is a hard requirement. Indeed, according to the above-mentioned algorithm, EEG and EMG follow two different and independent processing branches. In the following sub-section, we present the processing data path for a generic combined EMG and EEG channel. These are successively combined at top-level to determine voluntary contraction against each channel 1bit respective output. Fig. 3, shows a schematic of a single processing channel comprising both EMG and EEG branches.

B. EMG Processing Branch

Firstly, EMG samples (`EMG_Data`) are squared by an asynchronous squarer and passed to two separate FSM, `Global Power FSM` and `Local Power FSM` (Fig. 3), to calculate in parallel, respectively, the dynamic threshold (global average) and the local power (local average). These FSM work similarly and are respectively based on two block RAM (`Global Threshold` and `Local Threshold Block RAM` of $M = 512$ and $N = 128$, 32bit words) in which the new squared EMG samples are written using a loop address counter (see detail scheme on the right in Fig. 3), inherently providing a FIFO-like functionality.

The EMG powers are dynamically refreshed by the FSMs which implement an ad-hoc sequencing. After `Reset` is asserted, RAMs, the address loop counter and the powers (variable `Sum` in the detail box) are reset, if `Enable SW = '1'` then the FSM waits for new EMG sample. When a new EMG sample arrives (`500Hz CLK = '1'`) the last inserted sample is pointed and "pop" (512th and 128th for, respectively, `Global Power` and `Local Power Block RAM`). Then the read sample is subtracted and the new sample is added to refresh the overall power `Sum` within the window. Finally, the FSM overwrites the RAM word with the new data and then waits for `500Hz CLK = '0'`. The two FSMs differ only because the overall sum is divided by 128 (i.e., a 7bit right shift) for the local power and by 512 (i.e., a 9bit right shift). An asynchronous 64bit comparator (>) compares the powers calculated in parallel by the two blocks (`THR` and `Local THR`). `Local THR` is also compared to a fixed threshold (evaluated on the subject resting) that prevents unpredictable

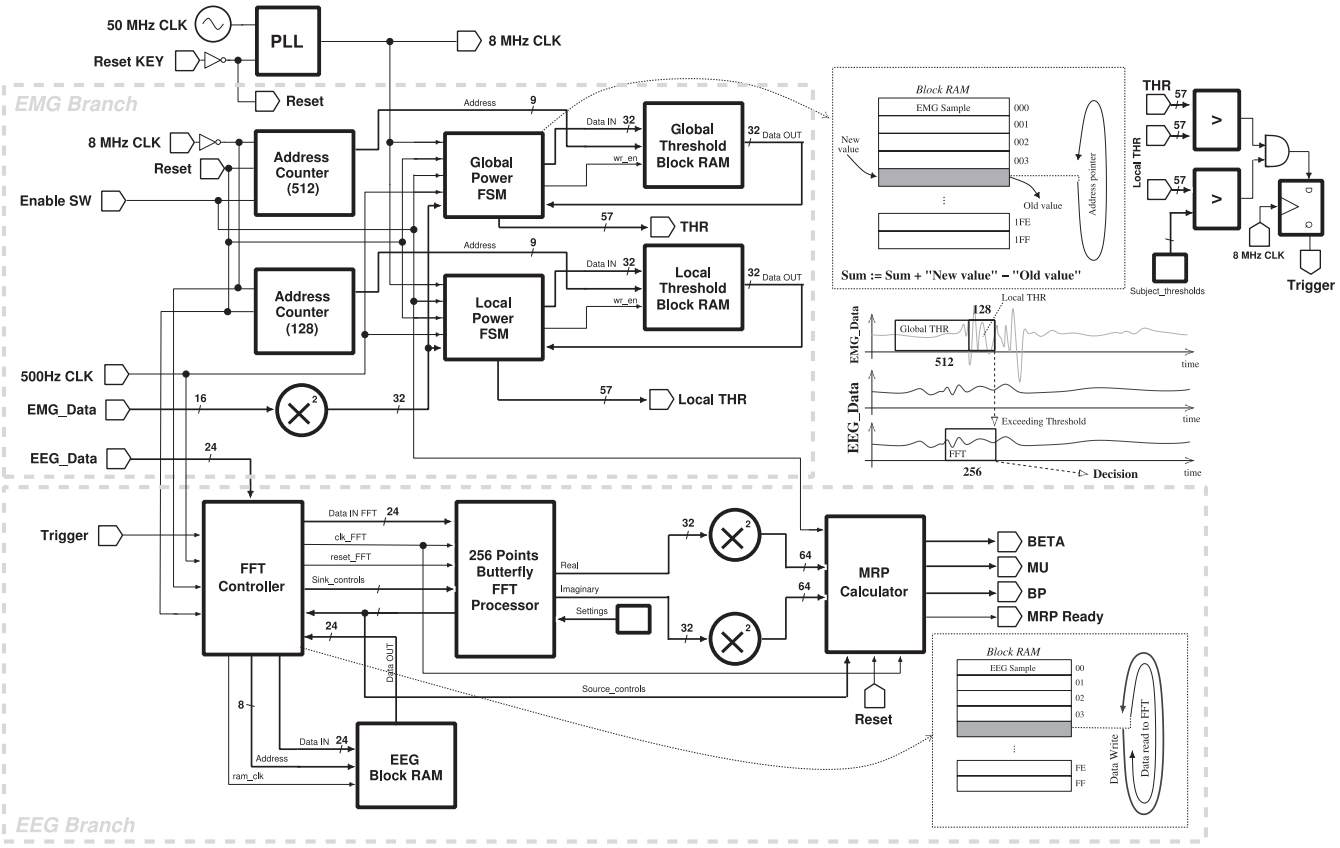

Fig. 3. Schematic of a single processing channel comprising both the EMG and the EEG processing branches.

behavior due to noise when the subject stops walking. The output of the comparator is the 1bit EMG trigger (signal Trigger), used both in the EEG computation to enable the time-frequency analysis and in the co-contraction calculation.

The co-contraction signal is obtained by computing an AND logic operation on agonist-antagonist coupled muscles. The adopted approach allows the efficient calculation of the powers in the desired windows, without necessarily having to re-compute, at each 8MHz clock rising edge, the overall sum of the RAMs.

C. *EEG Processing Branch*

The EEG branch comprises a 256 points 24bit resolution FFT processor based on a butterfly structure (`256 Points Butterfly FFT Processor`). The 256 EEG samples to be transformed are dynamically stored in a 256 24bit words RAM (`EEG Block RAM`) addressed by a loop address counter in the `FFT Controller`.

When an EMG rising edge arrives, it enables the time-frequency analysis on the coupled EEG channels: EEG samples are sequentially read and passed to the butterfly structure, which the FFT is computed in less than 1ms. The `FFT Controller` controls the signal for the FFT processor and generates a dedicated clock (`clk_fft`) at 4MHz. The FSM, first waits to detect a `500Hz CLK` rising edge, then it generates the clock `ram_clk` (which is the negated system clock), gated by an internal enable signal. Here, the enable signal is brought high so that two clock pulses are given to the RAM to write the incoming EEG data (`EEG_Data`). Then, the FSM implements a first check on the coupled EMG trigger signal. If `Trigger` rises to `'1'` the machine goes next, otherwise the machine waits that `500Hz CLK` is low again and returns to the initial state. If a `Trigger` rising edge is detected, the 256 samples stored into the RAM are passed the FFT block by properly temporizing the `Sink_controls` signals through a series of dedicated states. After data is sent, the FSM waits for the FFT completion by checking the value of `Source_controls` signals that are passed to the `MRP Calculator` as well. Finally, the FSM wait for `500Hz CLK` to return to zero and, next, waits for the `Trigger` to go to `'0'`. After that, the FSM waits for another `Trigger` rising edge to repeat the sequencing.

The FFT output data is interpreted by the `MRP Calculator`, which works with the `clk_fft` clock and enabled by a validation signal among the `Source_controls`. Prior to the `MRP Calculator`, data are squared and opportunely summed (both `real` and `imaginary` parts) using a 64bit adder in order to extract the BP, μ and β powers, in natural units (`BP`, `MU`, `BETA` signals). Finally, when `MRP Ready` is asserted, BP, μ and β are compared to fixed thresholds related to the subject, preloaded on the FPGA at top-level.

IV. Test and Validation

A. Bio-signal Dataset and Measurement Set-up

Data from 7 EEG motor-cortex channels (T_3, T_4, C_3, C_4, C_Z, P_3, P_4) and from an occipital one (O2) are recorded (±375mV analog input range, 24bit resolution, 500Hz sampling rate) and filtered using an 8th order band-pass Butterworth filter (0.5–30Hz). 8 EMG channels (Gastrocnemius, Tibialis, Rectus and Biceps Femoralis of both the legs) are synchronously recorded (16bit resolution at 2 kHz), filtered with an 8th order band-pass (10–200Hz) and down sampled to 500Hz to match the EEG sampling frequency. To achieve the bio-signal synchrony, the EMG synchronization signal generated by the collecting unit is inserted as input into the EEG gateway, which interprets its rising edge as the zero-time for recording. Both EEG and EMG monitoring systems are wireless and wearable. The dataset comprises experimental measurements on 10 healthy subjects (aged between 23 and 29), performing different tasks, i.e., resting sitting, resting standing, walking naturally, walking with obstacles and performing a second cognitive task.

A Matlab implementation of the algorithm has been used as golden reference to test the system. Identical input data have been processed offline by Matlab and the FPGA. To load data on the FPGA and to save outputs to be compared with the golden reference, further storing electronics have been necessary for testing. The application involves a huge quantity of data per second, approximately 160kbps [for EMG signals: 500S/(s·ch) · 16bit/S · 8ch = 64kbps, for EEG signals: 500S/(s·ch) · 24bit/S · 8ch = 96kbps]. For this reason 16 additional RAM storage blocks with approximately 65k rows and words of 16 (for EMG) and 24bit (for EEG) have been included in the FPGA. Each storage RAM contains a single channel where each word memorizes a complete sample. This way, it was possible to load on the FPGA recording segments of about 32 seconds at once, represented in two's complement (`.mif` format, converted with Matlab). The arrival of new samples has been emulated using the `500Hz CLK` signal (obtained by dividing the 50MHz frequency with the PLL and a 14bit counter) which enables 1 word RAMs reading, addressed by dedicated counters. Other data storage RAMs have been used to save the output data for the off-line comparison with Matlab. As outputs are in two's complement an additional back-conversion is necessary for the comparison.

B. Experimental Results

Since the validity of the algorithm implemented on Matlab has been already demonstrated in previous works [5-8], in this section we focus on FPGA performances evaluation. Fig. 4 shows the residual error of the EMG trigger generation (Right Gastrocnemius, natural gait). After transient of 2.34s, the Matlab and the FPGA output are coincident. Since the co-contraction indexes are calculated just by an AND logic between two coupled EMG triggers, the co-contraction error coincides with the EMG trigger error (Fig. 4). Fig. 5 overlaps BP (5.a), μ (5.b), β (5.c) computed by Matlab (blue graph) on the FPGA measurements (red markers) run on C_3 during a natural gait and triggered by the right Gastrocnemius. The BP calculated by the FPGA (Fig. 5.a) presents a mean relative error of 0.01% (mean BP 71.33 dB, mean absolute error 0.0074dB, variance 0.0064). The μ computation through FPGA (Fig. 5.b) returns a 0.012% relative error (mean μ: 60.73 dB, absolute error: 0.0073dB, variance: 0.0056). Finally, the β calculation (Fig. 5.c) outlines a relative error of 0.010% (mean β 61.99dB, absolute error 0.0062dB, variance 0.0075). This slight numerical error is imputable to the double conversion of the FPGA data, which, at first are converted from decimal to two's complement and then are converted back. Since Matlab was running on a 64bit desktop PC, the software calculation achieves a higher accuracy because running on floating point numbers.

For the EMG processing branch, from the `500Hz CLK` rising edge, seven 8MHz clock pulses are needed to complete the operations that are equivalent to slightly less than 10μs. The resources used for a single channel are 306 logic elements out of 32070 available and 20480/4065280 memory elements RAM and registers 188/64140 (including testing storage). Once an `trigger` rising edge is detected, approximately 1536 system clock pulses are necessary: 512cycles@8MHz are needed to load the 256 EEG samples stored in RAM into the FFT block, 256cycles@4MHz are necessary to compute the FFT (estimated by Quartus II), 256cycles@4MHz are needed for data to be available as outputs, thus the operation are completed in 0.13ms. The minimum delay between two different trigger rising edges is 2ms, hence, the computation time of this branch is consistent with the application requirements. Furthermore the use of RAMs to store the 500ms EEG signal allows the repetition of the FFT analysis because RAM data is not erased when read (it would be not possible using, for instance, a FIFO which will be flushed after a first FFT analysis and further 500ms would be necessary for a second one). Observe that it is not needed to wait all the FFT outputs since we are interested only on the first 16 coefficients. The EEG branch latency is actually lower. The EEG branch utilizes 4100/32070 logic elements, 6994/64140 registers and 36632/4065280 memory elements RAM (including testing storage). The overall system implementation with 16 bio-signals inputs and 28 outputs requires 81.7% ALMs, 44808 ALUTs, 73.4% registers, 10.3% block memory of the available resources. Tab. I summarizes the available resources used for the hardware implementation and testing. The system requires a huge amount of block RAM for a single channel testing (45.5%) just for loading 30s of data.

The designed system matches application-level requirements. The wireless recording system introduces a non-negligible latency for data digitalization (which is multiplexed) and transmission, amounting respectively to 1ms and 14ms. Due to the nature of the algorithm [6-8], the EMG trigger rises about 40ms later than the actual contraction. A single EMG trigger sample is computed in 10μs while the time-frequency analysis (when enabled) is run in 0.13ms: the FPGA processing is completed in less than 1ms. The overall processing chain, from data collection to FPGA output generation, takes about 56ms, largely meeting the time limit of 300ms. The system is inherently conceived for energy efficiency, compatibly with application requirements. The most power hungry FFT part is event-driven and triggered only when the EMG signal power

exceeds the threshold, a low probability event (statistically occurring at a rate of 1Hz during normal gait) compared to the EMG/EEG data triggers which are constantly generated at a fixed rate of 500Hz. Moreover, the moving average operations for the calculation of the thresholds are computed using a circular buffer plus an accumulator, which require only a single read and write operation on the respective block RAM at the arrival of a new sample every 2ms, which minimizes arithmetic operations and memory access. In a 180nm CMOS ASIC, a 16bit butterfly 256 points FFT at 4MHz would consume about 13mW during continuous operation including block RAM, which at 4MHz would consume approximately 1mW [13]. Overall, the fall prediction system power consumption (with the given resources in Fig. 3) when unrealistically all blocks are simultaneously operating (worst case) can be estimated as 150mW, which is a feasible upper bound for portable applications.

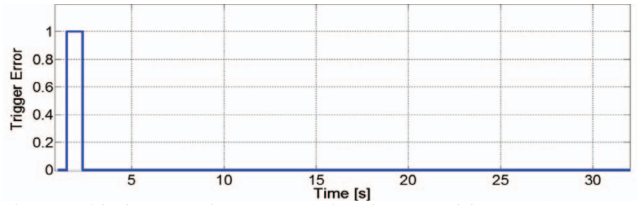

Fig. 4. Residual error on the Gastrocnemius trigger: Matlab vs. FPGA.

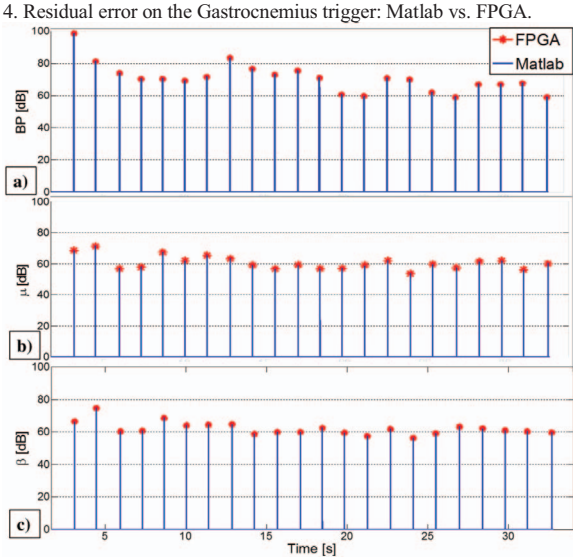

Fig. 5. Matlab (blue) vs. FPGA (red markers) outputs of BP (6.a), μ (6.b) and β (6.c). FPGA implementation returns a numerical error of about 0.01%.

TABLE I. FPGA RESOURCE UTILIZATION

SUB-SYSTEM	ALMs[2] (TOT: 32070)	ALUTs[3]	REGISTERS (TOT: 64140)	BLOCK MEMORY (BITS) (TOT : 4065280)
EMG Branch[1]				
Global aver. FSM	*55.3 (0.2%)*	*108*	*75 (0.1%)*	*0 (0.0%)*
Local aver.FSM	*52.9 (0.2%)*	*108*	*82 (0.1%)*	*0 (0.0%)*
Other	*158.5 (0.4%)*	*274*	*31 (0.0%)*	*20480 (0.5%)*
Total	**268.8 (0.8%)**	**492**	**188 (0.3%)**	**20480 (0.5%)**
EEG Branch[1]				
FFT controller	*103.8 (0.3%)*	*218*	*28 (0.0%)*	*0 (0.0%)*
EEG Block RAM	*42.5 (0.1%)*	*44*	*53 (0.1%)*	*6144 (0.15%)*
FFT processor	*2117 (6.6%)*	*3089*	*6695(10.4%)*	*30488 (0.7%)*
MRP Calculator	*256.6 (0.8%)*	*506*	*218 (0.3%)*	*0 (0.0%)*
Others	*1580.8(4.9%)*	*3191*	*0 (0.0%)*	*0 (0.0%)*
Total	**4100.8 (12.8%)**	**7048**	**6994 (10.9%)**	**36632 (0.9%)**
Testing stimulation logic	781.9 (2.4%)	1132	948 (1.5%)	1830912 (45.0%)
Single channel [4] (including testing storage)	5151.5 (16.1%)	8672	8130 (12.7%)	1888024 (46.4%)
Complete System (processing only)[5]				
7 EEG Branches	*23996 (74.8%)*	*40286*	*45227 (70.5%)*	*255164 (6.3%)*
8 EMG Branches	*1836.2(5.7)*	*3880*	*1432 (2.2%)*	*163840 (4.0%)*
Others	*360.9 (1.1%)*	*642*	*417(0.7%)*	*0 (0.0%)*
Total	**26193.1 (81.7%)**	**44808**	**47076 (73.4%)**	**419004 (10.3%)**

[1] Simulation on a single complete channel; [2] Adaptive Logic Modules; [3] Adaptive Look-Up Tables; [4] 1 EMG and 1 EEG coupled blocks; [5] 8 EMG and 7 EEG blocks.

V. CONCLUSION

We presented an FPGA (Altera Cyclone V) implementation, testing and validation of a fall prediction architecture operating during gait, based on combined EEG/EMG processing [5-8]. EMG signals are exploited to verify muscle contraction, evaluating the agonist-antagonist co-contraction and enable the time-frequency analysis on EEG data in order to detect MRPs occurred before the movement. The comparison between simulated and measured outputs outline a very low residual numerical error of about 0.012% (worst-case) due to the test set-up, demonstrating that an ASIC implementation of the algorithm is feasible. This FPGA prototype acknowledges an ASIC design but even at this development stage, it represents a breakthrough in the field of fall prevention during gait in ambient assisted living applications.

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