Testable Design of Repeaterless Low Swing On-Chip Interconnect

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***Abstract*—Repeaterless low swing interconnects use mixed signal circuits to achieve high performance at low power. When these interconnects are used in large scale and high volume digital systems their testability becomes very important. This paper discusses the testability of low swing repeaterless on-chip interconnects with equalization and clock synchronization. A capacitively coupled transmitter with a weak driver is used as the transmitter. The receiver samples the low swing input data at the center of the data eye and converts it to rail to rail levels and also synchronizes the data to the receiver's clock domain. The system is a mixed signal circuit and the digital components are all scan testable. For the analog section, just a DC test has a fault coverage of 50% of the structural faults. Simple techniques allow integration of the analog components into the digital scan chain increasing the coverage to 74%. Finally, a BIST with low overhead enhances the coverage to 95% of the structural faults. The design and simulations have been done in UMC 130 nm CMOS technology.**

***Index Terms*—Scan test, DFT, BIST, Repeaterless interconnect, Mesochronous synchronizers.**

I. INTRODUCTION

Low swing repeaterless interconnects have been researched extensively for improving the performance of long interconnects, while keeping the power consumption to acceptable levels [1]–[3]. These techniques use low swing on the line with equalization to enhance the bandwidth. A clock synchronizer is needed at the receiver to sample the data correctly, as the interconnect can have a multi-cycle latency. [3], [4]. Such repeaterless interconnect architectures need to use sophisticated mixed signal circuits for achieving high performance and robustness. However in order for these new interconnect architectures to be viable for large scale and high volume digital systems, they must be testable along with the rest of the digital circuits with an acceptable fault coverage. While the digital components of these circuits are typically simple and can be tested using fairly standardized test methods, testing the analog components along with the digital circuits is a challenging problem.

Testing of mixed signal circuits is generally tailored for specific applications and has been reported earlier for PLL's [5], [6]. This paper discusses the testability of repeaterless low swing interconnects that use mixed signal circuits for achieving best performance. The transmitter uses the capacitively coupled feed-forward equalizer reported in [7]. A receiver that employs coarse digital correction and fine analog correction for accurate adaptive synchronization reported in [4] is used. While this paper discusses testing of low swing interconnect using the above circuits as transmitters and receivers, the solutions presented can be used for other low swing interconnect systems as well. For the digital components a 100% coverage is possible with a scan test. For the analog sections, just a DC test of the full link can detect 50.4% of the structural faults. Simple techniques are used to integrate the analog components into the digital scan chain which enhances the fault coverage to 74.3%. The fault coverage is further increased to 94.8% by using a BIST with a lock detector. The circuits do not alter the critical path of the design.

A. Notations and Fault models

The additional circuitry added only for the purpose of testing are shaded grey in all the figures. These circuits will be turned off in normal operation. The structural fault model [6] is used for the analog circuits.

II. DESIGN OF THE TESTABLE INTERCONNECT

Fig. 1(a) shows the block diagram of the repeaterless interconnect. The transmitter is the capacitively coupled transmitter from [7]. The receiver is a clock recovery circuit that is used to generate a sampling clock that samples the data at the center of the data eye [4]. The circuit has two control loops for coarse and fine phase correction. The coarse phase correction loop performs correction in discrete steps quantized to the DLL phases. The fine correction loop performs continuous correction using a voltage controlled delay line. The circuit uses a phase detector to sense the phase difference between the received data and the sampling clock. The error signal from the phase detector is integrated and the integrated output (V_c) controls a VCDL which delays the sampling clock. The negative feedback loop thus formed, pushes the sampling clock to the center of the eye. The VCDL is designed to have a range greater than one phase step of the DLL over a range of control voltage corresponding to the window comparator thresholds. If the fine control loop fails to lock while the control voltage V_c is within the window thresholds, a coarse phase correction request is issued by the window comparator and the control voltage is reset to lie within the window by the strong charge pump. This process repeats till lock is achieved. In steady state, the DLL phase chosen is within the VCDL range from the center of the data eye. Fig. 1(b) shows the waveform of the control voltage and the chosen phase of the DLL with time, as the circuit locks to the correct phase from startup. Once lock is achieved, the phase difference between the sampling

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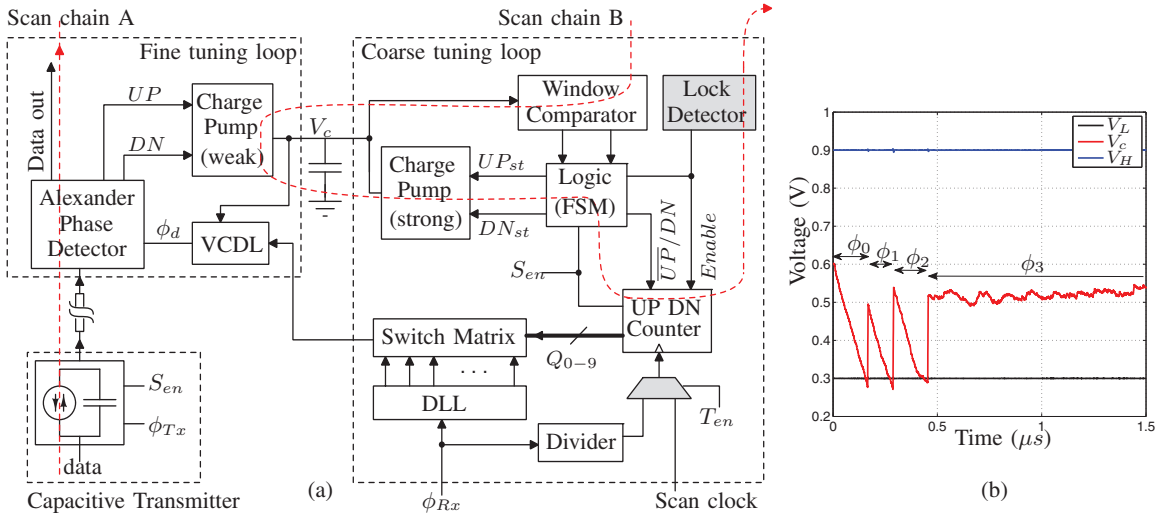

Fig. 1: (a) Block diagram of the interconnect. Receiver is divided into fine tuning and coarse tuning loops. VCDL: voltage controlled delay line, Vc: control voltage, S_{en}: Scan enable, ϕ_{Tx}: Transmitter clock phase, ϕ_{Rx}: Receiver clock phase, ϕ_d: sampling clock phase, T_{en}: Test enable. (b) Control voltage trajectory from startup to lock condition.

clock and the receiver clock can be found from the coarse tuning control word to an accuracy within the VCDL phase tuning range. If the sampling clock is less than half cycle from the receiver's clock, the data is delayed by half a clock cycle to ensure reliable crossover to the receiver clock domain. The simulated circuit was designed in UMC 130 nm CMOS technology with a supply voltage of 1.2 V and a data rate of 2.5 Gbps.

Since the receiver and the transmitter operate in different clock domains, the circuit is tested using two separate scan chains, which are the data path scan chain (Scan chain A) and the clock control path scan chain (Scan chain B). When test is enabled, the coarse correction loop's clock input is driven from an external scan clock as shown in Fig. 1. The divider in this circuit can be shared across multiple such receivers in the chip and tested separately.

A. The data path scan chain

The low swing transmitter (Fig. 2) is the first component of the data path scan chain. It uses series capacitors for equalization and the weak driver in shunt with the capacitors enables arbitrarily low data activity factors [7] (Single ended version is shown for brevity). Flip-flops are added to probe the driver side of the series capacitors (the shaded flip-flops in Fig. 2) which enable the scan chain to cover all the nodes up to the series capacitors. The additional latch in the data path is inserted to optionally introduce a half cycle delay at the transmitter, which is required for testing the phase detector at the receiver. This latch is transparent during normal operation and it can be absorbed into the buffer that drives the line. Since the interconnect has high latency, it is not in the critical path. Hence the delay added by the latch does not degrade the maximum operating frequency of the system.

Fig. 3 shows the circuit diagram of the receiver termination with the test circuit. It uses comparators with programmed offset of 15 mV for the DC test. This circuit is a single stage opamp followed by an inverter. The interconnect is designed for a logic swing of 60 mV and when the circuit has no faults the comparator gets an input of 30 mV. The window comparator compares the bias generated at the receiver with another voltage divider bias generator in the clock recovery circuit. The window comparator is constructed using two comparators with a programmed offset of +15 mV and -15 mV. Any fault in the weak driver or the series capacitors at the transmitter or the termination resistor at the receiver, results in a mismatch in the two arms of the differential interconnect. All such faults are detected by the comparators. Some faults, like drain open in one of the transistors of the transmission gate resistor, result in a dynamic mismatch, which is not detectable at DC. Hence the window comparator is designed to operate at the scan frequency (which is assumed to be 100 MHz) and these faults are detected with a simple toggling data pattern

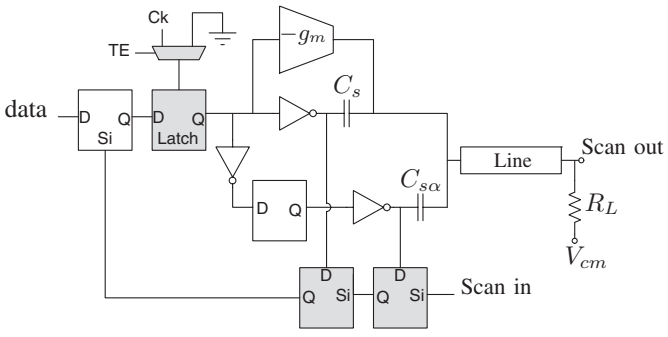

Fig. 2: The capacitive feed-forward equalizer with the weak driver. All the flip flops are clocked by the same transmitter clock, which is not shown.

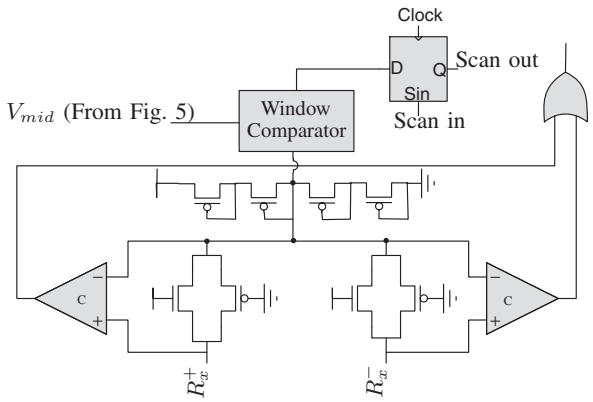

Fig. 3: The termination of the interconnect at the receiver.

during scan. Common centroid layout techniques can be used to reduce the inherent offset in these comparators. Since these comparators are either used at DC or at scan frequencies, the additional parasitics are not a problem.

The last component in the data path scan chain is the Alexander phase detector at the receiver. The circuit diagram of the phase detector is shown in Fig. 4. When the link is operated at the scan frequency, the phase detector always asserts the UP signal. To test the other signal path, the half cycle delay at the transmitter side is enabled, which makes the phase detector assert the DN signal. Thus, with two passes both these paths can be tested. The last flip-flop (which is driven by either ϕ_{Rx} or $\overline{\phi_{Rx}}$) in the data path is used to insert either a 1 clock or a half clock cycle delay. This is required for transferring the data to the receiver clock domain. Half cycle delay is chosen when the sampling clock is less than half a clock cycle away from the receiver clock and this is done by driving this last flip-flop with $\overline{\phi_{Rx}}$. For test purposes this can be controlled via the clock control path scan chain. When ϕ_{Rx} is chosen, it results in an increase in the length of Scan chain A register by 1 flip-flop.

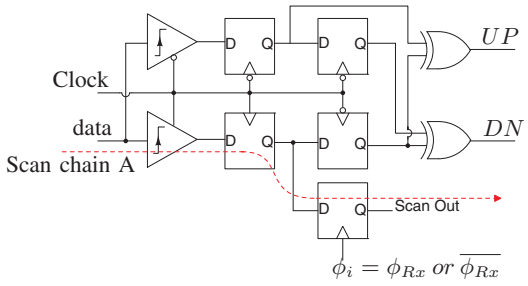

Fig. 4: The Alexander phase detector with scan.

B. Clock control path scan chain

The first circuit block in this scan chain comprises of the window comparator, the charge pumps and the control FSM. Fig. 5 shows the circuit diagram of this part of the system. The charge pump is an analog circuit and cannot be included in the scan chain as is. To work around this, the charge pump is converted to a combinational circuit when scan test is enabled by connecting the bias voltages for the current sources in the charge pump to GND for the PMOS source and to VDD for the NMOS sink. This essentially converts the analog charge pump into a combinational circuit with two inputs UP and DN and one output. Also when scan is enabled, the window comparator's input is connected to the middle of the thresholds thus forcing its output to be "00". Two flip-flops are used to capture the comparator's outputs, which are read through the clock control path scan chain. Scan chain A is used to make the phase detector assert either UP or DN signal. This results in the control voltage V_c being driven to a logic '1' or "0' respectively. When the scan is disabled and the circuit is clocked before re-enabling scan mode, the control FSM resets the control voltage to within the window. Most of the faults in the charge pump result in the control voltage not being reset to within the window or in not being driven to the desired logic level when scan is enabled. The comparators outputs can detect most faults in the charge pump circuit.

To test the ring counter, it's contents are accessed using scan chain B and its control inputs ($UP/\overline{DN}$ and $Enable$) are setup using scan chain A. The last circuit block in the clock control path scan chain is the switch matrix. Defects in this block may lead to inability of selecting a desired phase for locking or inability to deselect a particular phase. This is tested by pre-loading the ring counter with all zeroes pattern. This causes none of the phases to be picked, resulting in Scan chain A not getting clocked. Simple continuity test of Scan Chain A can detect a permanently selected phase. Further pre-loading different one hot values into the ring counter and testing the continuity of Scan Chain A all the paths in the switch matrix can be tested.

C. BIST

The Lock Detector in Fig. 1 is a simple saturating UP counter. It logs the number of times a coarse correction request has been issued. From any initial condition, the number of coarse corrections needed can be no more than half the number of DLL phases. The design used a 10 phase DLL and hence a 3 bit saturating UP counter is sufficient. For BIST, the interconnect is run with random data at speed. The receiver is expected to lock within 2 μs, which corresponds to 5000 cycles at 2.5 Gbps. Some of the faults in the charge pump, which are not detectable in the scan test, can be detected using this test. During scan test the charge pump's current sources were used as switches, which however mask drain source short faults in them. The BIST with the lock detector can detect such faults. The scan test of the charge pump tested only the main charge pump path and the charge balancing path (that drives the node V_p in Fig. 5) is not tested. Any faults in this second path or faults in the amplifier in the charge pump, result in the node V_p drifting towards V_{DD} or GND. This pushes one of the current sources to linear region and as a result causes increased jitter in the recovered clock, which can degrade the interconnect performance. The CP-BIST block in Fig. 5 is a window comparator that is designed for a window of 150

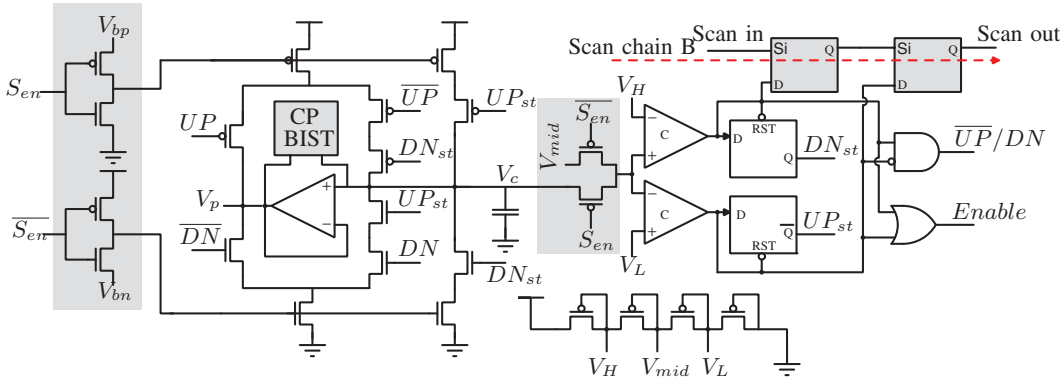

Fig. 5: Control logic for generating $\overline{UP}/DN$ and $Enable$ signals for the ring counter and UP_{st} & DN_{st} signals for the strong charge pump. V_H, V_L are the upper and lower thresholds of window comparator respectively. All flip-flops are clocked with the divided clock of the coarse control loop.

mV. Once lock is achieved, this comparator output being high indicates a fault in the charge pump that was not detected in the scan test.

The DLL in the receiver is not tested completely by this BIST. This DLL can be treated as a stand-alone unit and using the techniques reported in [8], a complete test of the DLL can be integrated with the interconnect test.

III. Simulation Results

The interconnect system was designed in UMC 130 nm CMOS technology. The digital components are tested using the scan test. Since the circuits are logically simple in nature, the stuck at fault coverage is 100%. The digital coarse correction is operated at a divided clock frequency which is in the range of scan test frequencies. Hence the delay faults in this path are also tested with 100% coverage. For the analog components, two DC tests with the interconnect input at logic 1 and logic 0 respectively can detect 50.4% of the structural faults in the circuit. Scan test of the analog circuits in the receiver by converting the charge pump to a combinational circuit enhances the coverage to 74.3%. Finally the BIST increases the fault coverage to 94.8%. Table I shows the fault coverage statistics and the incurred circuit overhead of the design.

Note : An extended version of this paper with detailed circuit diagrams can be found in an arXiv eprint [9].

TABLE I: Fault coverage statistics and circuit overhead

(a) Fault Coverage

Defect	Coverage
Gate open	87.8%
Drain open	93.9%
Source open	93.9%
Gate drain short	93.9%
Gate source short	100%
Drain source short	100%
Capacitor short	100%
Total	94.8%

(b) Overhead

Entity	No.
Flip-flop	7
Comparators (DC)	4
Comparators (100 MHz)	2
D-Latch	1
2×1 Multiplexer	2
3 bit saturating UP counter	1
Control signals	2
Logic gates	6

IV. Conclusions

This paper describes the test of repeaterless low swing interconnects which use mixed signal circuits for equalization and clock synchronization. The digital circuits are scan testable easily. Simple techniques are used to test the analog components along with the digital circuits for the scan test. A cumulative fault coverage of 95% is achieved with a DC test, a scan test and a BIST. This enables the use of low swing interconnect in large scale high volume digital systems.

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