All-digital Hybrid-control Buck Converter for Integrated Voltage Regulator Applications

Ta-Tung Yen, Bin Yu, Visvesh S. Sathe
Department of Electrical Engineering
University of Washington, Seattle
sathe@uw.edu

***Abstract*—As power-dissipation remains a roadblock to maintaining growth in computational performance, the trend toward increasingly aggressive reliance on Dynamic Voltage and Frequency Scaling (DVFS) by power power management systems, and Integrated Voltage Regulation (IVR) in particular, will continue. As voltage domains continue to shrink, and an increasing number of Voltage Regulators (VRs) are employed within a System-on-Chip (SoC), all-digital buck converters will become increasingly important from a scalability, portability, and system-methodology perspective. In addition to the existing challenges facing VR Modules, IVRs face additional efficiency and transient response challenges. In this paper, we propose a voltage-reference-free all-digital hybrid-control buck converter addressing these challenges through novel techniques for accurate digital derivative measurement for PID control, and fast, all-digital non-linear control for minimizing voltage droop. Simulations in 65nm CMOS demonstrate an 86% efficient, stable operation with fast transient response. A single-phase implementation using package mounted inductor and filter capacitor models achieves a 25mV droop for a 5A load current ramp at 500mA/ns.**

I. Introduction

Energy-efficiency continues to limit continued performance growth in modern computing systems. Although designers aggressively employ a variety of techniques to yield efficiency improvements, DVFS remains the most effective method to be employed thus far, and trends indicate continued aggressive DVFS use in the increasingly heterogeneous and multi-core systems of the future. Much work has been done on IVR systems [1]–[4]. Multiple power domains with faster transient response provide enhanced spatial and temporal control of individual voltage domains, enabling greatly enhanced DVFS implementations. As future microprocessors are posed to have hundreds of voltage domains [5], made possible only by integrated regulation, current IVR designs face several challenges including (1) the increasing difficulty and scalability of traditional analog IVR implementations (2) Degraded compatibility of IVR designs within, and portability across largely digital modules within the SoC, and (3) the need for fast-response IVR implementations due to the reduced available decoupling capacitance (decap) per voltage domain.

A basic digital buck converter architecture is outlined in Figure I. The sensed supply voltage is compared to a reference V_{ref}. The resulting error is converted into a digital code, and processed by a digital compensator (often a PID, or lead/lag implementation), whose output drives a Digital Pulse Width Modulator (DPWM) module which drives the bridge with the appropriate duty-cycle to maintain regulation.

Digital buck converter implementations are an attractive, scalable solution, offering (1) Improved portability across designs. (2) Improved scalability across technology generations in contrast with prevalent analog IVR design techniques. (3) Fully synthesizeable control implementations, readily compatible with modern SoC design flows. (4) Reduced susceptibility to process variation, requiring less post-fabrication trimming and calibration, reducing complexity and test-time. Consequently, digital IVR implementations are expected to play an important role the number of on-chip voltage domains continues to grow.

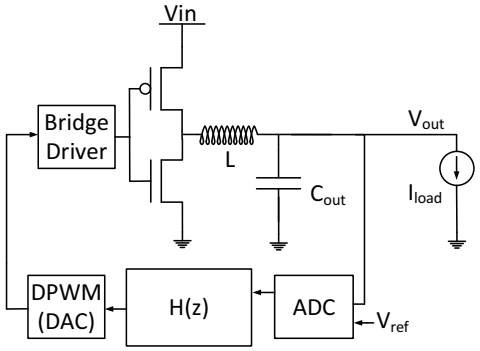


Fig. 1. Conventional ADC-based Digital Buck Converter

Several key challenges face state-of-the-art digital IVR control implementations. Reduced available per-domain filter capacitance requires even faster transient load response. Modern Advanced Configuration and Power Interface (ACPI) systems requiring a supply-voltage resolution of 6.25mV, or equivalently 8-bits of ADC resolution. Suppressing quantization error for stable control requires even higher resolution in the ADC, and consequently in the DPWMs [6], increasing power and complexity. Ripple-based techniques including time-optimal [7] and hysteresis-based architectures [8] have been proposed in the literature. Although well-suited to IVR applications due to their superior transient response, hysteretic control has not been widely adopted due the need for careful design to avoid noise and instability challenges [9]. Furthermore, these designs have not been demonstrated using all-digital circuits.

In this paper, we propose an all-digital hybrid-control voltage regulator suitable for IVR applications. The contributions of this work are as follows. (1) We propose an all-digital, voltage-reference free IVR design that effectively tracks the critical path of DVFS-enabled digital systems across its operating supply voltage range, avoiding margins due to temperature variation and regulator offsets. (2) A novel time-based discrete difference technique that efficiently enables the accurate measurement of the output voltage derivative used in PID control is proposed. (3) We propose the first all-digital hybrid-control implementation for IVRs driving digital systems.

Simulations in an industrial 65nm process technology demon-

978-3-9815370-6-2/DATE16/©2016 EDAA

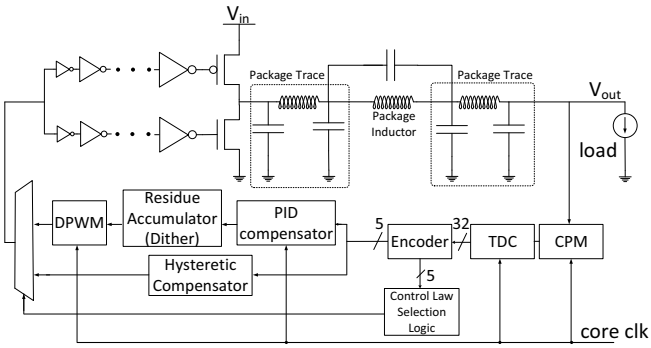


Fig. 2. Proposed hybrid-control all-digital buck converter architecture using package-mounted inductors for use in IVR applications. Package and on-chip decap are available. The architecture operates in one of two modes: linear-feedback or direct-drive for stable operation with fast transient response

strate stable, efficient operation with fast load regulation. Operating with a single phase, using package mounted inductor and filter capacitor models, the converter achieves 25mV droop for a 5A load current ramp at 500mA/ns. With an input supply voltage of 2V, the converter achieves a peak efficiency of 86% at 2A.

II. System Architecture

Figure 2 shows a block-diagram of the proposed hybrid-control all-digital buck converter architecture. The proposed architecture relies on linear-feedback (PID) control for steady-state operation, transitioning to a fast-response direct-drive mode, where the bridge is continuously driven to either V_{in} (V_{ss}) to respond to sharp transients. The proposed architecture offers the stability and multi-phase compatibility of linear-feedback control with the fast response of direct-drive mode. Though amenable to a multi-phase implementation, the current work describes a single-phase system in the interests of brevity.

The Critical-Path Monitor (CPM) module monitors the critical path of the system across its operating supply voltage. The measured timing slack is digitally encoded by a sub-gate delay resolution TDC for use in both PID and direct-drive control. The PID controller consists of a traditional PI module applied, along with the proposed derivative calculation module for reduced quantization noise and improved PID stability. The PID output is then provided to the DPWM through a digital $\Delta\Sigma$ modulator to enable high-frequency DPWM code dither for improved resolution. The DPWM consists of a saturating counter that implements a ramp function to compare the output of the residue accumulator. Control logic selects between the choice of the PID controller output or the direct-drive output, which subsequently drives the bridge.

Limit-cycling considerations constrain the voltage resolution of the CPM-TDC to be at least one bit less than that of the DPWM [6], motivating a coarser CPM-TDC. In contrast, a finer CPM-TDC voltage resolution is desirable for finer V_{out} control, enabling improved energy efficiency and reduced quantization noise accompanying the error signal for improved stability. The competing objectives of finer CPM-TDC resolution and limit-cycle avoidance are managed by maintaining a relatively coarse resolution for steady state operation (conditions under which the relative resolution relationship applies). High-resolution TDC data is used to support fast, stable transient response through accurate difference measurement (in the D module of the PID controller), and direct-drive control. Simultaneously, the effective resolution of the DPWM is enhanced by clocking the ramp-generation counter on both edges of the core clock for finer duty-cycle control, and by implementing a residue-accumulation-based dithering mechanism. More details on both, the TDC resolution management, and the DPWM design are provided in Section IV.

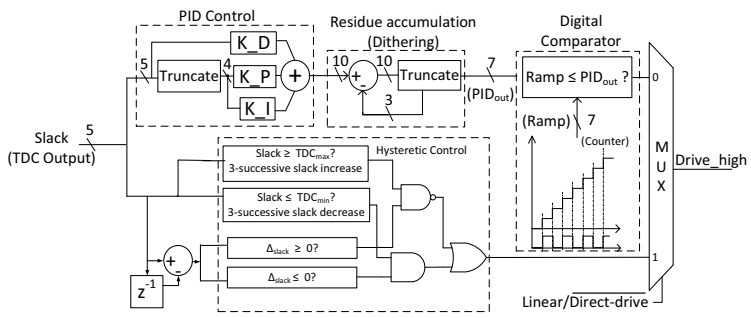
III. Hybrid-Controller

Figure 3 outlines the operation of the hybrid controller. Under steady-state operation, the controller operates in linear feedback mode, with a PID compensator providing load regulation. When V_{out} is lower (higher) than V_{min} (V_{max}), *and* the inductor current is lower (higher) than the load current, the controller transitions to direct-drive for fast transient response. Once the converter has rapidly met the load current deficit (excess) under direct-drive operation, the PID module re-assumes control of the loop. Note that during this current-driven control-law transition, the output voltage is nearly at its maximum or minimum. Clocked comparators make decisions based on both the current, and previous TDC code. Tracking Δ_{slack} estimates inductor current magnitude relative to the load current, allowing for a smooth transition back from direct-drive to linear control. The TDC provides two different levels of resolution. A high-resolution (6mV at 1.2V V_{out}) codes is used to minimize quantization error for direct-drive control, and for signal-derivative calculation in the D branch of the PID control. A lower resolution (truncated) code (relative to the DPWM) is used for PI control to prevent limit-cycling.

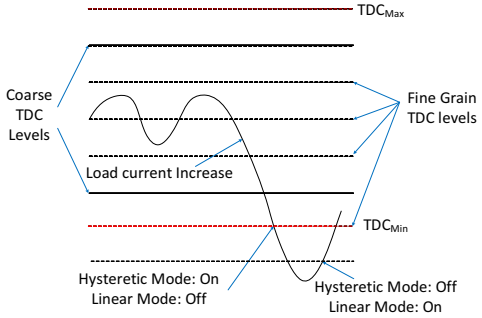
Figure 3b illustrates the time-domain operation of the hybrid-control converter. Under steady-state, the converter operates with linear-feedback. An increase in load current causes V_{out} to decline. As the corresponding slack drops below TDC_{min}, the system transitions to direct-drive, enabling the highest possible current flow into the inductor to meet the demand current. Once the inductor current exceeds the load current, V_{out} begins to increase. The hybrid-controller tracks Δ_{slack} using the high resolution TDC to detect this supply voltage upswing to transition into linear mode. Note that the transition into linear-feedback mode is driven by the relative magnitude of the inductor and load currents.

Since output voltages do not transition sufficiently to cause multi-code changes in the TDC within a single switching cycle, the conventional approach of determining code-differences in successive switching cycles yields noisy, inaccurate derivative measurements. Figure 4 shows the proposed approach for improved-accuracy signal-derivative calculation for the D component of the compensator, which instead relies on the number of core clock cycles (operating at a significantly higher multiple of the switching frequency) between TDC code changes, vastly improving measurement accuracy. The division operation shown in Figure 4 is used for illustration. For implementation, a 16-entry look-up table provides sufficient accuracy.

The PID controller output is compared against an internal counter-generated ramp within the DPWM, producing the drive signal with the target duty-cycle. A double-edge triggered counter provides improved resolution. In our implementation, the total ramp count is 127, yielding a 7.8mV resolution for any value of V_{out}. Dithering applied to the DPWM to ensure higher resolution compared to the CPM-TDC (a requirement for



(a) Controller block diagram



(b) Time-domain operation

Fig. 3. Hybrid-controller block diagram and operation

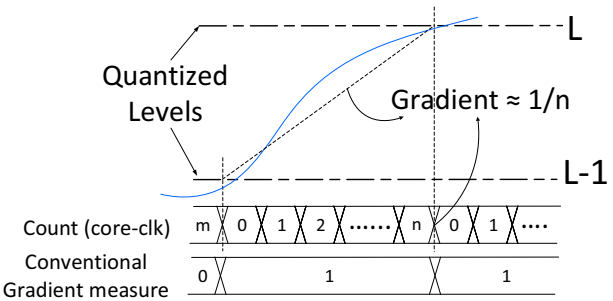
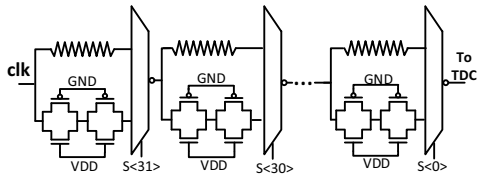


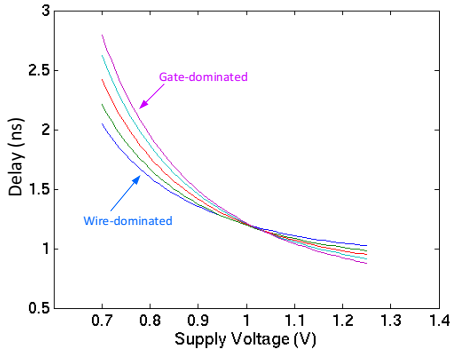
Fig. 4. Calculation of the discrete-time derivative of the error signal

avoiding limit cycles) further improves the effective resolution of the PWM by a factor of 8.

IV. CPM and TDC Design



(a) CPM simplified schematic. Delay elements within the chain are independently programmed to exhibit wire-dominated, or gate-dominated delay



(b) Simulation results of CPM delay over a range of V_{out} values. Selecting a mix of gate and wire-dominated delay cells provides a range of voltage-delay sensitivities

Fig. 5. CPM design

Figure 5 shows a simplified schematic of the CPM design, and simulation results demonstrating its ability to model a range of voltage-delay sensitivities in the system critical path. Canary circuits [10] have previously been used to model a limited set of critical paths decided upon at design-time. Such an approach is suited to a specific system block and is not readily portable to multiple voltage domains. In the proposed approach, two "basis" delay cells are employed – wire-dominated, and gate-dominated, corresponding to the lowest and highest possible delay-voltage sensitivities respectively. A convex combination of these two cells within the CPM chain will span the range of possible delay-voltage sensitivities as seen in Figure 5b, allowing the proposed construction to be portable across multiple designs. The TDC in the proposed architecture employs a vernier delay line [11] to achieve a CPM-TDC voltage (worst-case) resolution of 6mV at 1.2V.

V. Simulation Results

TABLE I
Parameters used for simulation experiments

Parameter	Quantity
V_{in}	2.0V
V_{out}	0.8V – 1.2V
I_{Load} (max)	6A
C_{pkg}, ESR	10μF, 2$m\Omega$ [12]
L, R_L	13nH, 40mΩ [13]
Switching Frequency	15.6MHz
CPM-TDC resolution	6mV
DPWM resolution (w/ dithering)	7 (10)

The hybrid-control architecture was evaluated in an industrial 65nm process technology through simulation analysis of a one-phase implementation assuming the use of package mounted inductors and decoupling capacitors. Circuit/system parameters used in our evaluation are outlined in Table I. package parasitics are included in the analysis. The bridge offers significant switching capacitance due to its size and use of metal and vias to reduce conduction losses. Therefore, wiring parasitics associated with the bridge and the pre-drivers were also included in the simulation. With the exception of the TDC and CPM, the all-digital controller was synthesized and constructed using auto-place-and-route tools prior to netlist extraction. Efficiency estimates of the converter includes the dissipation of all constituent blocks.

Figure 6 shows the simulated efficiency achieved by the proposed all-digital buck converter over a load current range of 1.5A to 4.5A at supply voltages of 0.8V, 1V and 1.2V. The

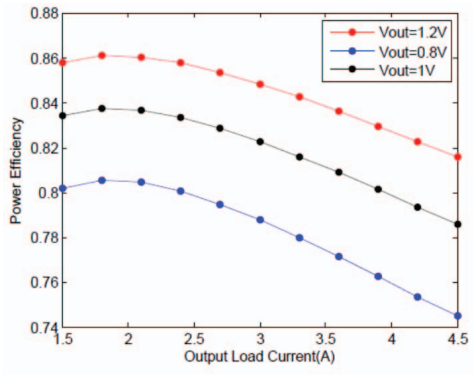
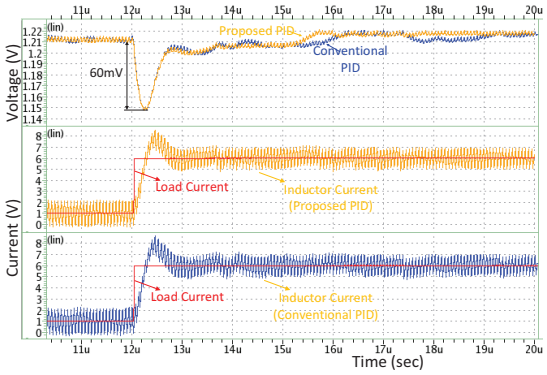
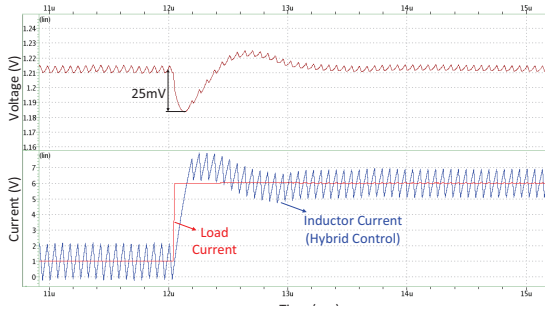


Fig. 6. Simulated efficiency of the hybrid-control converter

converter efficiency is dominated by the I^2R losses in the air-core inductor, a problem effectively addressed by increasing the phase count of the converter (outside the scope of this work). The existing simulation configuration achieves a peak efficiency of 86% at 2A of current load. Implemented with 211 standard-cells, the controller dissipates 5mW, accounting for approximately 0.5% of the power losses in the system at 2A.



(a) Conventional PID controller and proposed PID control with enhanced derivative measurement (direct-drive disabled). Inaccuracy in difference calculation causes a less stable restoration of the supply voltage



(b) Hybrid-control provides a stable response with minimal droop voltage

Fig. 7. Simulated transient response of V_{out} (conventional and proposed) due to a 10ns-5A current load ramp

Figure 7 shows the impact of the proposed architecture on transient step response. To examine effectiveness of the improved derivative calculation in the proposed architecture in linear feedback-mode, we evaluated current step response with direct-drive disabled. Figure 7a illustrates the voltage and current response of the architecture in linear-feedback mode, along with the step response of a conventional PID controller. The peak droop in both implementations is observed to be 60mV. With the hybrid controller enabled, a stable response with a peak droop of 25mV as shown in Figure 7b. As V_{out} transitions to VSS, and the positive slack margin falls below TDC_{min} , the hybrid-controller turns on the bridge to *continuously* increase the inductor current to meet the load current demand, during which time V_{out} continues to fall. When the inductor current exceeds the load current and V_{out} begins to transition upward, the high resolution TDC detects the transition and the control-law selection logic transitions the system into linear feedback mode, allowing for a gradual, near-seamless settling of the voltage. Notably, the proposed digital architecture enables the buck converter to respond with minimal time (accounting for non-zero granularity of digital control) – The actual regulator droop voltages vary based on the choice of inductors and filter capacitance.

VI. Conclusion

In this paper, we present a novel, all-digital hybrid-control buck converter architecture for IVR applications. The proposed architecture operates in linear-feedback mode in steady-state, and relies on a direct-drive approach to provide fast transient response. The proposed control law ensures smooth transition between the two modes. We also propose a novel approach to enabling enhanced voltage-difference measurement to allow for more stable PID response. By operating in linear mode under steady state, the proposed approach also readily translates to multi-phase operation. Simulation experiments indicate a 25mV peak droop at the output voltage of the converter in response to a 5A current ramp at 500mA/ns. The converter achieves a peak efficiency of 86% at 2A.

References

[1] G. W. Den Besten and B. Nauta, "Embedded 5 V-to-3.3 V voltage regulator for supplying digital IC's in 3.3 V CMOS technology," *JSSC*, vol. 33, no. 7, pp. 956–962, 1998.
[2] P. Hazucha, T. Karnik *et al.*, "Area-efficient linear regulator with ultra-fast load regulation," *JSSC*, vol. 40, no. 4, pp. 933–940, 2005.
[3] J. Kwong, Y. K. Ramadass *et al.*, "A 65 nm sub-microcontroller with integrated SRAM and switched capacitor DC-DC converter," *JSSC*, vol. 44, no. 1, pp. 115–126, 2009.
[4] N. Kurd, M. Chowdhury *et al.*, "5.9 Haswell: A family of IA 22nm processors," in *ISSCC, 2014*, Feb. 2014, pp. 112–113.
[5] S. Borkar, "Thousand core chips: A technology perspective," in *Proceedings of the 44th Annual Design Automation Conference*, ser. DAC '07. New York, NY, USA: ACM, 2007, pp. 746–749.
[6] A. Peterchev and S. Sanders, "Quantization resolution and limit cycling in digitally controlled PWM converters," in *PESC 2001.*, vol. 2, 2001, pp. 465–471 vol.2.
[7] A. Costabeber, L. Corradini *et al.*, "Time optimal, parameters-insensitive digital controller for DC-DC buck converters," in *PESC 2008.*, Jun. 2008, pp. 1243–1249.
[8] L. Corradini, E. Orietti *et al.*, "Digital Hysteretic Voltage-Mode Control for DC–DC Converters Based on Asynchronous Sampling," *IEEE Transactions on Power Electronics*, vol. 24, no. 1, pp. 201–211, Jan. 2009.
[9] R. Redl and J. Sun, "Ripple-Based Control of Switching Regulators :An Overview," *IEEE Transactions on Power Electronics*, vol. 24, no. 12, pp. 2669–2680, Dec. 2009.
[10] A. Drake, R. Senger *et al.*, "A Distributed Critical-Path Timing Monitor for a 65nm High-Performance Microprocessor," in *ISSCC 2007.*, Feb. 2007, pp. 398–399.
[11] T. Rahkonen and J. T. Kostamovaara, "The use of stabilized cmos delay lines for the digitization of short time intervals," *Solid-State Circuits, IEEE Journal of*, vol. 28, no. 8, pp. 887–894, Aug 1993.
[12] "Low inductance capacitors," http://www.avx.com/docs/catalogs/lga2t.pdf.
[13] "Low profile mini spring inductors," http://www.mouser.com/ds/2/597/mini_lp-270628.pdf.