Towards Automatic Diagnosis of Minority Carriers Propagation Problems in HV/HT Automotive Smart Power ICs

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***Abstract*— In this paper, a proposed methodology to identify the substrate coupling effects in smart power integrated circuits is presented. This methodology is based on a tool called AUTOMICS to extract substrate parasitic network. This network comprises diodes and resistors that are able to maintain the continuity of minority carrier concentration. The contribution of minority carriers in the substrate noise is significant in high-voltage and high temperature applications. The proposed methodology along with conventional latch-up problem identification for a test case automotive chip AUTOCHIP1 are presented. The time of the proposed methodology is significantly shorter than the conventional one. The proposed methodology could significantly shorten the time-to-market and ameliorate the robustness of the design.**

Keywords*— *smart power integrated circuits; substrate modeling; substrate noise; minority carriers

I. INTRODUCTION

Automotive applications have become a growing market for smart power integrated circuits. Nowadays, the automotive industry aims at developing green cars along with ameliorating network connectivity. Hence, the smart power ICs are becoming increasingly attractive to miniaturize the systems and implement more functions in the vehicles. Consequently, addressing electronics failures has a spate of interest in order to guarantee more robust and reliable products. Currently, the design centers can prove by simulation the functional modes. As a result, the number of the electronic failures are drastically reduced thanks to Design for Reliability (DfR) method [1] [2] globally deployed in automotive besides, the monolithic integration in ICs where reliability is ameliorated by manufacturing.

However, failures due to substrate noise coupling are still reported in tests after fabrication. These failures could be latch-up that can lead to the destruction of the circuit. The designer can extract them manually and consequently, the robustness of the circuit depends on the background of the designer. In [3], the noise in smart power ICs is addressed and a TCAD-guided design methodology for substrate current control is proposed. Addressing more complex structure with this methodology could be impractical as it takes excessively long time. In [4], a modeling methodology for the PN junctions contributing in the substrate noise has been introduced. Additional terminals to the conventional diodes and resistors are used to preserve the minority carrier diffusion. The key advantage of this technique is its compatibility with circuit simulator. Hence, the simulation time is considerably shorter than TCAD simulations. However, the substrate network is extracted manually that is tedious for complex circuit analyses.

The main objective of this paper is to propose an automated approach for modeling the substrate. This approach relies on automatically extracting the substrate parasitic components from the layout. These components are modeled using special types of diodes and resistors that ensure the continuity of the minority carrier propagation [5] [6] [7]. The tool used for the extraction and composing the equivalent substrate network is called AUTOMICS. We illustrate the conventional method for failure detection in the industrial verification flow and how our proposed verification flow could shorten the time-to-market and ameliorate the design.

The paper is organized as follows. In Section II, the AUTOMICS tool flow is illustrated and the calibration of the tool for the parameters of the process technology. The proposed design/verification flow is explained in Section III. Section IV shows a study for an industrial test case chip, finally, the conclusions are drawn in Section V.

II. SUBSTRATE PARASITIC EXTRACTION WITH AUTOMICS TOOL

AUTOMICS tool is capable of modeling the substrate considering the minority and majority carriers propagation. It depends on special types of diodes and resistors presented in [5]. The extraction procedure has two steps:

A. Geometrical features extraction using AUTOMICS tool,

B. Technological parameters calibration.

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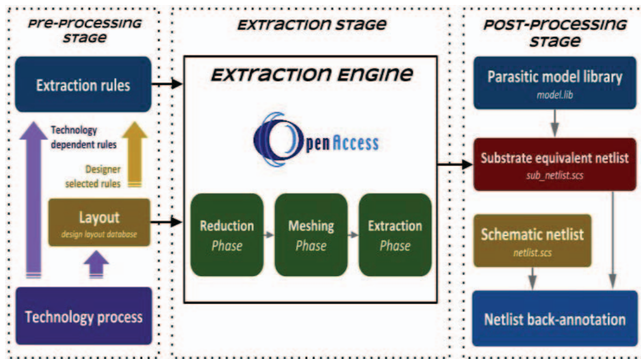

Figure 1 proposed substrate parasitic extraction flow

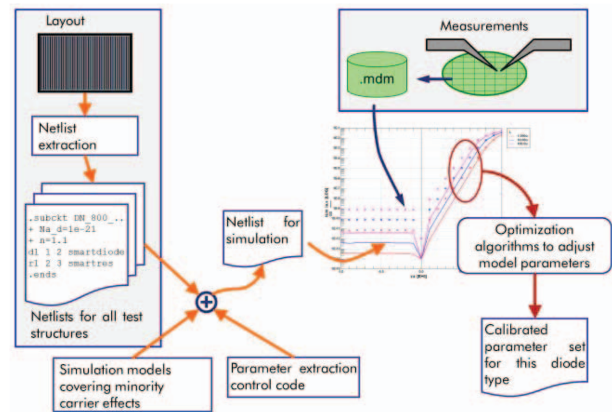

Figure 2 technology parameters extraction flow

A. *AUTOMICS tool geometrical features extraction*

The input to AUTOMICS tool is the layout of the design as shown in Figure 1. As layout designs are in two dimensions (x- and y-axes), the z-axis is technology dependent. For instance, the depth of mask layers, and their doping profiles. Thus, for extraction, this information is given as guide rules for extraction. These *extraction rules* are specified for each process technology. The entire Computer-Aided-Design (CAD) framework is developed using the "OpenAccess" open source API [8].

The processes operated on the layout are reduction, meshing, and extraction. In the *reduction* phase, a reduction mechanism is used to filter out the layers that are not contributing in the substrate parasitic coupling, e.g. metal layers. The *meshing* phase, a 2D meshing strategy is applied to the reduced layout. In conjunction with the extraction rules, a substrate 3D mesh is constructed. A non-uniform meshing mechanism is used to reduce the complexity. The *extraction* phase, parasitic devices are extracted and classified based on the doping profiles and orientation [6]. A netlist describing the extracted parasitic components is generated. In the post-processing stage, the extracted substrate netlist is ready for simulation with or without original schematic netlist. Simulations with the original netlist could be used to visualize the effect of minority carriers propagation in the substrate.

B. *Model parameters calibration*

Model calibration is a necessary step to estimate the doping concentrations and generate a parasitic model library for a certain technology. In general, TCAD simulations can be used in such calibration process. However, this approach needs a detailed input with respect to doping concentrations and doping profiles, which may not be convenient in industrial test cases. Therefore, a special set of test structures was implemented to characterize and model the basic diode behavior as well as the interaction between different well implants due to minority carriers taking into account shape and distance parameters of the well dimensions. The simulations are compared to measured data and an optimization algorithm is applied to tune the available model parameters to the measured curves. The calibration process in principle is shown in Figure 2.

III. PROPOSED SMART POWER ICS DESIGN METHODOLOGY

Certain design failures due to minority carriers coupling are only discovered after fabrication. The conventional design flow is shown in Figure 3, after fabrication an evaluation and validation step is done. Since the automotive applications are safety critical, extensive number of tests are performed on the chip. During these harsh tests, the design may fail. For well-designed circuits, the simulator shows no errors which may not be the real case. Thus, parasitic hand extractions should be done considering the parasitic components that normally are ignored by the current commercial tools e.g. lateral NPN transistors, that is a layout-dependent, can cause a latch-up failure. After identifying the source of failure, the circuit is redesigned and refabricated. In some cases, this loop could be repeated more than one time, prolonging the time-to-market.

Our proposal is to add extra steps to the conventional flow before fabrication. In these steps, the substrate parasitic components are extracted from the layout using AUTOMICS tool. The output of the tool is substrate equivalent network that considers the majority and minority carriers propagation. Then, it can be simulated with the original design to visualize the effects of minority carriers propagation in the substrate. DC analyses can be done to estimate the amount of dc leakage current coupled to different wells on the substrate. This estimation can be used to reduce coupling between different wells by inserting guard rings or increase the distance. In addition to DC analyses, transient simulations could show effects due to junction capacitances of different wells on the same substrate. These capacitances significantly affect the system operation when abrupt voltage changes occur. Such effects could be the main source of latch-up in some circuits as will be discussed in next section.

The proposed methodology has the potential to reduce the number of redesigns. As the designer would be able to check the design robustness against effects that do not appear in the circuit simulations only. Furthermore, he would be able to optimize the isolation techniques e.g. guard rings, hence reducing the silicon area. These two factors can lead to reduce the cost and shorten the time-to-market. The key advantage is the short simulation time along with acceptable accuracy.

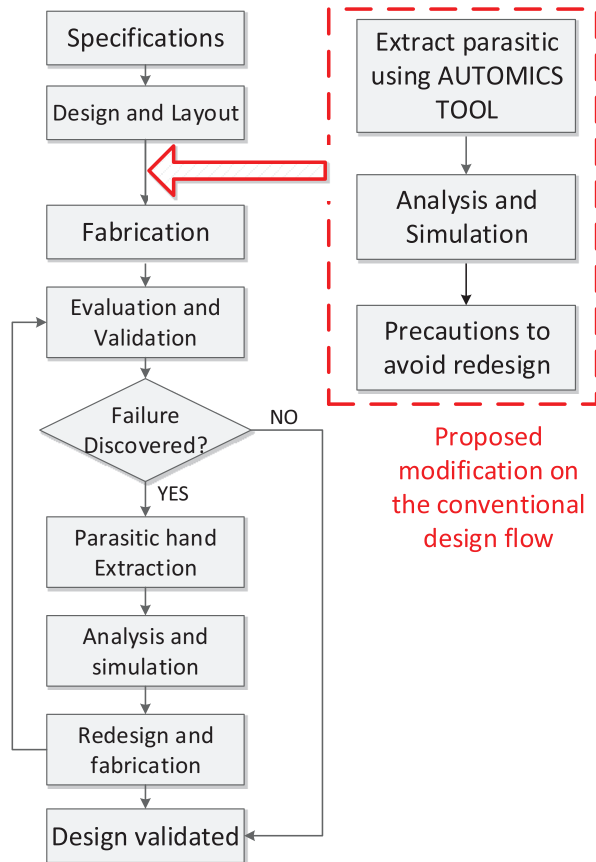

Figure 3 proposed design flow with AUTOMICS

IV. INDUSTRIAL CASE STUDY: AUTOCHIP 1

The AUTOCHIP1 is a smart power-IC developed in 0.35um HV-CMOS technology from AMS. It has been developed for 24V Valeo automotive technology applications and is able to sustain overvoltages up to 90V. It aims at controlling 28V up to 32V heavy duty alternators by rotor high current driver up to 5A in order to provide alternator output current to the battery and loads. It integrates on the same die a DC-DC converter to drive rotor coil, similar to the one described in [9], different I/O interfaces, a power management block and a small digital part that manage a serial communication with an external digital core, implemented on an FPGA. The FPGA solution has been chosen to increase the flexibility, like in [10].

This paper focuses on studying the DC-DC converter block. It includes a high-side switch and a low-side freewheeling diode. This stage regulates the current of the alternator rotor. One important point is the electrical connection and disconnection of the product that has high dV/dt up to 20V/ns that can be intermittent or during maintenance. In this section, the conventional procedure used to identify a problem in AUTOCHIP1 and our proposed methodology is discussed.

A. *Conventional problem identificaion*

The complete evaluation of the AUTOCHIP1 performances has been done in AMS and VALEO laboratories in parallel, performing the same tests and then cross-checking the results. One of the tests was the fast battery connection. Many fast battery connections at different temperatures and different voltages have been done. Through these tests, AUTOCHIP1 was very sensitive. As soon the battery is connected to a supply voltage of 50V, the device was severely damaged. Figure 4 shows the microphotograph of the AUTOCHIP1 after the test. The origin of this issue was a latch-up of the supply connection due to the activation of a parasitic SCR structure. Long investigations have taken more than three months, involving also emission microscope EMMI to localize and identify the p-n junctions in forward direction during the test, and substrate parasitic estimation. A new schematic has been done with involved substrate parasitics added by hand and simulated in order to replicate the measurement behavior. Since hand-made parasitic extraction was needed, as shown in Figure 5, many iterations were needed to rebuild the entire involved substrate network and to replicate correctly the measurement behavior. Such simulations are needed to increase the confidence level of the redesign and to validate the root cause explanation.

After reasoning and validation, a re-design to avoid the triggering of the parasitic SCR structure. AUTOCHIP2 was designed and simulated in conjunction with the hand-extracted substrate network. The fabricated AUTOCHIP2 manage to pass the battery connection test safely.

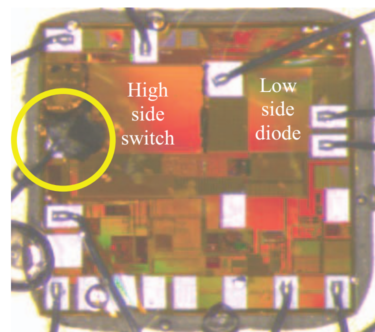

Figure 4 AUTOCHIP1 damage after battery connection

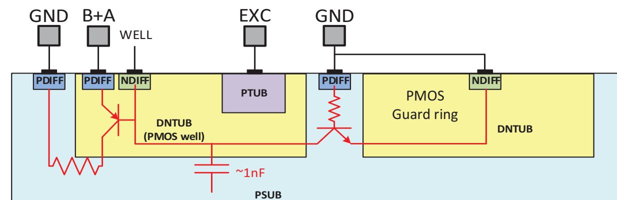

Figure 5 Example of substrate parasitic hand extraction

B. *Proposed problem identification*

Our proposed methodology can be used to identify such problem. At this stage, the layout of the design is available and can be processed by AUTOMICS tool. First, the calibration for the technology parameters is done to estimate the doping concentrations. Then, a reduction rules file is written to consider only the layers contributing in the substrate noise. For simplicity, only the deep Nwells and substrate contacts of the PMOS transistor are considered.

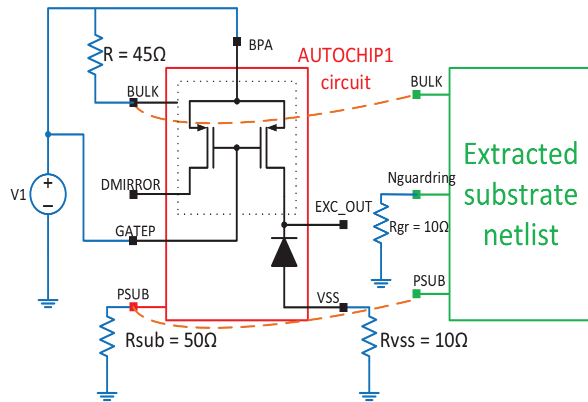

Figure 6 AUTOCHIP1 simulation testbench

The tool output is a schematic of the substrate parasitics. This schematic has three main terminals bulk of the PMOS, the N-type guard ring of the PMOS and the p-substrate contact. Figure 6 shows the testbench used for simulating AUTOCHIP1. It is noted that there is no connections for the guard rings in the design schematic as it is considered as a layout feature. The equivalent resistances of the contacts are estimated and inserted in the schematic. The voltage source V1 is set to 0V then ramps up to 12V in 10ns. As depicted in Figure 7, in case of circuit schematic only, a current spike appears at the supply connection and then the current returns to zero in fraction of microsecond. This indicates that the chip works properly. However, when the extracted substrate network is connected and the simulation is repeated. A holding current appears indicating the presence of a latched SCR structure. The results show an acceptable agreement with the measurement on the AUTOCHIP1. The simulation time and number of extracted components are shown in Table 1. The simulations were performed with a CPU six-core AMD Opteron (tm) Processor.

These results could be used by a designer to analyze the latchup structure and provide solution for this problem before fabrication. Obviously, using such tool would save long time for fabrication and redesign and consequently lowering the cost and ameliorate the circuit design.

Table 1 substrate simulation parameters

Number of extracted components	15083
Simulation CPU time (s)	12.5
Simulation elapsed time (s)	30.7

V. CONCLUSION

In this paper, we proposed a new methodology for analyzing smart power ICs. This methodology is based on extracting substrate parasitic components using a tool called AUTOMICS. The substrate is modeled as a network of diodes and resistors that preserve the continuity of the minority carrier propagation in the substrate. This aspect is essential for substrate analysis especially in case of high voltage and high temperature circuits. A test case of a chip called AUTOCHIP1 is presented. The parasitic hand-extraction took months plus the redesign and fabrication time. AUTOCHIP1 has been studied by the tool and the latch-up was detected. The proposed methodology gives an insight of the substrate behavior and shorten the time to market and hence reduces the cost.

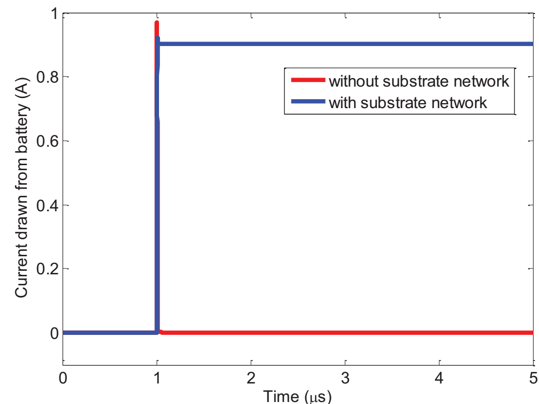

Figure 7 Simulation results with and without the extracted substrate network

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