Built-in Test of Millimeter-Wave Circuits Based on Non-Intrusive Sensors

Athanasios Dimakos^{*†}, Haralampos-G. Stratigopoulos[‡], Alexandre Siligaris[§], Salvador Mir^{*†}, and Emeric De Foucauld[§] ^{*}Université Grenoble Alpes, TIMA, F-38000 Grenoble, France [†]CNRS, TIMA, F-38000 Grenoble, France [‡]Sorbonne Universités, UPMC Univ. Paris 06, CNRS, LIP6, 4 place Jussieu, 75005 Paris, France [§]CEA-LETI, MINATEC Campus, 17 Rue des Martyrs, 38054 Grenoble, France

Abstract— This paper addresses the high-volume production test problem for millimeter-wave (mm-Wave) circuits. Bit error rate testing is the only feasible solution nowadays for mm-Wave transceivers, but is extremely costly and challenging to be implemented in high-volume production test floors. The lack of alternative solutions is due to the difficulty in extracting off-chip and processing mm-Wave frequencies. In this paper, we propose a built-in test solution that has two important attributes. First, it is based on non-intrusive sensors that are totally transparent to the mm-Wave circuit. They monitor variations in the performances of the mm-Wave circuit indirectly by virtue of offering an "image" of process variations. Second, the non-intrusive sensors operate at DC or low-frequency, thus dramatically simplifying the test of the mm-Wave circuit. We demonstrate the concept on a 65nm 60GHz mm-Wave low-noise amplifier (LNA).

Index Terms-mm-Wave circuit testing, built-in test, non-intrusive sensors, alternate test.

I. INTRODUCTION

The continuous scaling of CMOS processes down to 32nm and below has pushed the transit frequency and maximum oscillation frequency of transistors in excess of 230GHz, making them attractive for designing mm-Wave circuits and systems [1]. The need for designing high data-rate systems has led to several mm-Wave applications, including amplifiers and filters [2], gigabit/s point-to-point links, wireless local area networks (WLANs) with extraordinary capacity, shortrange high data-rate wireless personal area networks (WPANs) [3], and vehicular radar. The design of mm-Wave circuits and systems presents several challenges since it requires accurate modeling of active devices, passive components, interconnects, and transmission lines and it suffers largely from process, supply voltage, and temperature variations [4], [5]. Recent efforts focus on increasing the yield of mm-Wave circuits through calibration, adaptive circuit strategies, and self-healing algorithms [1], [6], [7].

The high-volume production test of mm-Wave circuits and systems is a major challenge towards their widespread adoption. The only standard test approach would be to rely on Automatic Test Equipment (ATE) with advance features and sophisticated calibration and de-embedding procedures and perform bit error rate testing based on a built-in loop-back connection [8]. However, this test approach incurs a high cost. In addition, the built-in loop connection requires a large area overhead and is very challenging from a design perspective since it needs to be carefully co-designed with the mm-Wave circuit to avoid performance degradation in the mm-Wave circuit.

In this work, we explore an alternative solution based on non-intrusive built-in sensors that have the comparative advantage that they are totally transparent to the mm-Wave circuit without degrading its performance and without requiring any co-design. The non-intrusive sensors are process control monitors integrated on the same die together with the mm-Wave circuit and offer an "image" of process variations. They incur low area overhead, they are tested at DC or low-frequency, and their outputs track variations in the performances of the mm-Wave circuit. Therefore, they can be used for enabling a low-cost alternate test approach where the performances of the mm-Wave circuit are inferred implicitly from the outputs of the non-intrusive sensors. This test strategy has been successfully applied in the past to data converters [9] and 2.4GHz RF circuits [10]-[12]. In this work, we demonstrate this test strategy on a 65nm 60GHz mm-Wave LNA.

The paper is organized as follows. In Section II, we present an overview of the proposed test strategy. In Section III, we discuss its benefits and disadvantages. In Section IV, we discuss the challenges and we provide some guidelines. In Section V, we present our case study. In Section VI, we present the selection of non-intrusive built-in sensors for our case study. In Section VII, we present and discuss in details our results and we point to directions for future work. Finally, in Section VIII we conclude the paper.

II. NON-INTRUSIVE BUILT-IN TEST: AN OVERVIEW

Considering any analog circuit, the underlying idea is to decompose it into "primitive" analog stages and critical single components and/or assemble basic analog stages from identical components that can be found in the circuit's topology. Analog stages may include bias stages, gain stages, current mirrors, level-shifters, etc., whereas single components may include transistors, resistors, capacitors, inductors, transmission lines, etc. Such analog stages and single components are then placed as "dummy" structures on the same die together with the circuit under test (CUT). In particular, they are placed in close physical proximity to the corresponding analog stages and components of the CUT that they are mimicking, such that corresponding analog stages and components are well matched following specific layout rules. We refer to the dummy structures as non-intrusive variation-aware sensors or simply non-intrusive sensors.

The underlying principle of operation is that, thanks to this physical proximity, the non-intrusive sensors will "witness"

the same die-to-die (D2D) and correlated within-die (WID) process variations as the corresponding structures in the CUT. As a result, we expect that measurements on the non-intrusive sensors (e.g. bias voltages, DC gain, transistor transconductance, resistance, capacitance, etc.) will offer an "image" of process variations within the CUT and, thereby, we expect that they will correlate to a large degree with the performances of the CUT. If such a correlation exists, then we expect that we will be able to predict the performances indirectly solely from the measurements on the non-intrusive sensors based on the alternate test paradigm [13].

Alternate test refers to a generic test approach that consists of inferring the performances of the CUT through unconventional, low-cost alternative measurements (e.g. the measurements provided by the non-intrusive sensors in our case). Formally, let M and P_i denote respectively the alternative measurement pattern and the *j*-th performance, j = 1, ..., n. The *n* mappings between *M* and P_j , j = 1, ..., n, do not have a closed-form mathematical expression and, thereby, they are modeled by n regression functions $f_j : M \rightarrow P_j$. The nregression functions are learned during an off-line training phase that employs a sample of fabricated instances of the CUT, which ideally should cover all the process corners and should be overall highly representative of the fabrication process. Once the n regression functions are learned, they can be readily used to infer the n performances of any instance simply through its alternative measurement pattern. For various practical ideas towards enhancing the efficiency of alternate test, the interested reader is referred to [13]-[17].

In short, the non-intrusive built-in test strategy capitalizes on the undesired phenomenon of process variations to provide low-cost alternative measurements from which performances can be predicted implicitly with accuracy.

III. BENEFITS AND DISADVANTAGES

The non-intrusive built-in test strategy presents several advantages:

- It is generic since virtually it is applicable to any analog circuit.
- It is low-cost since the test stimuli applied to the nonintrusive sensors and the measurements provided by the non-intrusive sensors are DC or low-frequency. In some cases, the non-intrusive sensors are self-biased. Thus, high-cost ATE with advanced features is no longer needed and, moreover, the inputs and outputs of the non-intrusive sensors can be multiplexed in a test bus so as to use a maximum of two pins for test.
- It is particularly attractive for RF and mm-Wave circuits since the built-in test circuitry is totally transparent to the CUT. In fact, design and test are completely dissociated.
- The CUT does not need to be powered-on during testing which largely facilitates parallel multi-site testing.

The disadvantages of the non-intrusive built-in test strategy are the following:

• It can only detect failures due to excessive process variations, thus it needs to be complemented with another test strategy that is capable of detecting defects. Recently,

it was shown that defects can also be detected nonintrusively based on temperature sensors [18].

• It cannot deal with uncorrelated WID variations (e.g. mismatch) that become important for advanced technology nodes from 65nm and below. Roughly speaking, the approach will fail if the uncorrelated WID variations start being comparable to D2D and correlated WID variations. It should be noticed, however, that the performances of RF and mm-Wave circuits do not depend on matching unless we consider fully differential topologies. Furthermore, mismatch appears as "noise" in the training set used to learn the regression functions in alternate test and, by default, the regression operation averages out this noise.

IV. CHALLENGES AND GUIDELINES

The main challenges of the non-intrusive built-in test strategy are the following:

- Identify the main process parameters (i.e. sheet resistance, oxide thickness, dopant concentration, junction capacitances, etc.) whose variation explains the variation in the performances of the CUT.
- Design non-intrusive sensors that capture and track variations in these process parameters.
- In addition, the non-intrusive sensors should be tested at DC or low-frequency and should incur low area overhead, in order to achieve a low cost.

There are several guidelines that can be followed towards addressing these challenges:

- A straightforward approach that has shown to work very well is to decompose the CUT into analog stages and single components and use as non-intrusive sensors identical dummy analog stages and single components.
- Process design kits for advanced technology nodes have hundreds of process parameters and it is not an easy task to dig into and fully understand the intricate relationships between the process parameters and the performances of a circuit. For this reason, we can rely on the main design parameters (transistors' geometry, transistors' transconductance, resistors' and capacitors' values, bias currents and voltages, etc.), which, in turn, are intricate functions of the process parameters, and choose to design nonintrusive sensors that capture effectively these design parameters. The designer's insights and input can be very valuable for performing this task.
- Rely on previous experience gained by applying the nonintrusive built-in test strategy to other circuit classes and/or other circuit architectures within the same circuit class. For example, the non-intrusive test strategy has been applied to a 2.4GHz RF LNA [11], [12] and conclusions from this case study can be explored towards applying the concept to a 60GHz mm-Wave LNA.
- Include an initial set of non-intrusive sensors that is the most straightforward from a conceptual point of view and perform an extensive simulation campaign to examine whether this set is largely sufficient. If not, the problem



Fig. 1. Schematic of 60GHz mm-Wave LNA.

of selecting non-intrusive sensors can be revisited and studied more thoroughly.

 Include a large set of non-intrusive sensors and then perform an extensive simulation campaign to study redundancy and keep the optimal set.

V. CASE STUDY

Our case study is a wideband 65nm 60GHz mm-Wave LNA. The circuit schematic comprises three single-ended amplifying stages, as shown in Fig. 1. The first stage uses a common source topology, in order to improve the NF, whereas the last two stages use a cascode topology, in order to achieve high gain and isolation. In addition, the two cascode amplification stages ensure an unconditional stability for the LNA in the 0-70GHz frequency range. Transistors in both the common source and the cascode amplification stages are biased at the strong-inversion side of moderate inversion, in order to achieve high transconductance efficiency, high transit frequency, and high bandwidth. Micro-strip transmission lines and short ended stubs are used for impedance matching, interconnect wiring, and the bias networks. The transmission lines at the gate and drain terminals of the transistors are used to supply bias and are also incorporated into the matching networks. Finally, the input and output of the LNA are AC-coupled and have been designed along with Ground-Signal-Ground (GSG) RF pads, in order to be matched at an impedance of 50Ω .

VI. NON-INTRUSIVE SENSORS DESIGN AND ALTERNATIVE MEASUREMENTS

Looking at the schematic in Fig. 1, we can directly identify two analog stages which we can replicate on the die as dummy and use them as non-intrusive sensors. In particular, we can use (a) a dummy common source stage composed of transistor M_1 and resistor R_1 , as shown in Fig. 2(a) and (b) a dummy cascode stage composed of transistors M_2 and M_3 and resistors R_2 , R_3 and R_4 , as shown in Fig. 2(b), noticing that the second and third stages that use a cascode topology are built from identical components. These dummy analog stages aim at monitoring the process variations that influence the gate and drain transconductances of the transistors of the 60GHz mm-Wave LNA. We use DC currents I_{DC1} and



Fig. 2. Non-intrusive variation-aware sensors built from identical analog stages and components that can be found in the topology of the 60GHz mm-Wave LNA.

 I_{DC2} as alternative measurements for the dummy common source and the dummy cascode stages, respectively, based on the test configurations shown in Fig. 2(a)-(b). Furthermore, we can use a dummy N+ poly resistor R_1 and a dummy metal-oxide-metal (MOM) capacitor C_1 , as shown in Fig. 2(c)-(d), in order to directly monitor variations in the N+poly resistors and MOM capacitors of the 60GHz mm-Wave LNA. For the dummy resistor we use the DC current I_{DC3} as alternative measurement based on the Ohm's law test configuration shown in Fig. 2(c). For the dummy capacitor, we extract the dummy capacitance C_1 from S-parameters at 100MHz using the expression

$$C_1 = \frac{\mathrm{Im}(\mathbf{Y}_{11})}{\omega}.$$
 (1)

This straightforward approach of extracting non-intrusive sensors from the topology of the CUT has shown to work very well for 2.4GHz RF LNAs as reported in [11], [12].

We also chose to monitor the gate resistance R_g of transistors since it is a design parameter that has a major impact on



Fig. 3. Layout view of the 60GHz mm-Wave LNA and the embedded non-intrusive variation-aware sensors.

impedance matching and noise at high frequencies. In principle, the gate resistance has a bias-independent component at DC and low frequencies, but it may include an additional component with bias dependence in high frequencies due to two additional effects, namely the distributed transmission line effect on the gate and the the non-quasi static effect in the channel [19]–[21]. The gate resistance is monitored by placing a dummy transistor M_1 , as shown in Fig. 2(e). In this test configuration, the dummy transistor M_1 is biased at the exact same DC bias conditions as the transistor M_1 of the 60GHz mm-Wave LNA in Fig. 1 and R_g is extracted from S-parameters at 100MHz using the expression

$$R_g = \frac{\text{Re}(Y_{11})}{(\text{Im}(Y_{11}))^2},$$
(2)

which is an approximation derived from the high-frequency small-signal equivalent transistor model [22].

Finally, we need also to account for variations in the transmission lines. We adopt a straightforward solution, which is to include in the set of non-intrusive sensors a dummy transmission line, as shown in Fig. 2(f). As alternative measurement we use the S_{11} extracted at a low frequency 100MHz, for which the inductance and capacitance of the transmission line are sensitized.

VII. SIMULATION RESULTS AND DISCUSSION

The 60GHz mm-Wave LNA and the non-intrusive sensors have been designed in the 65nm CMOS bulk technology of STMicroelectronics. The simulations are performed in the Cadence Virtuoso environment using the SpectreRF simulator.

Fig. 3 shows the layout pointing also to the placement of the LNA and the various non-intrusive sensors on the die. The dummy common source stage, the dummy cascode stage, and the dummy resistor are placed in close physical proximity to corresponding structures in the LNA. Excepting their pads, they can be considered as having zero overhead since their layout can be mingled with the layout of the LNA and placed in areas that are left void so as to respect electromagnetic design rules. The dummy capacitor has a relatively small value of 4.3pF and is placed close to its GSG RF pads so as to

 TABLE I

 LNA performances, nominal design value, and standard

 deviation when statistical variations in transmission lines are

(A) DISABLED AND (B) ENABLED.

_	Performance	Nominal Value	std (a)	std (b)
	S ₂₁ (dB)	16.4	0.87	0.97
	S_{11} (dB)	-15.39	1.04	1.09
	S22 (dB)	-17.99	2.49	2.4
	NF (dB)	5.69	0.23	0.27
	IIP ₃ (dBm)	-12.24	0.64	0.69

TABLE II Sets of non-intrusive sensors and corresponding groups of alternative measurements.

Set of Sensors	Alternative Measurements
А	$I_{DC1}, I_{DC2}, I_{DC3}, C_1$
В	$I_{DC1}, I_{DC2}, I_{DC3}, C_1, R_g$
С	R_g
D	$I_{DC1}, I_{DC2}, I_{DC3}, C_1, R_g, S_{11}$

perform a measurement that is as accurate as possible. Notice that in this design each of these dummy structures has its own dedicated pads. However, given that they are tested at DC or low-frequency, nothing would have prevented us from multiplexing their inputs and outputs so as to use only two pads and reduce the pad-dependent area overhead. On the other hand, the dummy structure for measuring R_g and the dummy transmission line occupy a large area on the die. A large fraction of this area is devoted to the de-embedding structures that should be used so as to estimate and remove the parasitics of the GSG RF pads. As we will see later on, while R_g is very useful in predicting variations in the performances, including the dummy transmission line in the set of non-intrusive sensors does not offer a significant advantage and, thus, we may as well choose to remove it.

Table I lists the LNA performances, the nominal design values, and the standard deviation observed in a Monte Carlo sample set of 1000 circuit instances considering both D2D and WID variations when statistical variations in transmission lines are (a) disabled and (b) enabled. Statistical models for D2D and WID variations are included into the process design kit of the technology. The library of components for this technology does not include transmission lines and, therefore, transmission lines are custom-built. The statistical model for the transmission lines is also custom-built and is rather pessimistic.

In the following analysis, we employ different sets of nonintrusive sensors and for each set we present the results of the alternate test. The sets of sensors and their corresponding groups of alternative measurements are shown in Table II. The regression functions in alternate test are learned using a training set of 800 Monte Carlo circuit instances and their generalization ability is evaluated on an independent validation set of 200 Monte Carlo circuit instances.

The prediction error of alternate test is expressed in terms of several error metrics, including the (a) average Root Mean Square (RMS) error expressed in %, (b) absolute average

2016 Design, Automation & Test in Europe Conference & Exhibition (DATE)

RMS error in units of each performance, (c) maximum error in units of each performance, and (d) Pearson correlation coefficient between the simulated (e.g. "true") and predicted performances expressed in %.

These metrics should be used with caution and judiciousness. The average RMS error metric offers an unspecific indication of prediction quality. It is commonly reported in alternate test experiments and we also include it in our analysis for the purpose of completeness. The average absolute RMS error and maximum error are the most informative error metrics since they allow us to make direct judgments about the quality of pass/fail test decisions after comparing the predicted performance to its specification. To speak of acceptable prediction results, the average absolute RMS error is recommended to be much smaller than one standard deviation of the performance, whereas the maximum error is recommended to be smaller than the measurement and repeatability errors in an ATE environment. Furthermore, we need to take into consideration the specification for each performance and the margin between the performance value with respect to the specification. No matter how large these error metrics are, if they are smaller than this margin, then the alternate test will not lead to any erroneous pass/fail test decisions. Finally, the Pearson correlation coefficient should be viewed with a pinch of salt. It offers a metric of linear correlation and a poor value does not necessarily imply poor prediction results that lead to erroneous pass/fail test decisions.

Table III shows the prediction results when using set A of non-intrusive sensors, which includes the dummy common source stage, the dummy cascode stage, the dummy resistor, and the dummy capacitor. In fact, this set contains the sensors with the minimum area overhead possible. As it can be seen, the prediction results are not very satisfactory, but already we observe that the average absolute RMS error is smaller or comparable to one standard deviation for each performance. The maximum error, however, can be as high as three standard deviations and is clearly higher than the measurement and repeatability errors for some performances, such as S_{21} and S_{22} .

Table IV shows the prediction results when using set B of non-intrusive sensors, where compared to set A of non-intrusive sensors we have added the dummy structure to measure R_g . As it can be seen, the prediction results have improved drastically. This is justified by the fact that variations in R_g explain to a large degree the variations of most performances, as can be attested by Table V where the set C of sensors contains only the dummy structure to measure R_g . As it can be seen from Table IV, for each performance the average absolute RMS error is smaller than one standard deviation. The maximum error, is smaller or at least comparable to the measurement and repeatability errors for all performances except S₂₂.

Table VI shows the prediction results when using set D of non-intrusive sensors, where compared to set B of non-intrusive sensors we have added the dummy transmission line. We observe that the prediction results compared to set B

TABLE III

ALTERNATE TEST PREDICTION RESULTS USING SET A OF NON-INTRUSIVE SENSORS.

Performance	Average RMS Error	Absolute Average RMS Error	Correlation Coefficient	Maximum Error
S_{21}	4.83 %	0.79 dB	64.07 %	3.08 dB
S ₁₁	6.41 %	0.98 dB	47.82 %	2.41 dB
S ₂₂	9.68 %	1.74 dB	64.31 %	4.16 dB
NF	4.74 %	0.27 dB	12.55 %	0.62 dB
IIP_3	5.11 %	0.63 dBm	34.55 %	1.45 dBm

TABLE IV

Alternate test prediction results using Set B of non-intrusive sensors.

Performance	Average RMS Error	Absolute Average RMS Error	Correlation Coefficient	Maximum Error
S ₂₁	3.77 %	0.62 dB	80.03 %	2.36 dB
S_{11}	3.42 %	0.53 dB	88.39 %	1.37 dB
S ₂₂	9.68 %	1.74 dB	63.78 %	5.19 dB
NF	2.71 %	0.15 dB	81.40 %	0.41 dB
IIP_3	3.13 %	0.38 dBm	81.09 %	1.07 dBm

TABLE V

Alternate test prediction results using Set C of non-intrusive sensors.

Performance	Average RMS Error	Absolute Average RMS Error	Correlation Coefficient	Maximum Error
S ₂₁	5.60 %	0.92 dB	46.65 %	4.35 dB
S_{11}	5.09 %	0.78 dB	71.82 %	2.42 dB
S ₂₂	12.68 %	2.28 dB	8.25 %	7.24 dB
NF	2.69 %	0.15 dB	81.73 %	0.41 dB
IIP_3	3.54 %	0.43 dBm	75.01 %	0.93 dBm

TABLE VI

Alternate test prediction results using Set D of non-intrusive sensors.

Performance	Average RMS Error	Absolute Average RMS Error	Correlation Coefficient	Maximum Error
S ₂₁	3.16 %	0.52 dB	86.40 %	1.69 dB
S ₁₁	3.14 %	0.48 dB	90.25 %	0.95 dB
S ₂₂	9.40 %	1.69 dB	65.76 %	4.11 dB
NF	2.29 %	0.13 dB	87.14 %	0.38 dB
IIP_3	2.39 %	0.29 dBm	89.63 %	0.64 dBm

have improved appreciably but not dramatically, implying that variations in the transmission lines are not the main source of performance variability. This can also be justified by Table I where we observe that the standard deviation does not vary appreciably when statistical variations in transmission lines are disabled or enabled. We argue that it is perhaps a wiser choice not to deploy a dummy transmission line for the following reasons: (a) the prediction results for set B of non-intrusive sensors are already deemed excellent for all performances except S_{22} ; (b) the dummy transmission line does not improve the error metrics for S_{22} ; (c) the statistical model for the transmission line is rather pessimistic as mentioned above, implying that the prediction results for set B of non-intrusive sensors are expected to be better; and (d) the dummy transmission line

2016 Design, Automation & Test in Europe Conference & Exhibition (DATE)

occupies a large area overhead.

Regarding the unsatisfactory maximum error for S_{22} , it is clear that the main process parameters that affect S_{22} are not well covered by the set of non-intrusive sensors. We studied the process parameters on which S_{22} strongly depends and we believe that the error metrics for S_{22} can be improved if we monitor variations in the silicon substrate of transistors. It is well known that, unlike at DC and low frequencies, substrate resistance begins to contribute at high frequencies, where the signal at the drain couples to the source and bulk terminals through the source/drain junction capacitance and the substrate itself. As reported in [23], [24], the substrate resistance affects mainly the output characteristics and can contribute as much as 20% or more to the total output admittance. In terms of future work, we will aim at developing a non-intrusive sensor specifically for S_{22} and demonstrate the idea on silicon.

VIII. CONCLUSIONS

In this paper we demonstrated a non-intrusive test strategy based on variation-aware sensors for a 65nm 60GHz mm-Wave LNA. Tapping into the signal paths of mm-Wave circuits, in order to extract useful information for testing, is utterly intolerable from a design point of view. Therefore, a standard loop-back test strategy for the complete transceiver or a nonintrusive test strategy, such as the one presented for the first time in this paper, for the complete transceiver or for its individual blocks, are the only candidate solutions. Compared to the loop-back test strategy, the non-intrusive test strategy has the comparative advantage that it incurs a much lower test cost at the expense of predicting the performances rather than measuring them directly. We demonstrated that by placing simple dummy analog stages and dummy single components on the die and by obtaining on these dummy structures simple DC or low-frequency measurements that offer an "image" of process variations, we are able to track variations in all performances except S₂₂ with an average error smaller than one standard deviation and a maximum error smaller or at least comparable to the measurement and repeatability errors in an ATE environment.

REFERENCES

- C. Maxey, G. Creech, S. Raman, J. Rockway, K. Groves, T. Quach, L. Orlando, and A. Mattamana, "Mixed-signal SoCs with in situ self-healing circuitry," *IEEE Design & Test of Computers*, vol. 29, no. 6, pp. 27–39, 2012.
- [2] C.H. Doan, S. Emami, A.M. Niknejad, and R. Brodersen, "Millimeter-wave CMOS design," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 1, pp. 144–155, 2005.
- [3] A. Siligaris, C. Mounet, B. Reig, P. Vincent, and A. Michel, "CMOS SOI technology for WPAN. Application to 60 GHz LNA," in *Proc. IEEE International Conference on Integrated Circuit Design and Technology and Tutorial*, 2008, pp. 17–20.
- [4] C.H. Doan, S. Emami, A.M. Niknejad, and R. W. Brodersen, "Millimeter-wave CMOS device modeling and simulation," in *Proc. IEEE International Symposium on Circuits and Systems*, 2004, pp. V–524–V–527.
- [5] D. Heo and J. Kim, "Guest editors introduction: Design and testing of millimeter-wave/subterahertz circuits and systems," *IEEE Design & Test*, vol. 31, no. 6, pp. 6–7, 2014.

- [6] A. Kazemipour, M. Salhi, T. Kleine-Ostmann, and T. Schrader, "A simple new method to calibrate millimeter-wave mixers," *IEEE Design & Test*, vol. 31, no. 6, pp. 46–51, 2014.
- [7] J.O. Plouchart, B. Parker, B. Sadhu, A. Valdes-Garcia, D. Friedman, M. Sanduleanu, F. Wang, X. Li, and A. Balteanu, "Adaptive circuit design methodology and test applied to millimeterwave circuits," *IEEE Design & Test*, vol. 31, no. 6, pp. 8–18, 2014.
- [8] R.L. Schmid, P. Song, C.T. Coen, A. C. Ulusoy, and J.D. Cressler, "A W-band integrated silicon-germanium loop-back and front-end transmit-receive switch for built-in-self-test," in *Proc. IEEE MTT-S International Microwave Symposium*, 2015.
- [9] A. Zjajo, M. J. Barragan Asian, and J. Pyneda de Gyvez, "BIST method for die-level process parameter variation monitoring in analog/mixed-signal integrated circuits," in *Proc. Design*, *Automation & Test in Europe Conference*, 2007, pp. 1301–1306.
- [10] L. Abdallah, H.-G. Stratigopoulos, S. Mir, and C. Kelma, "RF front-end test using built-in sensors," *IEEE Design & Test of Computers*, vol. 28, no. 6, pp. 76–84, 2011.
- [11] L. Abdallah, H.-G. Stratigopoulos, S. Mir, and C. Kelma, "Experiences with non-intrusive sensors for RF built-in test," in *Proc. IEEE International Test Conference*, 2012, Paper 17.1.
- [12] A. Dimakos, H.-G. Stratigopoulos, A. Siligaris, S. Mir, and E. De Foucauld, "Parametric built-in test for 65nm RF LNA using non-intrusive variation-aware sensors," *Journal of Electronic Testing: Theory and Applications*, vol. 31, no. 4, pp. 381–394, 2015.
- [13] P. N. Variyam, S. Cherubal, and A. Chatterjee, "Prediction of analog performance parameters using fast transient testing," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 21, no. 3, pp. 349–361, 2002.
- [14] H. Ayari, F. Azais, S. Bernard, M. Compte, V. Kerzerho, O. Potin, and M. Renovell, "Making predictive analog/RF alternate test strategy independent of training set size," in *Proc. IEEE International Test Conference*, 2012, Paper 10.1.
- [15] H.-G. Stratigopoulos and S. Mir, "Adaptive alternate analog test," *IEEE Design & Test of Computers*, vol. 29, no. 4, pp. 71–79, 2012.
- [16] M. J. Barragan and G. Léger, "A procedure for alternate test feature design and selection," *IEEE Design & Test of Computers*, vol. 32, no. 1, pp. 18–25, 2015.
- [17] J. Liaperdos, H.-G. Stratigopoulos, L. Abdallah, Y. Tsiatouhas, A. Arapoyanni, and X. Li, "Fast deployment of alternate analog test using bayesian model fusion," in *Proc. Design, Automation* and *Test in Europe Conference*, 2015.
- [18] L. Abdallah, H.-G. Stratigopoulos, S. Mir, and J. Altet, "Defectoriented non-intrusive RF test using on-chip temperature sensors," in *Proc. IEEE VLSI Test Symposium*, 2013.
- [19] X. Jin, J.-J. Jiunn, C.-H. Chen, W. Liu, M. J. Deen, P. R. Gray, and C. Hu, "An effective gate resistance model for CMOS RF and noise modeling," in *Proc. International Electron Devices Meeting*, 1998, pp. 961–964.
- [20] Y. Cheng and M. Matloubian, "High frequency characterization of gate resistance in RF MOSFETs," *IEEE Electron Device Letters*, vol. 22, no. 2, pp. 98–100, 2001.
- [21] Y. Cheng, M. J. Deen, and C.H. Chen, "MOSFET modeling for RF IC design," *IEEE Transactions on Electron Devices*, vol. 52, no. 7, pp. 1286–1303, 2005.
- [22] C. Enz, "An MOS transistor model for RF IC design valid in all regions of operation," *IEEE Transactions on Microwave Theory* and Techniques, vol. 50, no. 1, pp. 342–359, 2000.
- [23] S. H. Jen, C. Enz, D. R. Pehlke, M. Schroter, and B. J. Sheu, "Accurate MOS transistor modeling and parameter extraction valid up to 10-GHz," in *Proc. European Solid-State Device Research Conference*, 1998, pp. 484–487.
- [24] C. Enz and Y. Cheng, "MOS transistor modeling for RF IC design," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 2, pp. 186–201, 2000.