Analysis of NBTI Effects on High Frequency Digital Circuits

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***Abstract*—This paper analyzes some of the secondary effects in estimating negative bias temperature instability (NBTI) induced threshold voltage shift on high frequency digital circuits. Therefore, a circuit model is developed to be used for statistical estimation of the threshold voltage shift. Making use of this model as well as technology computer aided design (TCAD) and SPICE simulations, a methodology is developed to estimate NBTI induced threshold voltage shift. Simulation results reveal that commonly made assumptions on digital circuits, such as: square signal assumption and ignorable effect of drain bias, may yield overestimation of the NBTI induced threshold voltage shift by more than 10% after five years of operation, which may lead to a severe underestimation of a circuit's reliability.**

I. Introduction

Negative bias temperature instability (NBTI) is one of the major reliability concerns in nanometric PMOS devices. It is well known that some of the resulting threshold voltage shift due to NBTI, recovers after removing the negative bias voltage from the device. Conventionally, NBTI was explained by the reaction-diffusion theory [1], however recent studies point out that the charge trapping is the dominant contributor to the threshold voltage shift [2].

Almost all NBTI studies on digital circuits assume perfect (square) digital signals. In reality, if a circuit is operating at a very high frequency f, e.g. $f \approx 1$GHz, the wave shapes of the signals could not be assumed to be square. For the sake of clarity, gate-to-source V_{gs} and drain-to-source V_{ds} voltages of a 21-inverter ring oscillator are shown in Fig. 1, where V_{gs} and V_{ds} are not at high/low levels during 23% of the time. If a 9-inverter ring oscillator is analyzed, this ratio increases to 53%. It is clear that the square signal assumption is not valid for frequently switching circuits. It is shown in [3] that the shape of the V_{gs} signal affects the NBTI induced threshold voltage shift (ΔV_T). Therefore, square wave assumption might yield incorrect lifetime estimation for a high frequency digital circuit.

Also ignoring the drain bias of a transistor causes error in lifetime estimation. To be able to detach the hot carrier and the NBTI effects, silicon measurements are normally conducted by stressing the gate terminal of a transistor and grounding its remaining terminals. However, in many applications transistors operate at non-zero drain bias conditions and the silicon measurement could not be directly used. As an example, the drain bias V_{ds} shown in Fig. 1 is not at 0V during 62% of the time. The graph in Fig. 2 is re-drawn from [4], and shows that

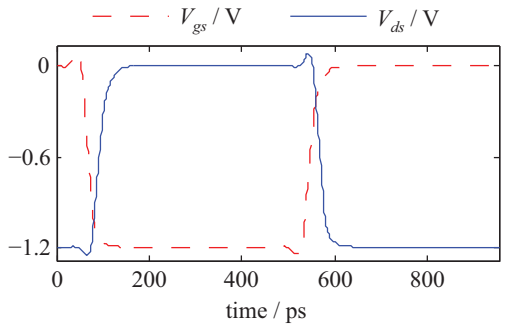

Fig. 1. Voltages V_{gs} and V_{ds} on a PMOS Transistor in a 21-Inverter Ring Oscillator with $L = 100$nm.

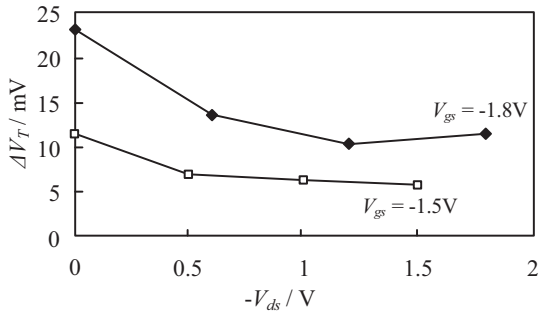

Fig. 2. ΔV_T vs. V_{ds} for a PMOS transistor with $L = 0.7\mu$m which is stressed at 125°C for 1000s. Re-Drawn from Fig. 6 of [4].

V_T shifts more if V_{ds} is set to 0, compared to the case where V_{ds} is set to -1V. Drain–bias NBTI is highly pronounced on advanced technologies as measurements on 40nm devices yield [4]. Thus, ignoring the drain bias would result in an erroneous lifetime estimation.

Moreover, shapes of the signals in a digital circuit change as the circuit ages, due to the increase in the propagation delays of the gates. As previously discussed, V_T shift due to NBTI depends on the shape of the signal, therefore the rate of aging changes in time. Consequently, rate of degradation for a fresh circuit is not same as the rate of degradation for an old circuit. Supporting the discussion, a fresh and an old 9-inverter ring oscillator circuits are simulated and the resulting V_{gs} signals are shown in Fig. 3, where the shapes of the two signals differ slightly, which indicates a shift in the rate of V_T degradation.

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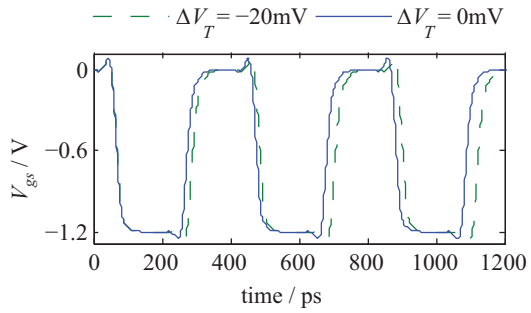


Fig. 3. V_{gs} of PMOS Transistors: a Fresh ($\Delta V_T = 0$V) and an Old ($\Delta V_T = -20$mV) 9-Inverter Ring Oscillator Circuit where $L = 100$nm.

This work is based on a statistical charge trap model [5] and analyzes the impacts of the three mentioned facts (non-square signals, drain bias and aging) on NBTI induced ΔV_T estimation. A brief review of the previous works as well as an overview of charge trap statistics may be found in Section II. To our knowledge, this is the first study which shows the error in estimating NBTI induced ΔV_T for high frequency digital circuits. Main contributions of this paper may be listed as:

- A circuit model is developed to simulate NBTI induced ΔV_T under periodic stress and presented in Section III.
- A methodology is developed to analyze NBTI induced effects on high frequency digital circuits and presented in Section IV.
- Shift in V_T due to signal imperfections, drain bias and shift in aging parameters are analyzed in Section V. Based on the simulation results, it is reported that ignoring these effect may result in overestimation of NBTI induced ΔV_T by more than 10% after five years of operation.

In this paper, due to their high operating frequency, ring oscillators are used. However, given the statistics of the input signals, the proposed methodology may be applied to other digital circuit.

II. Related Work and Background

Secondary effects (e.g. leakage [6]), variability, as well as reliability (e.g. NBTI [1], [2]) of MOS devices are extensively studied in the literature. At elevated temperatures, the threshold shift due to NBTI is reported as a dominating effect and analyzed by many researchers, e.g. [7]. More specifically, the frequency dependence of NBTI has also been analyzed in several works, e.g. [8]–[10]. Recent studies report that NBTI has some dependency to input signal frequency [11], [12]. Cited works [8]–[12] aim to understand the physics of NBTI and model it on single devices, thus real operating conditions of the devices are not in their scope. On the other hand, almost all papers analyzing NBTI on digital circuits simplify the operating conditions by assuming the inputs to the gates are pure digital (square) signals and ignoring the drain bias V_{ds}. The studies [4] and [13] show that the drain bias has a significant effect on NBTI induced ΔV_T and could not be ignored. It is discussed in [13] that the threshold voltage V_T of a PMOS device decreases when a negative V_{ds} bias is applied, however the V_T might increase when a more negative V_{ds} bias is applied due to the hot carrier effect. Also, the assumption of square signals is not valid at high frequencies and it is shown in [3] that the shape of the V_{gs} signal effects the NBTI induced threshold voltage shift without taking the V_{ds} into account.

Our study not only accounts for the signal shapes but also for the drain bias V_{ds} . To our knowledge, this paper is the first study reporting the estimation error in ΔV_T on high frequency digital circuits, due to commonly applied simplifications. Rest of this section contains a brief overview of charge trap statistics.

The probability of finding a trap filled at any time t is [15]:

$$p(t) = \frac{\tau_e}{\tau_e + \tau_c} + A \cdot e^{-t\cdot\left(\frac{1}{\tau_e}+\frac{1}{\tau_c}\right)} \tag{1}$$

where the constant A depends on the initial conditions; τ_c and τ_e are the mean times before an electron is captured and emitted by the trap, respectively. If a transistor is considered, these mean times depend on the bias conditions. In this paper, mean times τ_c and τ_e are referred as capture and emission time constants, respectively and their values are extracted from silicon measurements [2], [14].

If an occupied trap causes a shift of ΔV_t in the threshold voltage of a transistor then the expected value of the threshold shift at any time t is:

$$v_t(t) = p(t) \cdot \Delta V_t + (1 - p(t)) \cdot 0 = p(t) \cdot \Delta V_t \tag{2}$$

and $v_t(t)$ may be rewritten as:

$$v_t(t) = \Delta V_t \cdot \frac{\tau_e}{\tau_e + \tau_c} + B \cdot e^{-t\cdot\left(\frac{1}{\tau_e}+\frac{1}{\tau_c}\right)} \tag{3}$$

where B is a constant. Time constants τ_c and τ_e are specific for each trap and depend on the transistor bias.

For a periodic digital signal with a period of T, where $T \ll \tau_c$ and $T \ll \tau_e$, an effective value for the time constant of capture τ_c^* may be calculated [15] as:

$$\tau_c^* = \left[\frac{D}{\tau_{c_H}} + \frac{1-D}{\tau_{c_L}}\right]^{-1} \tag{4}$$

where D is the duty cycle of the signal, τ_{c_H} and τ_{c_L} are the capture time constants when the signal is at high and low levels, respectively. Similarly, an effective value for the time constant of emission may be calculated.

III. A Circuit Model for Statistical Analysis

The expected value of the threshold voltage shift v_t due to a trap is given in (3). In this section v_t is modeled by a resistor-capacitor (RC) network, which is suitable to be used with SPICE simulations.

For a single trap, the proposed circuit model is shown in Fig. 4a, where the voltage source is set to a value of ΔV_t which is the resulting threshold shift when the trap is occupied. For the sake of simplicity, the capacitor in the model is fixed at 1F. The resistors are proportional to the capture and the emission

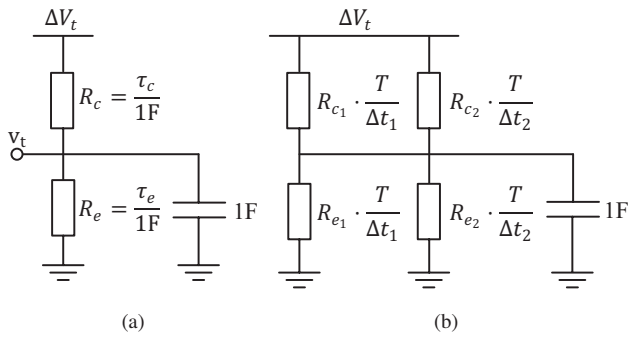


Fig. 4. Circuit Model for Statistical ΔV_T Estimation (a) General Model, (b) Model for a Square Signal Driven Transistor

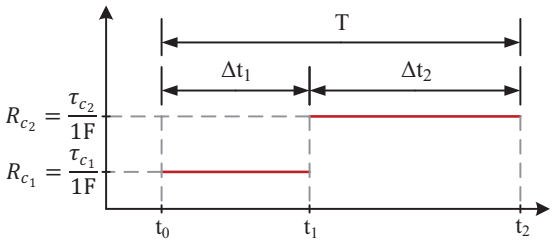


Fig. 5. A Sample Case where R_c Changes Periodically with a Period of T

time constants. Solving the governing differential equation, the potential difference on the capacitor v_t may be written as:

$$v_t(t) = \Delta V_t \cdot \frac{\tau_e}{\tau_e + \tau_c} + \left[v_0 - \Delta V_t \cdot \frac{\tau_e}{\tau_e + \tau_c} \right] \cdot e^{-t \cdot \left(\frac{1}{\tau_e} + \frac{1}{\tau_c} \right)} \quad (5)$$

where v_0 is the initial potential difference on the capacitor. This solution has the same form as the expected threshold shift in (3), and verifies the proposed model. The solution in (5) is only valid if the resistors (thus τ_c and τ_e) in Fig. 4a have constant values. However, resistors (thus τ_c and τ_e) depend on the transistor bias (V_{gs} and V_{ds}) and could not be assumed to have constant values. On the other hand, if the bias changes periodically and the frequency is relatively high, effective resistances may be calculated for the model in Fig. 4a.

Let a square signal is applied to a PMOS device causing the value of the resistor R_c in Fig. 4a to vary in time as shown in Fig. 5, where T is the period of the signal. If $T \ll \tau_c$ and $T \ll \tau_e$, the voltage on the capacitor $v_t(t)$ may be accepted as constant during a period. Then, total charge absorbed from the source in a single period may be written as:

$$Q_{\Delta V_t}^{t_0 \to t_2} = \frac{\Delta V_t - v_t}{R_{c_1}} \cdot \Delta t_1 + \frac{\Delta V_t - v_t}{R_{c_2}} \cdot \Delta t_2 \quad (6)$$

Based on this equation, an average source current could be calculated as:

$$I_{\Delta V_t}^* = \frac{Q_{\Delta V_t}^{t_0 \to t_2}}{T} = \frac{\Delta V_t - v_t}{R_{c_1}} \cdot \frac{\Delta t_1}{T} + \frac{\Delta V_t - v_t}{R_{c_2}} \cdot \frac{\Delta t_2}{T} \quad (7)$$

and using this current, an average resistance R_c^* could be defined as:

$$R_c^* = \left[\frac{I_{\Delta V_t}^*}{\Delta V_t - v_t} \right]^{-1} \quad (8)$$

$$= \left[\frac{1}{R_{c_1}} \cdot \frac{\Delta t_1}{T} + \frac{1}{R_{c_2}} \cdot \frac{\Delta t_2}{T} \right]^{-1} \quad (9)$$

$$= \left(R_{c_1} \cdot \frac{T}{\Delta t_1} \right) \parallel \left(R_{c_2} \cdot \frac{T}{\Delta t_2} \right) \quad (10)$$

As formulated in (10), R_c^* is a parallel combination of two resistors. Following a similar derivation, an average resistor R_e^* may also be calculated. Replacing the resistors in Fig. 4a with the corresponding parallel combinations the model in Fig. 4b could be obtained for the given scenario in Fig. 5. The model in Fig. 4a may be extended for any periodic signal. Using (9) and the definitions in Fig. 4a, an effective time constant could be formulated as:

$$\tau_c^* = \left[\frac{\frac{\Delta t_1}{T}}{\tau_{c_1}} + \frac{1 - \frac{\Delta t_1}{T}}{\tau_{c_2}} \right]^{-1} \quad (11)$$

This equality is same as the one given in (4). Replacing τ_c and τ_e in Fig. 4a with τ_c^* and τ_e^*, a closed-form solution, which is valid for any time is obtained:

$$v_t(t) = \Delta V_T \cdot \frac{\tau_e^*}{\tau_e^* + \tau_c^*} + \left[v_0 - \Delta V_T \cdot \frac{\tau_e^*}{\tau_e^* + \tau_c^*} \right] \cdot e^{-t \cdot \left(\frac{1}{\tau_e^*} + \frac{1}{\tau_c^*} \right)} \quad (12)$$

For any periodic signal, where $T \ll \tau_c$ and $T \ll \tau_e$, effective time constants τ_c^* and τ_e^* may be calculated and the solution in (12) would be valid.

The presented circuit model is inspired from [16], where the time constants for different signal levels are separated by diodes.

IV. Methodology

To be able to analyze the NBTI induced V_T shift on high frequency digital circuits, a special simulation methodology is developed which utilizes silicon measurement, technology computer aided design (TCAD) and SPICE simulations. The methodology is separated into three steps and a flow diagram is given for each step in Fig. 6. TCAD simulations are conducted in the first step and a lookup-table (LUT1) is constructed. This table and the data from silicon measurements are used in the next step to construct a second lookup-table (LUT2). These tables LUT1 and LUT2 are used in the final step to analyze the results of SPICE simulations and to estimate ΔV_T.

A. TCAD Simulations

As discussed in Section I, to detach the NBTI and the hot carrier effects, V_{ds} of a PMOS device is kept at zero bias during silicon measurements. However, in reality V_{ds} changes in time and is not fixed at 0V. A methodology is needed to estimate the trap data (τ_c and τ_e) for bias conditions where $V_{ds} \neq 0$V.

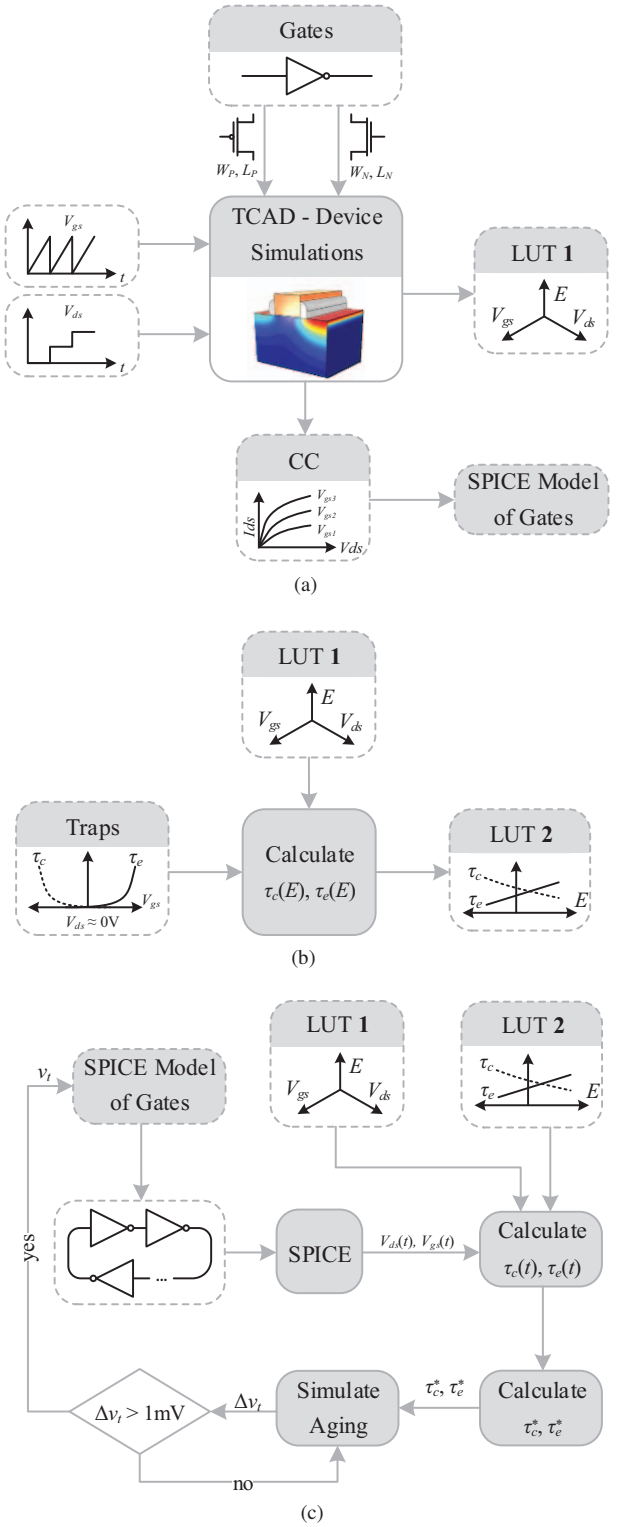


Fig. 6. Methodology (a) TCAD Simulations Conducted, (b) Time Constants Calculated, (c) NBTI Induced Shift in Threshold Voltage Estimated.

For a set of V_{ds} and V_{gs} values, the electric field is calculated via TCAD simulations, and the simulation results are stored in a 2-D lookup table (LUT1). When $|V_{gs}|$ is set to a relatively low voltage or $|V_{ds}|$ is set to a relatively high voltage, the vertical electric field in the channel would not be uniform. In these cases, the vertical electric field in the effective channel is averaged and stored into LUT1. Also, characteristic curves (CC) are extracted from the conducted TCAD simulations and based on these CCs, SPICE models are generated. The flow is visualized in Fig. 6a.

B. Calculation of the Time Constants

In this step, capture and emission time constants, extracted from silicon measurements [2], [14], and the lookup-table LUT1 are used to calculate the time constants as functions of the vertical electric field E. More formally, a change of variable is used to obtain $\tau_c(E)$ and $\tau_e(E)$ from $\tau_c(V_{gs})$ and $\tau_e(V_{gs})$, respectively. Calculated time constants are stored in a second lookup-table LUT2, which maps the electric field to the time constants. The process in this step is visualized in Fig. 6b.

C. Estimation of the Threshold Shift

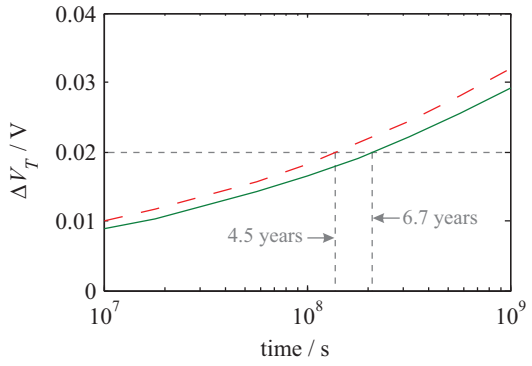
The table LUT1 stores the function $E(V_{gs}, V_{ds})$ and the table LUT2 stores the functions $\tau_c(E)$ and $\tau_e(E)$. These tables may be merged in a new lookup-table which stores the functions $\tau_c(V_{gs}, V_{ds})$ and $\tau_e(V_{gs}, V_{ds})$. The results of the SPICE simulation, $V_{gs}(t)$ and $V_{ds}(t)$, and the new table could be used to calculate τ_c and τ_e as functions of time. Having calculated $\tau_c(t)$ and $\tau_e(t)$, the model in Section III may be used to calculate the effective time constants, τ_c^* and τ_e^* and finally, the solution in (12) may be used to estimate the NBTI induced V_T shift at any time t.

The flow diagram for this step is shown Fig. 6c. To make a better lifetime estimation, the shift in the aging parameters are also taken into consideration and the SPICE model is updated when the change in its V_T is more than 1mV.

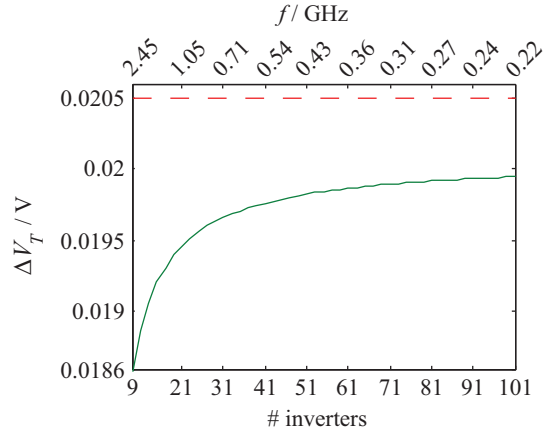
V. Results

Analyzing the NBTI induced ΔV_T, it is common to simplify the analysis by assuming the V_{gs} signal has a square shape and ignoring the drain bias as well as the shift in aging parameters. As shown in Fig. 3, the shape of a V_{gs} signal may deviate from a square wave at high frequencies. In addition, the Fig. 2 re-drawn from [4], shows ΔV_T depends on the applied V_{ds} bias. Moreover, rate of degradation for a fresh circuit is different than that for an old circuit. For instance, V_{gs} signals are shown for a fresh and a stressed ring-oscillator in Fig. 3, where τ_c^* of a trap decreased by 5.6% and τ_e^* of the trap increased by 4.3% after the stress. As a conclusion, those simplifications would yield an error in estimation of the NBTI induced ΔV_T. The methodology described in Section IV is used to estimate the error due to those simplifications, namely: imperfect square signals, the drain bias, and the shift in aging parameters.

To be able to simulate the simplified case, the flow in Fig. 6c is modified by reseting the V_{ds} signal, obtained from SPICE simulations, to 0V, thus only the V_{gs} signal is used. Also, the V_T update in the loop is disabled and a thresholding is applied to the V_{gs} signal. On the other hand, in simulating

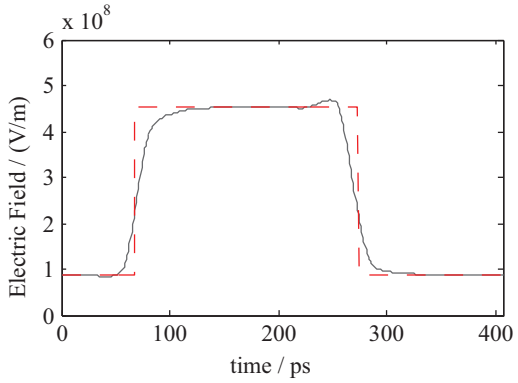


(a)

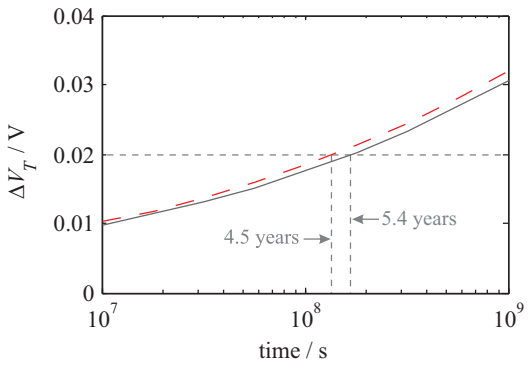


(b)

Fig. 7. Estimation Error in NBTI induced Threshold Voltage Shift where $L = 100$nm and Stressed at 125°C. Long Dashed Curves for Simplified Signals and Solid Curves for Real Signals (a) Shift in Threshold Voltage of 9-inverter Ring-Oscillator (b) Threshold Voltage Shift of Ring-Oscillators Running at Different Frequencies after 5 Years of Operation



(a)



(b)

Fig. 8. Effect of Signal Shape in Threshold Voltage Shift on a 9-inverter Ring-Oscillator. Long Dashed Curves for Squared V_{gs} Signals and Solid Curves for Real V_{gs} Signals (a) Electric Field vs. Time (b) Threshold Voltage Shift in Time where $L = 100$nm and Stressed at 125°C

the real case the flow is used as it is in Fig. 6c. Simulation results of the simplified case are compared with the real case and the results are given in Fig. 7a. It is observed that for the simplified case the NBTI induced ΔV_T is overestimated by 10.2% after 5 years of operation. If an NBTI induced threshold shift of 20mV limits the life time, then the simplified case underestimates the lifetime by 33%.

Estimated ΔV_T shifts, due to NBTI after five years of operation, for different ring oscillators are shown in Fig. 7b. The dashed line shows ΔV_T for the simplified case and the solid curve shows ΔV_T for the real case. This graph reveals that threshold voltages of all transistors are less effected under real operating conditions compared to simplified case, especially the transistors in high frequency ring oscillators, from the NBTI induced degradation.

In the following sections, the effects are analyzed one at a time and depending on the analysis, some parts of the flow, shown in Fig. 6c, are disabled or bypassed.

A. *Effects of Rise & Fall Times and Overshoots*

To analyze the error in ΔV_T due to the effects of rise/fall times and the signal overshoots, a modified version of the flow in Fig. 6c is used, where the V_{ds} signal, obtained from SPICE simulations, is reset to 0V and only the V_{gs} signal is used. Also, the V_T update in the loop is disabled. In addition, while conducting the simulations for the square signal case a thresholding is applied to the V_{gs} signal.

In Fig. 8a, the resulting electric fields are shown as functions of time, where the dashed curve is obtained when a square signal is applied and the solid curve is obtain when the real V_{gs} signal is applied. Note that the V_{ds} is kept at 0V for both cases. Corresponding threshold shifts are shown in Fig. 8b.

Simulation results reveal that under the square signal assumption, the NBTI effect in ΔV_T on a 9-inverter ring oscillator is overestimated by 4.5% after five years of operation. If an NBTI induced threshold shift of 20mV limits the life time, then the square signal assumption underestimates the lifetime by 17%. Although overshoots were reported to increase the NBTI induced threshold voltage degradation [3], the effect of rise and fall times are observed to overwhelm that effect as shown in Fig. 8.

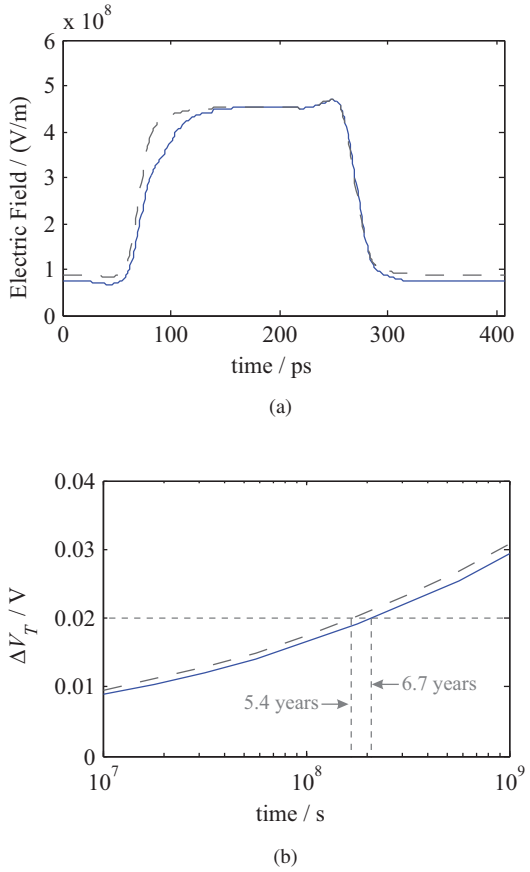


Fig. 9. Effect of Drain Biasing in Threshold Voltage Shift on a 9-inverter Ring-Oscillator. Long Dashed Curves for $V_{ds} = 0$V and Solid Curves for Real Biasing (a) Electric Field vs. Time (b) Shift in Threshold Voltage where $L = 100$nm and Stressed at 125°C

B. Effect of Drain Bias

Analyzing the effect of drain bias, the flow in Fig. 6c is used and the V_T feedback is disabled. First, the V_{ds} signal obtained from SPICE simulations are reset to 0V and the ring oscillator circuit is analyzed. Next, the analysis is repeated without reseting the V_{ds} signal. The resulting electric fields are shown in Fig. 9a, where the dashed curve corresponds to the case for which $V_{ds} = 0$V and the solid curve corresponds to the real case. The shifts in V_T as functions of time are given in Fig. 9b.

Results of the conducted simulations reveal that if the drain biases of the transistors are ignored, the NBTI induced ΔV_T on a 9-inverter ring oscillator is overestimated by 5.4% after five years of operation. If an NBTI induced threshold shift of 20mV limits the life time, then the lifetime is underestimated by 19% when the drain bias is ignored.

C. Effect of Circuit Aging

The effect of aging is analyzed via the simulation loop given in Fig. 6c, where the ΔV_T in the SPICE model is updated when V_T of a device changes more than 1mV. Simulations conducted on a 9-inverter ring oscillator yield that the slight change in the signal shape has an ignorable effect in lifetime estimation. When the shift in the aging parameters are taken into account, the ΔV_T is observed to increase less than 0.1%.

VI. Conclusion

The NBTI induced threshold voltage shift depends on the operating conditions of a circuit and ignoring some of these may yield erroneous lifetime estimation. Based on the charge trap theory, this paper shows that there is more than 10% error in NBTI induced ΔV_T estimation, if the exact wave shape of the V_{gs} signal and the drain bias V_{ds} are not accounted for.

Due to the limitations of the available TCAD simulator, the simulations are conducted for a 100nm technology. Measurements on a state of the art high-k FinFET technology are also analyzed in a simplified flow and the shift in V_T is observed to be an order of magnitude greater. As the technology scales the ratio of ΔV_T to the supply voltage V_{dd} aggressively increases and very precise lifetime estimation techniques are required.

Acknowledgment

This study is supported by the European Union's Seventh Framework Program under the grant agreement number 619234 (MoRV).

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