Reconfigurable Nanowire Transistors with Multiple Independent Gates for Efficient and Programmable Combinational Circuits

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***Abstract*— We present MUX based programmable logic circuits built from newly proposed compact and efficient designs of combinational logic gate. These are enabled by reconfigurable Schottky barrier nanowire transistors with multiple independent gates, which can be dynamically switched between p- and n-type functionality. It will be shown that a single device can be used to replace paths of several transistors in series. This leads to topological differences and increased flexibility in circuit design. We found that especially complex functions, like Majority and Parity gates of many inputs, which are generally avoided in standard CMOS technology, benefit from the new device type. This can be exploited to directly map reconfigurable building blocks, e.g. dynamically switching NAND to NOR. Exemplary 6-functional logic circuits will be shown, which exhibit up to 80% reduction in transistor count, while maintaining the same functionality as compared to the CMOS reference design. Logical effort analysis indicates that 20% less circuit delay and 33% less normalized dynamic power consumption can be achieved.**

Keywords*— *reconfigurable FET, RFET, Schottky FET, polarity-control, logical effort, logic gates, programmable circuit

I. INTRODUCTION

Complementary Metal Oxide Semiconductor (CMOS) Technology is widely dominating today's integrated electronics market. In order to increase the hardware performance, vast progress has been made within the last 50 years in both areas: transistor scaling and circuit architecture. In contrast to these, the design of the main circuit building blocks have not changed ever since the introduction of the CMOS layout by Wanlass in 1967 [1]. Being fast, versatile and energy efficient two-input NAND gates have become the workhorse for logic as well as memory applications.

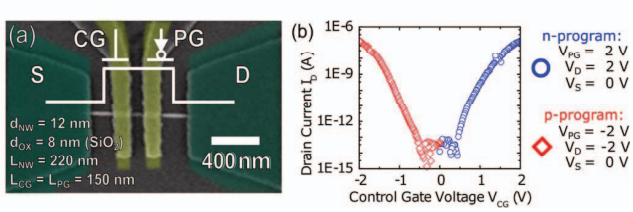

Figure 1. (a) Colored top view SEM image of a fabricated and measured reconfigurable field effect transistor (RFET). The inset shows a symbol used for circuit diagrams with source (S), drain (D), control gate (CG) and program gate (PG) contacts. (b) Measured p- and n-programmed transfer characteristics exhibiting symmetry along V_{CG} = 0 V.

Functions with a high number of inputs, like Majority (MAJ) and Parity gates have been considered to be inefficient and slow.

In this study, we present new designs of combinational logic gates with lower transistor count as well as decreased gate delay compared to classical CMOS implementations. Moreover, those gates can serve as reconfigurable logic blocks for highly adaptive systems. The technology is enabled by reconfigurable Schottky barrier nanowire transistors with multiple independent gates, which are introduced in Section II. We evaluate the design and circuit topology of the proposed logic gates using the method of logical effort in Section III. Based on those gates two efficient reprogrammable logic circuits providing six different functions are introduced in Section IV. We conclude our investigation with some important considerations on area, power consumption and interfacing of the new technology.

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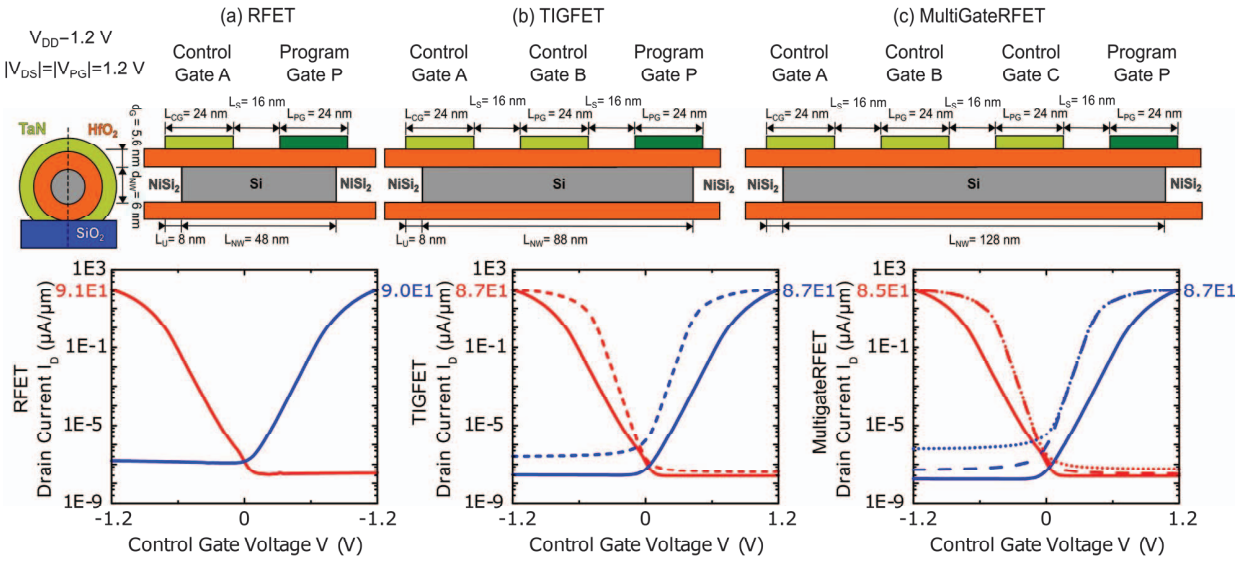

Figure 2. Cross sectional views and TCAD simulation data of an (a) Reconfigurable (R)FET, (b) Three-Independent gate (TIG)FET and (c) Multigate RFET with a layout compatible to each other. In all realizations, the device polarity is adjusted at the program gate directly aligned on top of the drain contact (dark green). The transistors operates either as p-type (red line) or n-tpye (blue line) device. Different numbers of control gates (light green) can be used to turn the device on. Control gate A (straight line) is aligned directly at the Source contact, while Control Gate B (dashed line) and Control gate C (dotted line) are placed in the center of the channel. It is evident, that the current output in the on-state is nearly independent on the channel length, number of gates or which gate actually turns the device on. Details about the simulation setup can be found in Ref. [6].

II. Reconfigurable Nanowire Transistors With Multiple Independent Gates

Recently, various types of silicon nanowire Schottky barrier transistors that enable a dynamically reprogramming between p- and n-function, have been demonstrated [2]–[5]. The functionality is enabled by longitudinal metal-$NiSi_2$ / intrinsic-Si / metal-$NiSi_2$ nanowire heterostructures, controlled by two or more independent gates. One of the most advanced concepts is the symmetrical reconfigurable field effect transistor (RFET) [4], depicted in Figure 1. In this realization two topgates are applied. The gate overlapping the source junction (control gate CG) thereby controls the carrier flow, just like in a standard CMOS device. The additional gate aligned on top of the drain contact (program gate PG), is used to program the transistor by blocking the undesired carrier type. Depending on the voltage scheme the device either exhibits p-type functionality, meaning the current output is high when the input voltage at the CG is low (red squares), or n-type functionality, meaning the current output is high when the applied CG voltage is high (blue circles). Remarkably, both program types thereby deliver the same output current at identical geometry. Therefore truly complementary inverter circuits could be demonstrated from those devices employing a single supply voltage potential [4].

It has been proven by measurements [2], simulations [6], and scanning gate microscopy (SGM) analysis [7] that within a reasonable region the on-current flowing through the device is independent from the channel drift and only determined by the injection at the source sided Schottky barrier. As a consequence the RFET can operate also with an ungated area in the middle of the channel, which is in contrast to classical CMOS devices. This gives the opportunity to add additional independent gates to the structure. As the on-resistance of the device is dominated by the resistance of the source sided barrier the current of the device is nearly not degraded by increasing the channel length [8], as long as a good electrostatic control over the channel potential is maintained. This is illustrated in Figure 2 based on simulation data of three exemplary RFET structures with different number of gates. In addition, the on-current for an individual multigate device is identical no matter if the transistor is steered directly at the source gate (Fig. 2(b) control gate A, straight lines) or at the channel gate (Fig. 2(b) control gate B, dashed lines), although steeper subthreshold slopes can be achieved with the latter operation mechanism. The concept has be experimentally proven by Zhang et al. [5] for devices with three independent gates and can be extended to larger multigate RFETs as shown in this work by the simulations in Figure 2(c).

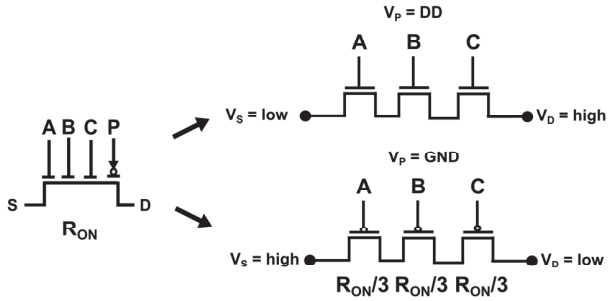

Figure 3. Equivalent circuit of a multigate RFET with four gates. One single transistor resembles three single gated transistors in series. All three transistors are programmed to p- or n-functionality depending on the applied voltage scheme. In addition, they virtually operate with an effective resistance R_{eff} of only 1/3 of the internal resistance of the device.

The transistors thereby only pass a current, if all control gates are in the on-state at the same time. Consequently each multigate RFET can be described by an equivalent circuit consisting of several standard FETs in series (Fig. 3). This equals a wired-AND logic functionality enabled by a single device. Moreover, as the internal resistance is dominated by

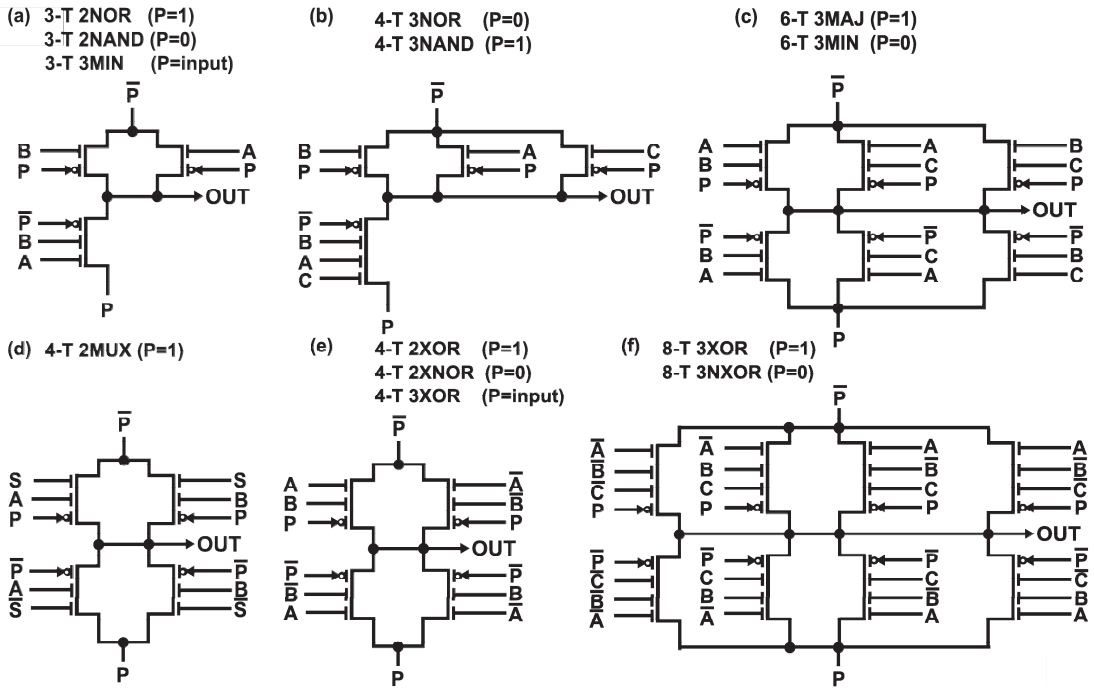

Figure 4. Efficient combinational logic gates built from Multigate RFET technology with (a) 2NAND and 2NOR, (b) 3NAND and 3NOR, (c) 3MIN and 3MAJ (d) inverting 2-way MUX (e) 2XOR and 2XNOR and (f) 3XOR and 3XNOR functionality. In a static case the program signal P is set to GND (0) or DD (1). A dynamic schwitching between both functions can be acheived by altering the program signal. In addition the gates (a) and (e) can be executed in a transmission gate style by applying the program gate as additional input signal to map the 3MIN and 3XOR function, respectively.

the injecting barrier at the source side, each of those equivalent transistors within the wired AND operate with a virtual lower channel resistance R_{EFF} of only R_{ON}/m, where m is the number of control gates and R_{ON} the real on-resistance of the device. This effect can be exploited on the logic gate level to design efficient combinational circuits with reduced delay and transistor count as compared to classical designs.

III. Efficient Combinational Logic Gates

The wired-AND functionality of the multigate RFETs can be used to simplify circuit designs of logic gates. For example, if the two transistors within the serial branch of a standard two-input NAND gate are merged into a single RFET device, a three-transistor (3-T) 2NAND gate is resulting (Fig. 4(a)). The identical structure can be steered as a 2NOR gate, if all signals applied at the program gates (P) are reversed [9], or as a 3-T 3MIN transmission gate, if the program signal is used as third input signal [5]. The same concept can be used to decrease the transistor count of 3NAND, 3NOR 2MUX, 3MAJ, 3MIN, 2XOR and 3XOR designs, exploiting RFETs with up to four independent gates (as shown in Fig. 4 and Table I).

A. Estimation of Gate Delay using Logical Effort Theory

Due to the lack of a compact model for our novel experimental device, we analyzed the delay of the proposed circuits using the logical effort theory as described in [6], [10]. The big advantage of this method is that it delivers technology independent results, which are directly transferable from a micrometer sized lab technology to highly integrated circuits. By reformulation of a simple RC based model, the propagation delay t_{PD} through an arbitrary logic gate can be described by:

$$t_{PD} = \tau D, \tag{1}$$

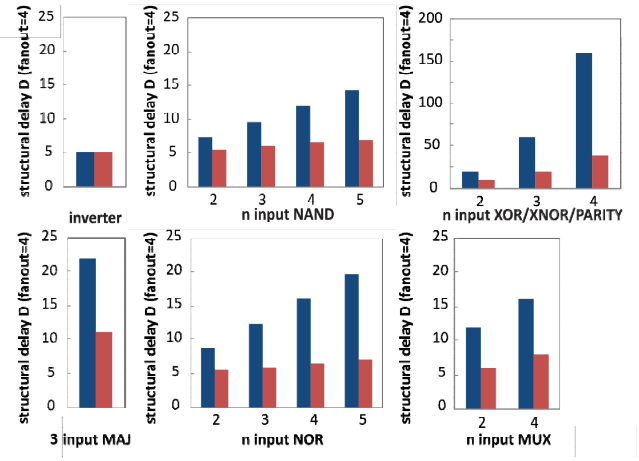

Figure 5. Comparison of structural delay between logic gates in CMOS (blue) and Multigate RFET (red) technology. Delays for gates with more than three inputs are projections, assuming that the individual transistor performance is not altered by this design change. All values are calculated assuming a fanout of 4, using the method of logical effort and are under the constriction that an equal individual device performance can be achieved.

with

$$D = gh + p, \tag{2}$$

where τ is the intrinsic inverter delay, D is the structural delay of the circuit, h is the fanout, p is called parasitic delay and g is called logical effort, which is a direct measure for the logic gates' topological complexity. Calculated values for g and p are given in Table I. It is evident, that due to their lower transistor count, all proposed multigate RFET gates exhibit a reduced logical effort and less parasitic capacitance compared to their CMOS counterparts. This performance increase is a

TABLE I
COMPARISON OF STATIC LOGIC GATE IMPLEMENTATIONS IN MULTIGATE RFET AND CMOS TECHNOLOGY

GATE	TRANSISTOR COUNT #T, LOGICAL EFFORT g, PARASITIC DELAY p	MULTIGATE RFET	CMOS
INVERTER	#T	2	2
	g total	1	1
	p	1	1
2NAND	#T	3	4
	g total	2	8/3
	g per input	1	4/3
	p	3/2	2
2NOR	#T	3	4
	g total	2	10/3
	g per input	1	5/3
	p	3/2	2
2X(N)OR	#T	4	8
	g total	4	8
	g per bundle	2	4
	p	2	4
3NAND	#T	4	6
	g total	3	5
	g per input	1	5/3
	p	2	3
3NOR	#T	4	6
	g total	3	7
	g per input	1	7/3
	p	2	3
3X(N)OR	#T	8	24
	g total	12	36
	g per bundle	4	12
	p	4	12
3MAJ / 3MIN	#T	6	10
	g total	6	12
	g per bundle	2	4
	p	3	6
2MUX	#T	6	12
	g total	4	8
	g per input	1	2
	p	2	4

result out of the virtually lower channel resistance per input. In addition, there is always only a single transistor placed between the output node and the supply potentials. This omits the need for having several nanowires in parallel to speed up the serial branches. As a consequence, several changes in circuit topology become evident here. First of all, NAND and NOR circuits can be built with equal performance, simplifying timing constraints. Secondly, that for the individual inputs all sorts of NAND, NOR and MUX gates have a logical effort value equal to that of an inverter. This connotes, they all have equal driving strength. As a result multigate RFETs provide an increased design flexibility as e.g. all of those gates can be used to buffer a subsequent transmission gate, without an additional delay penalty. In addition, this implies that the use of inverters should be avoided as often as possible in RFET designs. Assuming a fixed fanout of h = 4 for all gates, the normalized circuit delay can be calculated. The results plotted in Fig. 5 show that indeed except for the inverter all combinational circuits perform better if built from multigate RFETs under the assumption that an equal individual device performance can be achieved. Especially MAJ and PAR functions of many inputs, which are avoided in standard CMOS designs, show a largely decreased delay (up to -75%).

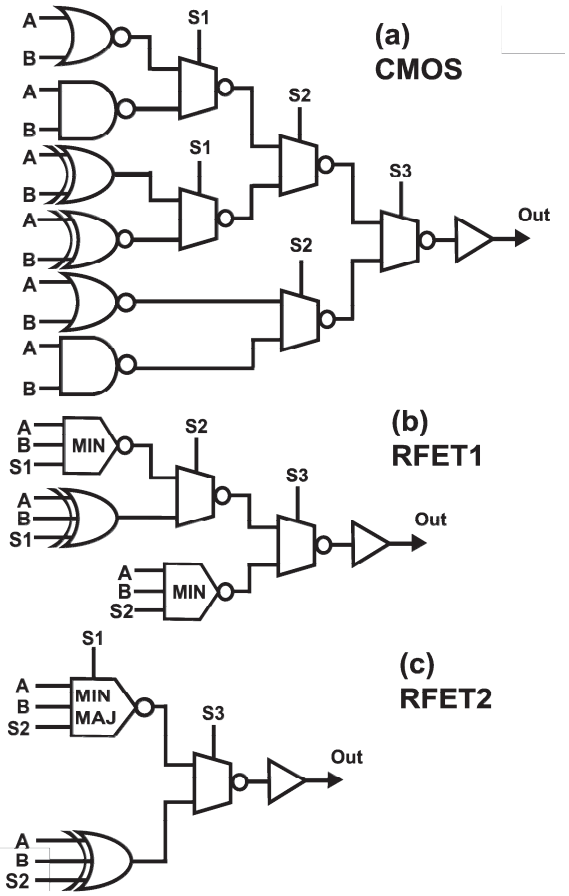

Figure 6. MUX tree-based 6-functional programmable logic circuits providing AND, OR, NAND, NOR, XOR and XNOR function of A and B as selected by the signals S1, S2 and S3. (a) CMOS implementation using 92 transistors. (b) Implemenation with 34 Multigate RFET employing Minority and Parity gates. (c) Implemenation with 26 MultigateRFET employing a reconfigurable MIN/MAJ gate.

However, for an overall delay comparison also the intrinsic inverter delay τ, which is a measure for the performance of the integrated technology, has to be accounted for. For our simulated example structure, the on-current level is still about a factor of four lower than the ITRS requirements, due to the energy barrier in the on-state (90 $\mu A \mu m^{-1}$ vs. 351 $\mu A \mu m^{-1}$ specified in 2012 edition for low-standby-power devices). This can be overcome, if four stacked nanowires are used on top of each other as demonstrated by De Marchi et al. [3]. Another option explored in literature would be to employ low-bandgap semiconductors, such as Germanium [11]. This would not only increase the currents, but also lower the threshold-voltages.

B. Dynamic Reconfigurable Operation

It is evident from the circuit designs in Fig. 4, that most of the proposed gates can fulfill two functions depending on the applied program signal P, e.g. a NAND gate can be reprogrammed to resemble a NOR functionality. This fine-grain reconfiguration can be easily implemented by adding a single input inverter to dynamically route the program signals. The resulting gate can be seen as a buffered three-transistor transmission-gate providing the Minority (MIN) function,

TABLE II
COMPARISON OF MINIMAL PATH DELAYS D_{MIN} OF THE PROGRAMMABLE LOGIC CIRCUITS SHOWN IN FIG. 6
DELAYS OF THE CRITICAL PATHS DETERMINING THE OVERALL CIRCUIT SPEED ARE MARKED BOLD

	(A) CMOS DESIGN		(B) MULTIGATE RFET 1	(C) MULTIGATE RFET 2
SIGNAL/FUNCTION	PATH DELAY D_{MIN} (C_{OUT}=32, FANOUT=1)	PATH DELAY D_{MIN} (C_{OUT}=128, FANOUT=4)	PATH DELAY D_{MIN} (C_{OUT}=32, FANOUT =4)	PATH DELAY D_{MIN} (C_{OUT}=32, FANOUT=4)
$A/B_{NAND/NOR}$	21.5 / 22.1	26.1 / 27.0	**21.5**	18.5
$A/B_{AND/OR}$	19.7 / 20.5	25.5 / 26.7	21.1	21.1
$A/B_{XOR/XNOR}$	**22.7**	27.0	20.3	19.0
S1	16.8	21.7	20.1	18.5
S2	15.2	22.0	20.7	**22.7**
S3	15.4	**28.5**	14.3	14.3

which is a combination of NAND and NOR. As a tradeoff for the increased functionality the logical effort values for the logical signals A and B double, due to the fact that there is an additional transistor placed between the supply potential and the output node. The novel gates can be used as ultra-fine grain building blocks for highly adaptive systems.

IV. PROGRAMMABLE LOGIC CELL DESIGN

A number of fine-grain reconfigurable cells, built on either carbon nanotubes or silicon nanowires have been proposed within the last years, exploiting fine-grain reconfigurability. Up to 8 functions could be realized with as little as 10 transistors [12], [13]. However, the need for having two independent clocking signals, to precharge the dynamic logic stages used to design these cells, heavily limited their applicability. Here, we propose a different strategy to employ fine-grain reconfigurable transistors in programmable logic circuits. By simply replacing key elements in a static MUX tree not only a lot of transistors can be saved, but also the circuit level performance in terms of delay and power consumption can be improved. This is exemplarily shown by a 6-functional circuit design providing the AND, OR, NAND, NOR, XOR or XNOR function of two inputs depicted in Fig. 6. It is evident, that a pair of NAND and NOR gates and the respective multiplexer can be merged into a single 3MIN transmission gate. Similar, the branch containing the XOR and XNOR function can be merged to a single 3-input XOR or Parity gate. In addition, the usually used inverter-buffered transmission gate multiplexers (10 transistors in total) can be replaced by the efficient static RFET multiplexer depicted in Fig. 4(d). As a result the overall transistor count is reduced by 63%. An even more compact implementation is possible, if AND, OR, NAND, and NOR functionality are all provided by the reconfigurable MIN/MAJ gate depicted in Fig. 4(c), employing P and C as individual select signals. Doing so, the transistor count is further reduced down to only 26 devices (28% of the respective CMOS implementation). Also notice, that the overall circuit remain fully static by this optimization.

A. Critical Delay Estimation

The method of logical effort can be also applied to networks of logic stages [10]. One of the key predictions of logical effort is that the minimum possible structural delay D_{MIN} of a given logical path can be expressed as:

$$D_{MIN} = N(h\prod g_i b_i)^{\frac{1}{N}} + \sum p_i, \qquad (3)$$

where N is the number of stages within the path, g_i and p_i are the logical effort and parasitic delay values of the individual stages, respectively. h is the fanout C_{OUT}/C_{IN} of the whole path and $b_i=C_{TOT}/C_{PATH}$ the branching effort of each stage, where C_{TOT} and C_{PATH} are the total and on-path capacitances at the output of each stage, respectively. Although the real delay might be slightly higher, depending on the distribution of capacitances along the path, it can be proven theoretically that the resulting D_{MIN} is within 15% of the real minimum [10]. The critical delay of the whole circuit is determined by the delay of the slowest individual path for a given fanout or load capacitance. For the analysis of our exemplary programmable circuit designs, we chose an output capacitance of 32 (normalized to the input capacitance of a single transistor gate). For both RFET implementations this equals a fanout of 4 with respect to the input capacitance of signal A. The results of the calculations are given in Table II. First of all, it is evident, that the individual path delays within the RFET design are quite evenly distributed between each path, which is highly desired for a fast circuit design. Also, due to the employment of the reconfigurable gates, the fanin of the multigate RFET circuits is much lower than that of its CMOS counterpart. As a result, the CMOS gate driving the same capacitance shows a similar delay, but at decreased fanout. Comparing the critical path delays to that of a CMOS design with identical fanout, a 25% (20%) reduction in delay is achieved with the multigate RFETs cells, respectively. Similar to the results of the individual gates, this is under the assumption that an identical individual device performance can be achieved.

B. Area, Power Consumption and Interfacing

Although the footprint of the individual devices is larger compared to that of a single gated reference transistor it becomes evident from the exemplary programmable logic circuit that a high amount of transistors can be saved using the multigate technology. In addition, it has to be considered that the RFET technology does not require any doping, well implantation, or shallow trench isolation (STI), reducing the overall area on chip needed. Also, the circuit designer has therefore more degrees of freedom concerning the layout. Conversely, smart power routing schemes have to be found to deal with the overhead of inputs and signals per device [14]. Typically, the measure $C \cdot V_{DD}^2$ is given as an indicator for the dynamic power consumption of a certain technology, where C is the input capacitance of an NMOS transistor and V_{DD} the supply voltage. On the transistor level multigate RFETs can be assumed to show increased dynamic power dissipation compared to CMOS, as a higher supply voltage is needed to overcome the energy barrier in the on-state of the device.

TABLE III
TRANSISTOR COUNT #T, NORMALIZED DYNAMIC AND STATIC GATE CAPACITANCES C_{DYN} AND C_{STAT}, INTERNODAL CAPACITANCES C_{INT} AND DYNAMIC POWER PRODUCT $\Sigma C \cdot V_{DD}^2$ AS INDICATORS FOR AREA AND POWER CONSUMPTION OF THE PROGRAMMABLE LOGIC CIRCUITS SHOWN IN FIG. 6

	(A) CMOS DESIGN	(B) MULTIGATE RFET 1	(C) MULTIGATE RFET 2
#T	92	34	26
C_{DYN}	92	54	46
C_{STAT}	0	24	16
C_{INT}	22	6	4
V_{DD}	1	1.2	1.2
$\Sigma C \cdot V_{DD}^2$	114	111	79

However, a largely decreased amount of input capacitances are needed on the gate or system level to map the same functionality. In addition, there are less internodal capacitances to be charged, as there is always only a single transistor placed between the supply potentials and the output node. On the other hand, RFET technology needs some additional static programmed gates. A simple indicator for the dynamic power consumption of the proposed circuits can be given if all dynamic, static and, intermodal capacitances are summed up and multiplied with the technology typical supply voltage V_{DD}. The results, assuming 1 V for CMOS and 1.2 V for RFET technology, are shown in Table III. A reduction of up to 33% in dynamic power dissipation is indicated for the MIN/MAJ based RFET design, albeit the higher voltage level. Note that this result is also normalized to the capacitance value of a single device, which might differ between a RFET and CMOS technology of the same size. However, one should note that also the loss in static power dissipation is expected to be much lower in RFETs compared to classical MOSFETs, due to the direct blocking of reverse junction leakage at the drain contact. E.g. in our simulated example structure shown in Figure 3, the leakage current level is still orders of magnitude below the requirements specified in the ITRS for low-standby-power devices, making the technology promising for ultra-low-power applications.

Finally, being a charge based and complementary operating technology interfacing RFETs with CMOS is rather simple, as a standard periphery can be used for adjusting the required supply voltages. Even more important, the beauty of being a doping-free technology is that RFET integration does not require any high-temperature process steps. This provides the possibility to directly implement them into the back-end of a CMOS chip, thus making use of their enhanced functionality.

V. CONCLUSION

In this study, we have presented new compact and efficient designs of combinational logic gates. These are enabled by reconfigurable Schottky barrier nanowire transistors with multiple independent gates, which can be used to replace arrangements of multiple transistors in series. This leads to several differences in circuit topology, e.g. NAND, NOR and MUX all provide inverter drive capability. We found that especially complex gates, like Majority and Parity benefit from the new device type. We have shown on the example of 6-functional MUX tree-based programmable logic circuits how these gates can be exploited to improve adaptive circuit designs. Our analysis, applying the method of logical effort, indicated that a static 6-functional programmable circuit built from only 26 devices can exhibit up to 20% less circuit delay and 33% less dynamic power consumption than the CMOS reference design, while maintaining the same functionality.

REFERENCES

[1] Wanlass, Frank M, "Low stand-by power complementary field effect circuitry," U.S. Patent No. 3,356,858, 05-Dec-1967.

[2] A. Heinzig, S. Slesazeck, F. Kreupl, T. Mikolajick, and W. M. Weber, "Reconfigurable Silicon Nanowire Transistors," *Nano Lett.*, vol. 12, no. 1, pp. 119–124, Jan. 2012.

[3] M. De Marchi, D. Sacchetto, S. Frache, J. Zhang, P. Gaillardon, Y. Leblebici, and G. De Micheli, "Polarity control in double-gate, gate-all-around vertically stacked silicon nanowire FETs," in *Electron Devices Meeting (IEDM), 2012 IEEE International*, 2012, pp. 8.4.1

[4] A. Heinzig, T. Mikolajick, J. Trommer, D. Grimm, and W. M. Weber, "Dually Active Silicon Nanowire Transistors and Circuits with Equal Electron and Hole Transport," *Nano Lett.*, vol. 13, pp. 4176 Sep. 2013.

[5] J. Zhang, M. De Marchi, D. Sacchetto, P.-E. Gaillardon, Y. Leblebici, and G. De Micheli, "Polarity-Controllable Silicon Nanowire Transistors With Dual Threshold Voltages," *IEEE Transactions on Electron Devices*, vol. 61, no. 11, pp. 3654–3660, Nov. 2014.

[6] J. Trommer, A. Heinzig, T. Baldauf, S. Slesazeck, T. Mikolajick, and W. M. Weber, "Functionality-Enhanced Logic Gate Design Enabled by Symmetrical Reconfigurable Field Effect Transistors," *Transactions on Nanotechnology IEEE*, vol. 4, 2015.

[7] D. Martin, A. Heinzig, M. Grube, L. Geelhaar, T. Mikolajick, H. Riechert, and W. M. Weber, "Direct Probing of Schottky Barriers in Si Nanowire Schottky Barrier Field Effect Transistors," *Phys. Rev. Lett.*, vol. 107, no. 21, p. 216807, Nov. 2011.

[8] W. M. Weber, A. P. Graham, G. S. Duesberg, M. Liebau, C. Cheze, L. Geelhaar, E. Unger, W. Pamler, W. Hoenlein, H. Riechert, F. Kreupl, and P. Lugli, "Non-Linear Gate Length Dependence of On-Current in Si-Nanowire FETs," in *Solid-State Device Research Conference, 2006. ESSDERC 2006. Proceeding of the 36th European*, 2006, pp. 423–426.

[9] J. Trommer, A. Heinzig, S. Slesazeck, T. Mikolajick, and W. M. Weber, "Elementary Aspects for Circuit Implementation of Reconfigurable Nanowire Transistors," *IEEE Electron Device Letters*, vol. 35, no. 1, pp. 141–143, Jan. 2014.

[10] I. E. Sutherland, R. F. Sproull, and D. F. Harris, *Logical Effort: Designing Fast CMOS Circuits*. Morgan Kaufmann, 1999.

[11] J. Trommer, A. Heinzig, A. Heinrich, P. Jordan, M. Grube, S. Slesazeck, T. Mikolajick, and W. M. Weber, "Material Prospects of Reconfigurable Transistor (RFETs) – From Silicon to Germanium Nanowires," *MRS Online Proceedings Library*, vol. 1659, pp. 225 2014.

[12] I. O'Connor, L. Junchen, F. Gaffiot, F. Pregaldiny, C. Lallement, C. Maneux, J. Goguet, S. Fregonese, T. Zimmer, L. Anghel, T.-T. Dang, and R. Leveugle, "CNTFET Modeling and Reconfigurable Logic-Circuit Design," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 11, pp. 2365–2379, Nov. 2007.

[13] P.-E. Gaillardon, X. Tang, G. Kim, and G. De Micheli, "A Novel FPGA Architecture based on Ultra-Fine Grain Reconfigurable Logic Cells," *IEEE Transactions on Very Large Scale Integration Systems*, 2014.

[14] O. Zografos, P.-E. Gaillardon, and G. De Micheli, "Novel grid-based power routing scheme for regular controllable-polarity FET arrangements," in *2014 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2014, pp. 1416–1419.