Inverters' Self-Checking Monitors for Reliable Photovoltaic Systems

M. Omaña A. Fiore C. Metra
DEI, University of Bologna
Bologna, Italy
{martin.omana; alessandro.fiore; cecilia.metra}@unibo.it

***Abstract*—Photovoltaic systems are a widespread form of green energy, that is becoming increasingly considered also as a form of economical investment. Their reliability is consequently becoming a concern. In this paper we focus on the reliability of the DC-AC converters (inverters) of photovoltaic (PV) systems. We analyze the effects of the faults likely to affect their operation in the field. We show that such faults can impact catastrophically the power delivered to the load. We then propose a self-checking monitor, that is able to detect the occurrence of such faults in the field, as well as faults possibly affecting itself. Our monitor can therefore be adopted to guarantee the concurrent on-line test of faults affecting the inverters of PV systems. Moreover, if used together with suitable recovery strategies, for instance based on proper hardware reconfiguration, it can provide PV systems with fault tolerance ability, thus meeting the increasing demand for reliable PV systems.**

Keywords – Photovoltaic Systems; Inverters; Self-Checking; Fault Tolerance; Reliability

I. INTRODUCTION

Photovoltaic (PV) systems are a widespread source of green energy [1, 2]. Recently, they have also become a form of economical investment, thus making their reliability a concern.

Generally, PV systems consist of two main blocks: the PV array, that converts the sun energy into a continuous (DC) voltage, and the DC-AC converter (inverter), that converts such a produced DC voltage into an alternate (AC) voltage to be delivered to the load, usually the power grid [1, 3].

As shown in recent studies [4, 5, 6, 7], the most critical part of PV systems from the reliability point of view is (are) the inverter(s). In fact, although faults may on principle affect both the PV array and the inverter(s), it has been reported that current PV arrays guarantee a lifetime well beyond 20 years (which is the lifetime limit considered by the industry of PV systems), while the estimated life-time of the inverter(s) is shorter than 10-15 years [2, 5, 7].

Faults possibly affecting PV arrays and inverters in the field have been identified in [5, 7]. It has been shown that the failure rate of MOS transistors and diodes of the inverter is considerably higher than the failure rate of the PV array and the other components of the inverter. However, the impact of such faults on the in-field operation of PV systems, particularly on their power efficiency, has not been evaluated.

More recently, in [8] a preliminary analysis has shown that faults affecting some transistors/diodes composing the inverters of PV systems may produce a catastrophic effect on the power delivered to the load, thus on the efficiency of the whole PV system. However, the effects of all other possible inverter faults, such as faults affecting the inverter control circuitry, have not been evaluated. Always in [8], a monitor circuit able to detect the considered faults affecting the transistors/diodes of the inverter has been presented. However, such a monitor is not able to detect its possible internal faults, which might compromise its effectiveness.

Based on these considerations, in this paper we extend the fault analysis in [8], by including also faults possibly affecting the control circuitry of the inverter. We will show that such faults can produce a catastrophic effect on the power delivered to the load (*e.g.*, a reduction up to the 80%).

We then propose a monitoring circuit able to detect the occurrence of faults affecting the inverter (included its control circuitry). The proposed monitor is self-checking with respect to faults possibly affecting itself, thus avoiding that their occurrence in the field can compromise its effectiveness. Such a monitor can therefore be adopted to guarantee the concurrent on-line test of faults affecting the inverter of PV systems, despite the possible occurrence of faults affecting itself. Moreover, if used together with suitable recovery strategies, for instance based on proper hardware reconfiguration, our monitor can provide PV systems with fault tolerance ability, thus meeting the increasing demand for reliable PV systems.

The rest of the paper is organized as follows. In Section II, we introduce the considered PV system and inverter. In Section III, we analyze the impact of faults possibly affecting the inverter on the power delivered to the load. In Section IV, we propose a monitoring circuit able to detect concurrently the faults likely to affect the inverter, as well as faults affecting itself. In section V, we describe a possible design of our monitor and we prove its effectiveness. In section VI, we analyze its self-checking ability with respect to possible internal faults, and we evaluate its power cost. Finally, we draw some conclusive remarks in Section VII.

II. CONSIDERED PV SYSTEM

Fig. 1 schematically shows a general PV system, consisting of a PV array and an inverter, transforming the DC voltage generated by the PV array (V_{PV}) into an AC voltage (V_{OUT}) suitable to be delivered to the load (*e.g.*, the power grid). As known [3], other PV systems exist, which employ a higher

978-3-9815370-6-2/DATE16/©2016 EDAA

number of inverters. For simplicity, we will hereinafter refer to the scheme in Fig. 1, but our analyses and solution apply to PV systems with more inverters as well.

The power grid can be realistically modelled as an L-R low-pass filter, for example with a cutoff frequency of 50Hz [3, 9], $L=100\mu H$ and $R=0.1\Omega$. Moreover, we consider the realistic case of a PV array composed by series of 18 PV cells, each one modeled as in [5, 3]. For simplicity, we will hereinafter assume the simple case of a single series. However, our analyses can be straightforwardly extended to the more realistic case of several parallel series of 18 PV cells.

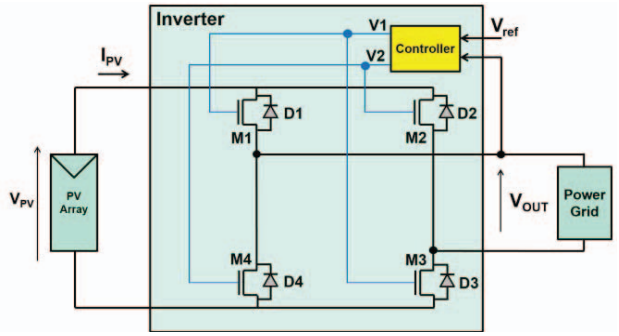

Fig. 1. Schematic representation of a PV system with a single inverter implemented by a H-bridge.

As a realistic example, we consider the inverter implemented by a H-bridge (Fig. 1). It consists of four MOS transistors (M1-M4), and four safety diodes (D1-D4) connected in parallel to transistors M1-M4, respectively, to prevent possible high voltage spikes from damaging the transistors.

The Controller of the inverter is a sinusoidal pulse-width modulation circuit [9, 10]. It generates the control signal *V1 (V2)* for the transistors' couple M1-M3 (M2-M4). *V1* and *V2* are complemented periodic signals, with a fixed period $T_S = 1/f_S$. As a realistic example, we consider $f_S = 2.5kHz$. The controller compares the external reference voltage (V_{ref}) with the output of the inverter (V_{OUT}). Based on such a comparison, the controller adjusts the time interval (within each T_S) during which M1-M3 and M4-M2 are conductive, so that V_{OUT} follows V_{ref} [9, 10]. As an example (typical for PV systems employed in Europe), we assume that V_{ref} is a 50Hz sinusoidal wave.

III. Effects of Faults Affecting the Inverter

We have considered all faults that have been found likely to affect an inverter in the field [5, 7]. They are:

- shorts between the drain and source terminals of the MOS transistors (*i.e.*, faults equivalent to transistor stuck-ons);
- opens on the gate terminal of the MOS transistors (*i.e.*, faults equivalent to transistor stuck-opens);
- shorts between the two terminals of diodes (*i.e.*, faults equivalent to diode stuck-ons);
- opens between the two terminals of diodes (*i.e.*, faults equivalent to diode stuck-opens).

We have considered such faults as possibly affecting the MOS transistors and diodes of the H-bridge, as well as the MOS transistors of the Controller. We have analyzed their effects on the steady-state operation of the inverter in the field, particularly on the power delivered to the load, as well as on the harmonic components of the current that the inverter absorbs from the PV array (I_{PV} in Fig. 1). We have not considered the initial short setting phase of the inverter, since during this time interval the inverter is not connected to the load [11]. To evaluate the faults' effects, we have performed electrical level simulations by HSPICE of the considered inverter (Fig. 1) with shorts emulated by a very small resistance (1mΩ), and opens by a very large resistance (10MΩ). We have not considered faults affecting the capacitors and inductors of the Controller since their likelihood has been proven to be much smaller than that of the faults listed above [5]. As usual for concurrent fault detection, we have assumed that faults occur one at a time in the field [12].

We have found that, but for the opens on diodes D1-D4, all considered faults reduce significantly the power that the inverter delivers to the load.

The achieved results are summarized in Fig. 2. It shows the relative reduction in the power delivered to the load by the faulty inverter, with respect to the fault-free case (*i.e.*, $\Delta P_O(\%)=100[(P_{O\text{-}fault\text{-}free} - P_{O\text{-}faulty}) / P_{O\text{-}fault\text{-}free}]$). In particular, faults possibly affecting the Controller have been grouped in *faults of kind 1* and *faults of kind 2*, where *faults of kind 1* (*faults of kind 2*) consist of the Controller faults that have been verified making *V1* or *V2* behave as if stuck-at 1 (stuck-at 0).

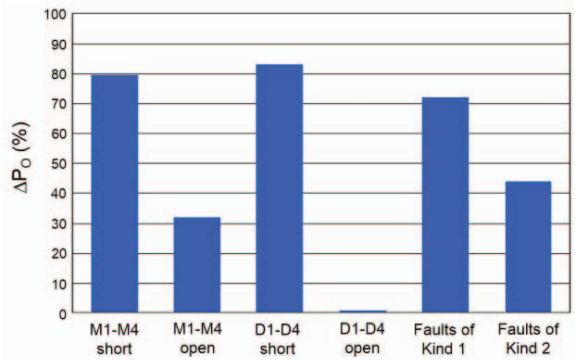

Fig. 2. Relative reduction in the power delivered to the load by a faulty inverter over the fault-free case.

From Fig. 2 we can observe that the power delivered by the faulty inverter drops approximately by:

- the 80%, for shorts affecting transistors M1-M4, or diodes D1-D4;
- the 30%, for opens affecting transistors M1-M4;
- the 70%, for *faults of kind 1* (*i.e.*, Controller faults making *V1* or *V2* behave as if stuck-at 1);
- the 40%, for *faults of kind 2* (*i.e.*, Controller faults making *V1* or *V2* behave as if stuck-at 0).

We have also analyzed the effects of the considered faults on the harmonic components of the current absorbed by the

inverter from the PV array (I_{PV}). We have verified that, but for the faults that do not impact the power delivered by the inverter (*i.e.*, opens on D1-D4), all other faults increase significantly the amplitude of the I_{PV} harmonic component at 50Hz.

As an example, Figs. 3(b) and 3(c) report the harmonics of I_{PV} for the case of a fault affecting the Controller making *V1* behave as if stuck-at 1 and as if stuck-at 0, respectively, while Fig. 3(a) shows the harmonic components of I_{PV} in the fault-free case. We can notice that, in the fault-free case, I_{PV} presents harmonic components with non-negligible amplitude at 50 and 100Hz, and at several frequencies that are multiples of f_S.

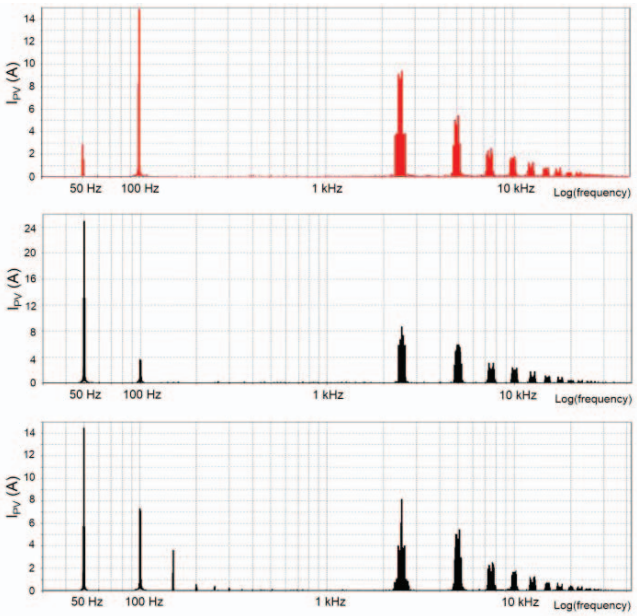

Fig. 3. Harmonic components of the current absorbed by the inverter from the PV array (I_{PV}) for the case of: (a) fault-free inverter; (b) Controller of the inverter affected by a fault making V1 behave as if stuck-at 1; (c) Controller of the inverter affected by a fault making V1 behave as if stuck-at 0.

By comparing Fig. 3(a) with Figs. 3(b) and (c), we can notice that the amplitude of the harmonic component at 50Hz is considerably higher in the faulty case, than in the fault-free case (*i.e.*, we have verified that in the worst case it is approximately 4 times higher in the faulty cases). Additionally, differently from the fault-free case, in the faulty circuit the amplitude of the harmonic component at 50Hz is much higher than that of the harmonic component at 100Hz.

Finally, as discussed in [13, 14], faults affecting the PV array may reduce the value of the DC voltage produced by the array, but do not distort the harmonics of I_{PV}. Therefore, distortions in the I_{PV} harmonic cannot be due to faults affecting the PV array.

IV. Inverter Monitor for Concurrent Fault Detection

Based on the results of our analyses, we propose a monitor able to detect faults affecting the inverter and the monitor itself, during the inverter steady-state operation in the field.

A. Proposed Monitor: Basic Idea

The basic idea behind our monitor is to detect the distortion of the harmonics of the current absorbed by the faulty inverter. As shown in Section III, the amplitude of the 50Hz harmonic of I_{PV} increases significantly in the presence of faults reducing the power delivered by the inverter. Therefore, such faults could be detected by comparing the amplitude of the 50Hz harmonic of I_{PV} with a proper threshold value. Fig. 4 shows the schematic representation of a monitor based on such an idea.

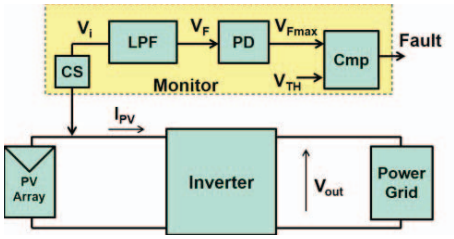

Fig. 4. Schematic representation of a possible monitor to detect faults affecting the inverter.

It employs a current sensor (CS) to measure the current I_{PV}. The CS produces a voltage V_i proportional to I_{PV}, and thus the amplitude of the harmonics of V_i will be proportional to that of the harmonics of I_{PV} at the same frequency. Then, a low pass filter (LPF), with a cutoff frequency of 50Hz, is adopted to filter out the harmonics of V_i at frequencies higher than 50Hz. For frequencies lower than 50Hz, the only harmonic component of V_i with non-negligible amplitude is the one at 50Hz, so that the amplitude of the signal at the LPF output (V_F) will be the amplitude of the V_i harmonic at 50Hz. By simply connecting a peak detector (PD) to the output of LPF, we obtain the maximum value of V_F (V_{Fmax}), which is the amplitude of the V_i harmonic at 50Hz. As shown in the previous Section, for a faulty inverter, the harmonic at 50Hz of I_{PV} has an amplitude approximately 4 times higher than that for a fault-free inverter. Thus, for a faulty inverter, also the value of V_{Fmax} will be approximately 4 times higher than that for a fault-free inverter. Therefore, to identify whether an inverter is faulty or not, we could simply compare V_{Fmax} with a proper threshold (V_{TH}) by means of a comparator (Cmp). Cmp would generate a signal "Fault" assuming: a high logic value, if the inverter is faulty (*i.e.*, if $V_{Fmax}>V_{TH}$); 2) a low logic value, if the inverter is fault-free (*i.e.*, if $V_{Fmax}<V_{TH}$). The value of V_{TH} should be chosen to fall between the amplitude of the 50Hz harmonic of V_i in the faulty and in the fault-free case, which could be determined by means of simulations of a faulty and a fault-free inverter, respectively.

Since, as previously stated, our monitor is intended to detect faults affecting the steady-state operation of the inverter (*i.e.*, when the inverter can deliver power to the load), the output values produced by our monitor prior to the inverter steady-state operation should be discarded, or the monitor should be enabled during the inverter steady-state operation only, by adding a proper enable signal to the scheme presented in Fig. 4.

However, it can be noted that the occurrence of a simple

stuck-at 0 fault affecting signal "Fault" could compromise the effectiveness of a monitor of the kind in Fig. 4, making it unable to detect faults affecting the inverter. This may be the case also for other faults affecting the monitor in Fig. 4. To address this issue, a self-checking monitor is proposed that, although based on the idea presented above, is able to detect the occurrence of faults not only affecting the inverter, but also faults affecting itself. Such a monitor guarantees the concurrent on-line test of faults affecting either itself, or the inverter.

B. *Proposed Self-Checking Monitor*

Based on the idea described above, we propose a self-checking monitor, whose schematic representation is shown in Fig. 5. It consists of two sub-blocks (SB1 and SB2), each one equal to the scheme in Fig. 4, but for the LPF filter that is now substituted by a LPF/HPF filter that can act as either low pass filter (LPF) or high pass filter (HPF), depending on the value of a clock signal *CK*. The cutoff frequency of both the LPF and the HPF implemented by LPF/HPF is 50Hz. When *CK=1,* the LPF/HPF of SB1 (SB2) behaves as LPF (HPF), while when *CK=0* (that is when *CK'=1)*, the LPF/HPF of SB1 (SB2) behaves as HPF (LPF).

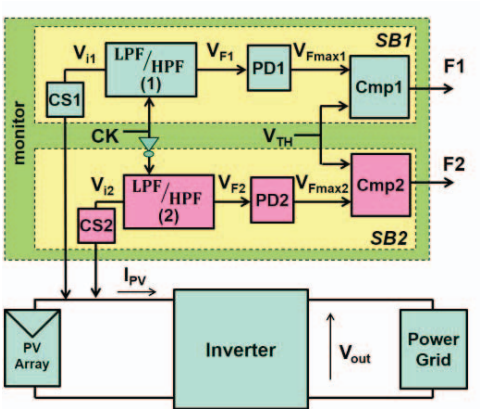

Fig. 5. Schematic representation of our proposed self-checking monitor, able to detect faults affecting the inverter, as well as its possible internal faults.

This way, if the inverter is fault-free, the peak voltage produced by the LPF/HPF acting as LPF (*i.e.*, that within SB1, if *CK=1*, or that within SB2, if *CK=0*) will be lower than the threshold voltage V_{TH} (chosen as described in the previous subsection). Thus, the comparator of the sub-block associated with the LPF/HPF acting as LPF (*i.e.*, Cmp1 of SB1 if *CK=1*, or Cmp2 of SB2 if *CK=0*) will give a low logic value to its output. Meanwhile, the peak voltage produced by the LPF/HPF acting as HPF will be higher than V_{TH}, since as shown in Fig. 3 the current I_{PV} (and thus the voltages $V_{i1,2}$) presents several harmonics of non-negligible amplitude at frequencies higher than 50Hz. Thus, the comparator of the other sub-block will give a high logic value to its output. Therefore, for a fault-free inverter, our monitor will give to its outputs (*F1*, *F2)* alternating and complementary logic values (i.e., (*F1*, *F2*) = (1, 0) or (0, 1)).

Instead, when the inverter is affected by a fault, the amplitude of the signal at the output of the LPF/HPF acting as LPF will be higher than V_{TH} (since, as discussed in the previous subsection, in the faulty inverter the amplitude of the 50Hz harmonic of I_{PV}, and consequently $V_{i1,2}$, increases significantly). Consequently, the comparator downstream the LPF/HPF acting as LPF will give a high logic value to its output. Simultaneously, the amplitude of the signal at the output of the LPF/HPF acting as HPF will be higher than V_{TH}. Therefore, the comparator downstream the LPF/HPF acting as HPF will also give a high logic value to the output. Therefore, in case of faults affecting the inverter, both outputs of our monitor will present a high logic value (*F1*, *F2*) = (1, 1).

As will be discussed in Section VI, when an internal fault affects our monitor, the outputs *F1* and *F2* will both be = 1 or 0 (i.e., (*F1*, *F2*) = (1, 1) or (0, 0)) for a semi-period of *CK* signal.

Therefore, (*F1*, *F2*) = (1, 1) or (0, 0) at the outputs of our monitor will reveal the presence of a fault affecting either the inverter, or the monitor itself, while (*F1*, *F2*) = (1, 0) or (0, 1) will indicate correct operation of both the inverter and our monitor.

V. Monitor Design and Verification

We have designed our monitor considering, as an example, the following discrete components: the operational amplifiers LT1012 in [15]; the CD4069UB NOTs in [16]; and the CD4030B EXORs in [16].

As for the current sensors CS1,2 (Fig. 5), they have been implemented by means of Hall effect current sensors of the kind in [17]. Each sensor measures indirectly the current absorbed by the inverter by measuring its associated magnetic field [17]. Then, the sensors give to their outputs a voltage $V_{i1} = V_{i2} = k*I_{PV}$, where k is the equivalent transresistance of the Hall Effect current sensors.

As for the LPF/HPF blocks of SB1 and SB2 (Fig. 5), we have implemented them as shown in Fig. 6(a). In particular, when *X=1* (*X=0*), the circuit in Fig. 6(a) implements a Sallen-Key second order LPF (HPF), as shown in Fig. 6(b) (Fig. 6(c)). We connect signal *X* of the LPF/HPF of SB1 (SB2) to *CK* (*CK'*). This way, when *CK=1*, the LPF/HPF of SB1 (SB2) implements a LPF (HPF) while, when *CK=0*, the LPF/HPF of SB1 (SB2) implements a HPF (LPF). As an example, we have considered a *CK* frequency of 30Hz.

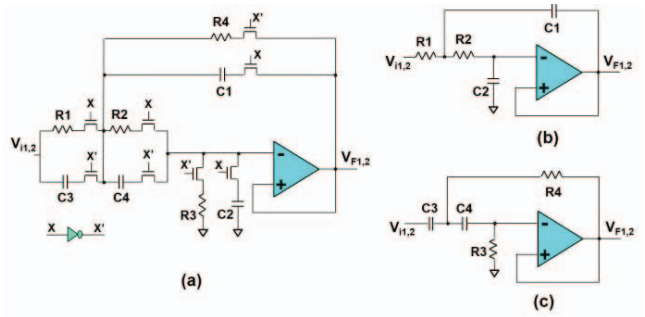

Fig. 6. Implementation of (a) the LPB/HPF block of our monitor in Fig. 5; (b) the resulting Sallen-Key second order LPF when signal *X* in the LFP/HPF block is = 1; (c) the resulting Sallen-Key second order HPF when signal *X* in the LFP/HPF block is = 0.

To obtain a LPF with cutoff frequency at 50Hz, we have considered $R1 = R2 = 10K\Omega$, $C1 = 1\mu F$, and $C2 = 423nF$. Instead, to obtain a HPF with a cutoff frequency at 50Hz, we have considered $R3 = 27k\Omega$, $R4 = 375\Omega$, and $C3 = C4 = 0.47\mu F$. Moreover, since the voltages V_{i1} and V_{i2} (at the outputs of the current sensors CS1 and CS2, respectively) present a maximum voltage value of approximately 3V, we have powered the operational amplifiers with a voltage of ±5V.

As for the peak detectors (PD1,2) and comparators (Cmp1,2), they have been implemented as shown in Fig. 7.

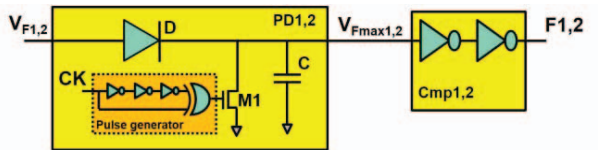

Fig. 7. Implementation of the peak detector and comparator of our proposed monitor.

As stated before, each PD (PD1 and PD2) gives to its output (connected to a capacitor C=1μF) a voltage value equal to the maximum voltage value of the output signal of the LPF/HPF block. The transistor M1 and the block "pulse generator" allow to discharge the capacitor C after each rising/falling edge of *CK* (to reset PD at every CK semi-cycle).

Moreover, as stated before, we can choose the threshold voltage V_{TH} by evaluating the maximum voltage values of the output signal of LPF (which is proportional to the amplitude of the 50Hz harmonic of I_{PV}) in the fault-free case, and in the faulty case respectively. From the performed simulations, we have verified that, when the inverter is fault-free, the LFP/HPF acting as LPF produces an output signal with a maximum voltage value of approximately 0.95V. On the other hand, when the inverter is faulty, the LFP/HPF acting as LPF gives an output signal with a maximum voltage value of approximately 3.5V. Therefore, the maximum voltage values given at the output of LPF change from 0.95V (in the fault-free case) to 3.5V (in the faulty case). We can consequently choose V_{TH} to be equal to 2.5V, which is half the voltage value of the considered power supply voltage. This way, as shown in Fig. 7, we can simply implement the comparators Cmp1,2 by a cascade of two symmetric NOTs (we use two NOTs to avoid signal inversions), whose logic threshold (V_{LT}) is equal to 2.5V.

We have verified the described behavior of our monitor by means of electrical level simulations performed by HSPICE.

We have emulated each possible short/open affecting the inverter as described in Section III. As usual to concurrent fault detection, we have assumed that faults occur one at a time [12].

As an example, Fig. 8 shows the V_{OUT} produced by the inverter, together with signals *F1* and *F2* given to the output of our proposed monitor when: i) the inverter is fault-free (before time *t1*); ii) the Controller of the inverter is affected by a fault making *V1* behave as if stuck-at 0 (after time *t1*).

We can observe that, as expected, before the fault occurrence at time *t1*, the outputs of our monitor (*F1*, *F2*) alternate from (1,0) to (0,1), with a frequency equal to that of signal *CK*, thus indicating a fault-free condition. Instead, after time *t1*, due to the presence of the fault, V_{OUT} is distorted and (*F1, F2*) = (1,1), thus correctly indicating the presence of the fault. We have verified that our proposed monitor behaves this way for all possible inverter faults, but for the open faults on diodes D1-D4 which, however, as proven before, do not reduce the power that the inverter delivers to the load. Therefore, our monitor allows to detect all inverter's faults possibly reducing the power efficiency of the PV system.

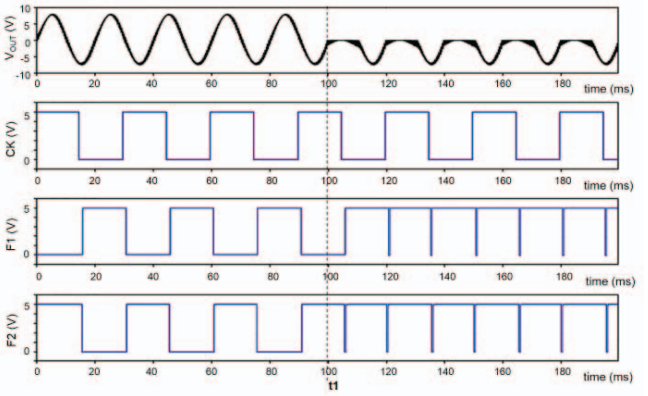

Fig. 8. Simulation results showing the V_{OUT} produced by the inverter and signals *F1* and *F2* given to the output of our monitor when the inverter is fault-free (before *t1*), and when the Controller of the inverter is affected by a fault making V1 behave as if stuck-at 0 (after *t1*).

VI. Monitor Self-Checking Ability and Power Cost

Our monitor should be self-checking with respect to its internal faults, in order to avoid that they can compromise the monitor effectiveness. Similarly to the inverter, we have considered a set of faults $\mathcal{F}$ possibly affecting our monitor consisting of: shorts between the drain and the source terminals of the transistors; opens on the gate terminal of the transistors; shorts between the two terminals of diodes; opens between the two terminals of diodes.

Similarly to checkers of self-checking circuits (SCCs) (e.g., those in [18]), our monitor should satisfy either the *Totally Self-Checking* (*TSC*) [12], or the *Strongly Code-Disjoint* (*SCD*) [19] property with respect to the faults in $\mathcal{F}$. Moreover, we have assumed the conventional hypotheses that [12]: 1) faults occur one at a time; 2) the time elapsing between the occurrence of two successive faults is longer than a period of the *CK* signal.

We have verified that our monitor satisfies the *TSC* property with respect to most faults in $\mathcal{F}$, while it satisfies the *SCD* property with respect to the remaining faults in $\mathcal{F}$, that are: *i)* shorts affecting the diode of the peak detector (D in Fig. 7); *ii)* shorts affecting transistors of the NOTs of comparators Cmp1,2 (Fig. 7); *iii)* shorts affecting the *pMOS* transistors of the NOT and EXOR gates of the pulse generator (Fig. 7).

More in details, under fault-free (faulty) conditions, our monitor maps fault-free (distorted) harmonic components of I_{PV} at its input into indications of correct operation (error) at its

output. Thus our monitor satisfies the code-disjoint (*CD*) property [12]. Moreover, we have verified that the majority of faults in $\mathcal{F}$ (*i.e.*, all faults but those in *i)*, *ii)* and *iii)*) are activated during one *CK* semi-period. When activated, they result in the generation of an error indication at the output of our monitor (*i.e.*, (*F1, F2*) = (1,1) or (0,0)) during the whole *CK* semi-period. Consequently, our monitor in self-testing (*ST*) [12] with respect to them. In the *CK* semi-period during which these faults are not activated, our monitor behaves as if it were fault-free. Therefore, our monitor is also fault-secure (*FS*) [12] with respect to these faults, therefore *TSC*.

As for faults in *i)*, *ii)* and *iii)*, they cannot be detected (so our monitor is not *ST* with respect to them). However, they do not affect the correct operation of our monitor. Moreover, we have verified that if these faults are followed by another fault in $\mathcal{F}$, either our monitor produces an error indication (during one *CK* semi-period), or such faults do not affect the correct operation of our monitor, and this holds true for all possible sequences of faults in $\mathcal{F}$. Therefore, our monitor satisfies the *SCD* property with respect to these faults.

Finally, we have evaluated the cost of our monitor in terms of impact on the efficiency of the PV system.

The efficiency of a PV system without our monitor (η_{no_mon}) and with our monitor (η_{mon}) can be expressed by:

$$\eta_{no\_mon}(\%) = \frac{100 \cdot P_{load}}{P_{load} + P_{Inverter}} \text{ and}$$

$$\eta_{mon}(\%) = \frac{100 \cdot P_{load}}{P_{load} + P_{Inverter} + P_{mon}}, \text{ respectively,}$$

where P_{load} is the power delivered by the inverter to the load, $P_{inverter}$ is the power dissipated by the inverter and P_{mon} is the power dissipated by our monitor.

By means of electrical level simulations performed by HSPICE, we have found that it is $P_{mon} \cong 0.6W$, independently of the power delivered by the inverter to the load. As an example, for a $P_{load} = 100W$, the power dissipated by the inverter is $P_{inverter} \cong 9W$, so that the power dissipated by our monitor is approximately only the 6.7% of that dissipated by the inverter. Consequently, the efficiency of the PV system without our monitor is $\eta_{no\_mon} \cong 91.7\%$, while it is $\eta_{mon} \cong 91.2\%$ when our monitor is employed.

VII. Conclusions

We have analyzed the effects of faults likely to affect the inverter of photovoltaic systems in the field. We have shown that they can reduce dramatically (up to the 80%) the power delivered to the load. We have then proposed a self-checking monitor, that is able to detect the occurrence of such inverter's faults in the field (by producing a proper error message), as well as faults possibly affecting itself. Our monitor can be adopted to guarantee the concurrent on-line test of faults affecting the inverter of photovoltaic systems. Moreover, if used together with proper recovery strategies, for instance based on hardware reconfiguration of the array in order to exclude the faulty inverter and substitute it by a proper spare, our monitor can provide photovoltaic systems with fault tolerance ability, thus meeting the increasing demand for reliable photovoltaic systems.

References

[1] European Photovoltaic Industry Association: "Market Report 2011", 2011.

[2] V. A. Kuznetsova, R. S. Gaston, S.J. Bury, S.R. Strand, "Photovoltaic Reliabity Model Development and Validation", in *Prof. of IEEE Photovoltaic Specialists Conference*, 2009, pp. 432-436.

[3] S. B. Kjaer, J.K. Pedersen, Blaabjerg, "A Review of Single-Phase Grid-Connected Inverters for Photovoltaic Modules", *IEEE Transactions on Industry Applications*, Vol. 41, 2005, pp. 1292-1306.

[4] S. V. Dhople, A. Davoudi, P.L. Chapman, A.D. Dominguez-Garcia, "Reliability Assessment of Fault-Tolerant DC-DC Converters for Photovoltaic Applications", in *IEEE Energy Conversion Congress and Exposition*, 2009, pp. 2271-2276.

[5] A. M. Bazzi, K. A. Kim, B. B. Johnson, P. T. Krein, A. Dominguez-Garcia, "Fault Impacts on Solar Power Unit Reliability", in *IEEE Applied Power Electronics Conf. and Exposition*, 2011, pp. 1223-1231.

[6] H. M. Maghraby, M.H. Shwehdi, G.K. Al-Bassam, "Probabilistic Assessment of Photovoltaic (PV) Generation Systems", *IEEE Trans. on Power Systems*, Vol. 17, 2008, pp. 205-208.

[7] F. Chan, H. Calleja, "Design Strategy to Optimize the Reliability of Grid-Connected PV Systems", *IEEE Transactions on Industrial Electronics*, Vol. 56, 2009, pp. 4465-4472.

[8] M. Omaña, D. Rossi, G. Collepalumbo, C. Metra, F. Lombardi, "Faults Affecting the Control Blocks of PV Arrays and Techniques for Their Concurrent Detection", in *Proc. of IEEE Intl. Symp. on Defect and Fault Tolerance in VLSI and Nanotechnology Systems*, 2012, pp.199-204.

[9] F. Richardeau, P. Baudesson, T. A. Meynard, "Failures-Tolerance and Remedial Strategies of a PWM Multicell Inverter", *IEEE Trans. on Power Electronics*, Vol. 17, No. 6, Nov. 2002, pp. 905-912.

[10] D. C. Martins, R. Demonti, "Interconnection of a Photovoltaic Panels Array to a Single-Phase Utility Line from a Static Conversion System", *IEEE Proc. of PESC*, Vol. 3, 2000, pp. 1207-1211.

[11] N. Mohan, "Power Electronics and Drives", MNPERE, Minneapolis, 2003.

[12] D. A. Anderson, G. Metze, "Design of Totally Self-Checking Circuits for m-Out-of-n Codes", *IEEE Trans. on Computers*, Vol. 22, No. 3, pp. 263-269, March 1973.

[13] D. Rossi, M. Omaña, D. Giaffreda, C. Metra, "Modeling and Detection of Hot-Spot in Shaded Photovoltaic Cells", *IEEE Trans. on Very Large Scale Integration (VLSI) Syst.,* Vol. 23, Issue 6, 2015, pp. 1031 – 1039,

[14] D. Giaffreda, M. Omaña, D. Rossi, C. Metra, "Model for Thermal Behavior of Shaded Photovoltaic Cells Under Hot-Spot Condition", in *Proc. of IEEE Int. Symp. on Defect and Fault Tolerance in VLSI Systems*, 2011, pp. 252 – 258.

[15] http://www.linear.com/product/LT1012

[16] http://www.ti.com/lsds/ti/logic/gate-products.page

[17] C. Xiao, L. Zhao, T. Asada, W. G. Odendaal, J. D. van Wyk, "An Overview of Integratable Current Sensor Technologies", *Conference Record of the Industry Applications*, 2003, vol. 2, pp. 1251-1258.

[18] M. Omaña, D. Rossi, C. Metra, "High Speed and Highly Testable Parallel Two-Rail Code Checker", in *Proc. of Design, Automation and Test in Europe (DATE)*, 2003, pp. 608-613.

[19] M. Nicolaidis, B. Courtois, "Strongly Code Disjoint Checkers", *IEEE Trans. on Computers*, Vol. 37, No. 6, 1988, pp. 751-756.