A Detailed Methodology to Compute Soft Error Rates in Advanced Technologies

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***Abstract*—System reliability has become a key design aspect for computer systems due to the aggressive technology miniaturization. Errors are typically dominated by transient faults due to radiation and are strongly related to the technology used to build hardware. However, there is a lack of detailed methodologies to model and fairly compare Soft Error Rates (SER) across different advanced technologies. This work first describes a common methodology that from (1) technology models, (2) location (latitude, longitude and altitude), (3) operating conditions and (4) circuit descriptions (i.e. SRAM, latches, logic gates) can obtain accurate Soft Error Rates. Then, we use it to characterize soft errors through current and future technologies. Results at the technology layer show that new technologies, such as FinFET and SOI, can reduce SER up to 100x while the location can increase SER up to 650x.**

I. Introduction

Aggressive technology scaling introduces a large set of different sources of failure for hardware components [3]. Therefore, reliability has become an important design concern for modern computer systems. Unreliable hardware components affect computing systems at several levels, spanning from electronics to applications. Errors are strongly related to the technology used to build the hardware blocks composing the system and are caused by effects such as physical fabrication defects, aging (e.g., NBTI), environmental stress (e.g., radiations), etc.

After a fault manifests in a given hardware block, it can be propagated through the different hardware/software layers composing the full system. Even if several faults can be masked during this propagation some of them can possibly reach the software layer of a system by corrupting either data or instructions composing an application, as is shown in Figure 1. These errors can prevent the correct execution producing erroneous results if the computation is completed, or even prevent the execution of the application by causing exceptions, abnormal termination or lead to an application crash. This may have a serious impact on the overall reliability of the system.

Radiation induced failures (RIF), more commonly called Soft Errors, have a huge impact on reliability and are becoming a major concern in the industry [2]. In this context a comprehensive analysis and comparison of the impact of future and existing technologies on Soft Error Rates (SER) is of paramount importance. Therefore, in this paper we analyze and characterize the effect of radiation due neutron strikes in current and future technologies. We have simulated the most common and basic elements of hardware with different technology models, which are shown in Table I, to characterize their vulnerability to soft errors. We have developed a detailed methodology, homogeneous across technologies for having accurate SER estimates and a fair comparison across technologies. For that purpose, we have first identified predictive models for future technologies and developed SPICE circuits for the components that our analysis targets. Second, we have performed SPICE simulations to test the reliability of these components with the different technologies and parameters like voltages or temperatures. Finally, SER of each basic component are obtained and used to compute

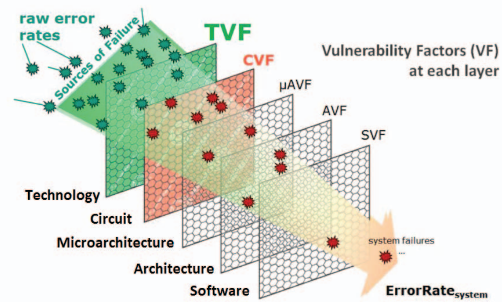

Fig. 1. Error Propagation through different levels

TABLE I
HARDWARE ELEMENTS AND TECHNOLOGIES ANALYZED

Technology (CMOS)	Technology Nodes
Bulk Planar (ASU PTM Models)	22nm and 16nm
Bulk FinFET (ASU PTM Models)	20nm and 14nm
SOI Planar (UTSOI Model)	22nm

X

Circuits
SRAM Cells 6T/8T/10T
Flip Flop - D
Latch
Logic Gates (AND, OR, NOT)

the SER of more complex components like SRAM memories or logic blocks. Moreover, we analyze some important trends about SERs using the data obtained.

The main contribution of this paper is, therefore, a detailed methodology to estimate the SER of the most common hardware components built with different technologies, as well as a detailed analysis of the results obtained and the trends observed.

The rest of the paper is organized as follows: section II describes the fundamentals and related work on soft errors, section III describes the methodology used for our characterization of soft errors, section IV analyzes and discusses the results obtained and finally section V describes future work and gives some final conclusions.

II. Background and Related Work

RIF [18] are mainly produced by two types of sources, alpha particles from the packaging and neutrons from the atmosphere. Alpha particles are already well known and they can be mitigated by changing the packaging materials of the chip. On the other hand, neutron strikes produce soft errors that are difficult to detect and have a high impact on the reliability. Therefore, we focus on computing the SER due to neutrons.

A particle that hits a transistor of an electronic device produces a certain amount of electrical charge. This charge needs to cross a certain threshold to activate an off transistor, producing different results such as losing the stored data or a glitch in the output of a logic gate producing wrong results. This minimum charge necessary to cause a circuit malfunction is termed as the critical charge of the circuit and is represented as Qcrit. Typically, Qcrit is estimated in circuit models by injecting different current pulses in the sensitive nodes of an element till

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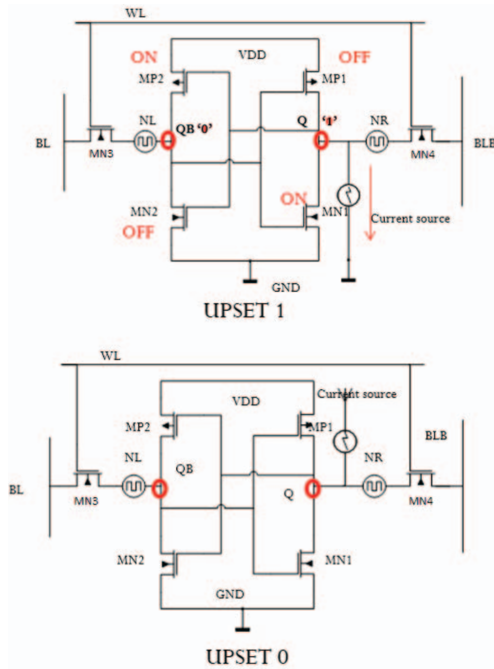


Fig. 2. Induced Soft Error in a 6T SRAM Cell

the circuit malfunctions. Figure 2 shows an example with a 6T SRAM cell made of a pair of inverters. The pulse is injected in the sensitive node Q, where the value is stored, and the current injected is increased until the charge is high enough to activate the OFF transistor. Then, the disturbance is propagated to the second sensitive node causing the cell to flip its value.

Hazucha and Svensson [9] proposed the following model to predict neutron induced SER:

$$CircuitSER = Constant \times Flux \times Area \times e^{\left(-\frac{Qcrit}{Qcoll}\right)} \quad (1)$$

Constant is a constant parameter dependent on the process technology and circuit design style, *Flux* is the flux of neutrons at the specific location, *Area* is the area of the circuit sensitive to soft errors, and *Qcoll* is the charge collection efficiency, which is the ratio of collected and generated charge per unit volume. *Qcoll* depends strongly on doping and *Vcc* (operating voltage) and can be derived empirically using either accelerated neutron tests or device physics models, whereas *Qcrit* is derived using circuit simulators.

With every process generation, the area of a given circuit shrinks, so this should reduce the effective SER from one process generation to the next. However, Qcrit also decreases because the voltage of the circuit decreases across process generations. Therefore, for some elements like latches and logic, these effects are often assumed to cancel each other out, resulting in a constant SER across generations. However, if Qcrit is sufficiently low, such as in SRAM devices, then the impact of the area begins to dominate. This is referred to as saturation effect, where the SER decreases with process generations. However, the circuit is highly vulnerable to soft errors in the saturation region. In the extreme case, as Qcrit approaches zero, almost any amount of charge produced by alpha or neutron strikes will result in a transient fault.

Ziegler and Lanford [25] demonstrated in 1979 that cosmic rays creating energetic neutrons could cause soft errors. Indeed, in modern devices, cosmic rays are the predominant cause of soft errors. They analyzed SRAM memories with experimental tests and developed their own method to characterize soft errors, the Burst Generation Rate (BGR) method. From that point, many researchers have studied the effect of neutron strikes in electronic devices. One of the most important studies is the one from Hazucha and Svensson [8]. They analyzed a 65nm SRAM with experimental tests and then proposed a model to characterize soft errors through different technologies.

Many studies focus on characterizing the SER of individual components such as latches [16], flip flops [12] or SRAM cells [13], using Hazuchas model or experimental tests. Some of these studies also provide alternative designs of these components to improve their resistance to radiation. In addition, there have been some studies analyzing all the basic components including combinatorial logic [10]. Nevertheless, most of them are done for bulk planar technologies up to 22nm only. There are also some recent studies on new technologies such as FinFET [24], SOI [5][15] and III-V HEMT [17], but those studies do not allow a cross-technology comparison.

Our work provides the soft error characterization of all the basic components that can be found in any electronic device and data for the most recent technologies, materials and technology nodes. In addition, we also provide data for different environmental setups. To the best of our knowledge, in the literature there is not a study comparing SERs for all those recent technologies on the same ground. Works analyzing specific technologies build upon different assumptions and methodologies, thus limiting the conclusions that can be extracted when comparing these works. In contrast, our work shares the same assumptions and methodology for the different technologies compared and, consequently, results across circuits and technologies are fully comparable.

III. Methodology

Our methodology follows the workflow in Figure 3. As we target an exhaustive design space characterization, we wrote a python script for each component that is analyzed. Each script defines a collection of loops to simulate an element with a variety of configuration parameters, such as temperatures and voltages, and different technology models. In the inner loop, a function call is made. This function defines another loop to iterate the current injected in the sensitive nodes of an element until a flip or glitch is detected measuring the stored value (SRAM) or the output (Logic Gates). An example of such scripts is shown in Algorithm 1. To make the SPICE simulations, HSPICE [23] which is a commercial circuit simulator from Synopsis, is invoked in a subprocess. The minimum charge generated from a pulse that causes a malfunction is stored and defined as the Qcrit of that element. Finally, for each Qcrit, a raw SER is computed using the model in [9]. In this methodology, we model the propagation of the current generated from a strike through the substrate of one transistor. Therefore, we assume that one strike only affects one transistor. Analyzing the effect of one strike on multiple transistors is part of our future work.

There are some factors that affect the Qcrit obtained such as the voltage and the temperature [11][19][4]. Because of that, we decided to test a variety of parameters and compute a Qcrit for each combination. Voltage ranges from 0.7V to 1.2V which can be used to distinguish between high performance and low power processors. Temperatures tested include 25, 50, 75 and 100 C^o which can be used to map idle, typical and extreme conditions. Stored values 0 and 1 have been tested for SRAM cells, and for logic gates all the input combinations have been analyzed. Moreover, each element may have more than one sensitive node so all nodes are considered. A double exponential pulse is used to simulate the charge generated from a neutron strike, since it

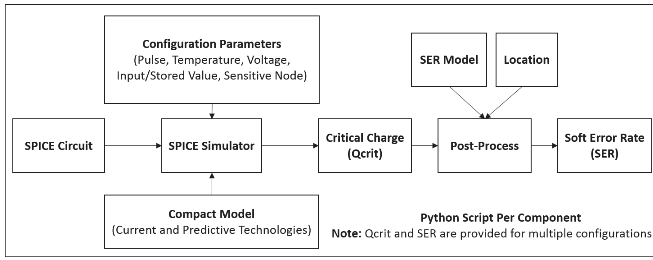


Fig. 3. Workflow schema

Algorithm 1 Script Pseudo-code

```
for all Technologies do
  for all Voltages do
    for all Temperatures do
      for all Inputs or Stored values do
        for all Sensitive Nodes do
          Current = 0;
          Flipped = 0;
          while not flipped do
            Increase Current Injected;
            Generate SPICE Files;
            Simulate Element in HSPICE;
            Read Simulation Results;
            if Flip Detected then
              Flipped = 1;
              Write Results in Database;
            Clean Simulation Files;
End all loops
```

is the most commonly used model by the community. The shape of the current pulse also strongly affects Qcrit. For that reason, multiple rise time constants used in the literature (2ps, 16ps, 33ps and 90ps) have been tested but maintaining a falling time constant of 200ps. The pulse width also has a strong effect on Qcrit affecting the integral range. Looking at the literature, there is not a clear way to define the pulse width so we decided to define it from the start of the pulse until the pulse decreases an 80% of its maximum which represents the spike of the pulse. Then, Qcrit is computed by doing the integral of the current pulse in that range.

Once Qcrit has been obtained, it needs to be mapped into a SER expressed in Failure in Time (FIT), which are the number of failures in one billion (10^9) device-hours of operation. We used the model of Hazucha and Svensson [9] that has already been described (see eq. 1) but using Qs instead of Qcoll:

$$SER_{raw} = Constant \times Flux \times Area \times e^{\left(-\frac{Qcrit}{Qs}\right)} \quad (2)$$

The area sensitive to neutron strikes is the drain area of the transistors which is defined in the netlists of the SPICE circuits, so it can be easily obtained. The constant is a technology independent parameter which was computed by Hazucha and Svensson and has a value of $2.2 * 10^{-5}$. The exponential part of the formula is the technology vulnerability factor (TVF). If the charge collected (Qcoll) by a particle is greater than Qcrit a soft error is produced. Charge Collection Efficiency (Qs) is the mean of Qcoll in a range of energy particles and a parameter dependent on the technology which is usually computed experimentally. However, Qs scales approximately linearly with the Length of the Gate (Lg), so Qs has been scaled down with a linear regression from experimental data [9] for CMOS technology. In the case of newer technologies, a study of how Qcoll changes has been done, and an approximate technology factor has been extracted from previous works [5][1][6]. Therefore, Qs has been scaled based on available empirical data to enable the comparison across technologies while minimizing the impact on accuracy.

The reference neutron flux commonly used in the SER computation is from New York City at sea level. However, neutron flux depends on the location and is mainly affected by two parameters: Altitude and Vertical Cutoff [26]. Neutron flux increases exponentially with the altitude while the vertical cutoff is a parameter of the magnetic field of the Earth which depends on the coordinates. The maximum Earth magnetic field is in the poles while the minimum is in the equator. Therefore, the neutron flux decreases when approaching the equator and increases in the poles. There are two main ways to compute the flux considering the location. The first one involves using the methodology described in Annex A of the JEDEC standard [22]. Alternatively, one can use the online calculator from [21] which is compatible with the JEDEC standard and outputs the flux relative to the flux from NYC. The second method involves the use of a model tested and corrected with empirical data which has been proposed by Gordon et al. [7], and has the following high level form:

$$F = F_{ref} \times F_{alt}(d) \times F_{BSYD}(Rc, d, I) \quad (3)$$

Gordon's model to compute the neutron flux dependent of the location can be combined with the SER model. However, we omit the details on this model since we use the online calculator [21].

To conclude, multiple SER values are obtained for each combination of parameters. The SER of the circuit or element is the sum of the SER for all sensitive nodes [10]. Therefore, SER from different sensitive nodes but same conditions are added. For example, a 6T SRAM cell has two sensitive nodes which are symmetric. Therefore, the SER of the cell can be computed as the sum of the SER of one node storing a 1 and the SER of the other node storing a 0. Then, depending on the element, SERs are derated by a timing factor, such as the latch where a factor of 50% is applied. Finally, a weighted average can be done with the SERs of different states to give a unique SER for the element. This is the case of logic gates where the SER can be averaged by the SERs of the different inputs, but still there will always be multiple SERs for the different voltages, temperatures and current pulses.

IV. Results

As has been already described, to obtain the SER of a component, Qcrit is required. Qcrit is obtained with HSPICE simulations by inserting a current pulse in the sensitive nodes of the component. This section describes how the SER has been computed for each component, summarizes some of the results obtained and provides plots to show different trends.

A. SER of Basic Hardware Elements

To obtain the Qcrit of the SRAM cell, current pulses are inserted in the storage node Q since the other node (Qb) is symmetric as shown in Figure 2. The dimensions of the 6T cell used have been taken from the literature and summarized in Table II in terms of lambdas [20] and number of fins (nfins) [14]. The values of Qcrit obtained are summarized in Table III, showing the maximum, the minimum and the average Qcrit from all the environmental parameters tested (i.e. voltage, temperature, stored value and pulse time). The latest technology nodes have usually lower critical charge than their

TABLE II
6T SRAM CELL SIZE

Size in terms of Lambdas (L/W) and NFINS			
Technology	**MP1-MP2**	**MN1-MN2**	**MN3-MN4**
Bulk and SOI (L/W)	3/3	2/8	2/4
FinFET (NFINS)	1	2	2

TABLE III
6T SRAM CELL QCRIT

6T SRAM Cell Summary (from all the environmental parameters)			
Technology	**Minimum Qcrit (fC)**	**Maximum Qcrit (fC)**	**Average Qcrit (fC)**
22nm Bulk Planar	0.07	35.89	5.79
22nm SOI Planar	0.53	43.97	9.70
20nm Bulk FinFET	1.94	120.10	21.00
16nm Bulk Planar	0.03	22.79	3.64
14nm Bulk FinFET	2.74	104.00	30.09

predecessors. However, recent technologies, such as FinFETs and SOI improve this aspect and they have a higher Qcrit.

A SER is computed for each Qcrit. Then, as the total SER of the element is the sum of the SER from all sensitive nodes, in the case of SRAM cells, SER from the same environment (voltage, temperature and pulse) but different stored values (0 and 1) are added because the cell has two sensitive nodes and each one always stores the inverse of the other node. Moreover, we could also weight SER values depending on the state of the cell (i.e. holding, reading and writing), but as most of the time cells are holding a value, only the holding mode is considered. Table IV shows the total SER of the 6T and 8T cells simulated with typical environmental parameters (1V, $50C^o$) and the pulse of 2ps which is the worst case.

Both cells have similar SER values, and similar values are obtained with the 10T cell (omitted due to lack of space), as the core of all the cells is the 6T and they all have the same sensitive nodes. The highest SER are with bulk planar and the lowest with bulk FinFET, which corresponds with the highest and lowest Qcrit values. In the case of bulk planar, the 16nm node has lower SER than the 22nm node. This occurs because the reduction in area has more effect when Qcrit values are already very low, overcoming the reduction of Qcrit.

The methodology used to compute the Qcrit of the latch is similar to the methodology used for SRAM cells. However, the latch can be in two modes, transparent, which is when the latch transfers the input value to the output, or holding the value, being 50% of the time each one. Only the hold mode is considered on the following results since in transparent mode the flipped value is usually overwritten and can be only propagated if the flip happens in a very specific moment (setup time). Table V shows the Qcrit values obtained for the latch, showing the maximum, the minimum and the average Qcrit for all the combinations of parameters. Results are similar to those of SRAM cells, being FinFET and SOI technologies the most robust ones by having a higher Qcrit.

Similarly to SRAM cells, SER from both sensitive nodes are added for each environmental setup (i.e. Temp, V). Then, SER of different inputs (0 and 1) are weighted considering equal probabilities. Finally, since we only consider the holding mode, we assume that 50% of the time the latch is not sensitive to particle strikes, so we apply a 0.5x derating factor to the SER. Table VI shows the total SER of a latch. The critical charges are similar to the ones of the SRAM cells. However, since the SERs of the latch are derated by a time vulnerability factor of 50%, the final results are lower. The technology comparison shows similar trends, being SOI and FinFET more robust to soft errors. Flip flop results are similar since it is composed of two latches being each one vulnerable 50% of the time, so results

TABLE IV
6T AND 8T CELLS SERS

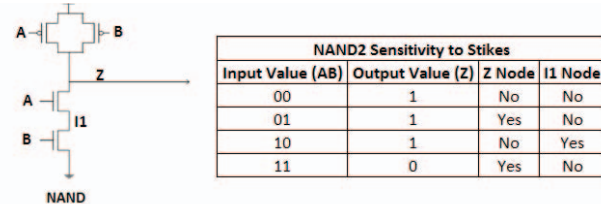
SRAM Cells with Typical Conditions (1V, $50C^o$)		
Technology	**6T Total SER (FIT)**	**8T Total SER (FIT)**
22nm Bulk Planar	2.04E-05	1.99E-05
22nm SOI Planar	1.17E-06	1.17E-06
20nm Bulk FinFET	2.04E-07	1.85E-07
16nm Bulk Planar	1.09E-05	1.07E-05
14nm Bulk FinFET	5.59E-09	3.57E-09

TABLE V
LATCH QCRIT VALUES

Latch Summary (from all the environmental parameters)			
Technology	**Minimum Qcrit (fC)**	**Maximum Qcrit (fC)**	**Average Qcrit (fC)**
22nm Bulk Planar	0.54	16.79	4.27
22nm SOI Planar	0.39	63.39	4.26
20nm Bulk FinFET	1.90	39.05	12.49
16nm Bulk Planar	0.36	8.19	2.40
14nm Bulk FinFET	2.71	117.40	21.88

are omitted.

Logic gate SER analysis is done by injecting the current pulses in the internal nodes that are sensitive to neutron strikes, which depends on the inputs and gate type. Understating that a particle strike activates an off transistor, we can analyze which nodes are sensitive to particle strikes and inject the current pulse in these nodes. Choosing a NAND of 2 inputs as example, we obtained Figure 4, which shows which nodes are sensitive for each combination of inputs. This analysis is done for each gate to simulate the strikes only in the sensitive nodes. Qcrit values for the NAND2 are shown in Table VII.



NAND2 Sensitivity to Stikes			
Input Value (AB)	Output Value (Z)	Z Node	I1 Node
00	1	No	No
01	1	Yes	No
10	1	No	Yes
11	0	Yes	No

Fig. 4. NAND2 Sensitivity Analysis

A SER is computed for each input combination by adding the SER of all the sensitive nodes. Then, the SER of each input combination are weighted by the probability of the input to occur, but for now, equal probabilities are considered. SER results for the NAND2 are shown in Table VIII.

SER values of logic gates are even lower than for SRAM cells and latches. This occurs because for each combination of inputs, a gate usually has one or even none sensitive nodes to strikes. In contrast, the SRAM cells and the latch always have two sensitive nodes. Therefore, when computing the SER as the average of all different input combinations the SER of the gate is reduced and it is thus lower than in other components.

B. Trends in Soft Error Rates

Gathering the results of the previous subsection we can discuss the results and give some trends by comparing the technologies, temperatures, voltages and locations.

Figure 5 shows the SER of different components and technologies, where each color represents a technology and each group of bars a component. SERs are in logarithmic scale. As shown, the higher SER correspond to bulk planar and the lower to bulk FinFET with SOI planar in the middle. Therefore, the most vulnerable technology is the bulk planar while bulk FinFET and SOI planar can reduce SERs up to 100x, which makes sense since the sensitive area and the collected charge are bigger in bulk planar. Across components, both memory

TABLE VI
LATCH SERS

Latch with Typical Conditions (1V, 50C^o)	
Technology	**Total SER (FIT)**
22nm Bulk Planar	5.97E-06
22nm SOI Planar	4.59E-07
20nm Bulk FinFET	1.02E-07
16nm Bulk Planar	2.58E-06
14nm Bulk FinFET	2.49E-09

TABLE VII
NAND2 QCRIT VALUES

NAND2 Summary (from all the environmental parameters)			
Technology	**Minimum Qcrit (fC)**	**Maximum Qcrit (fC)**	**Average Qcrit (fC)**
22nm Bulk Planar	0.73	63.39	15.78
22nm SOI Planar	0.68	153.00	21.65
20nm Bulk FinFET	3.33	214.40	50.07
16nm Bulk Planar	0.59	87.05	16.35
14nm Bulk FinFET	4.51	314.80	75.42

cells have similar results, the latch is a bit more reliable as it is vulnerable 50% of the time and the NAND2 has the lower SERs. Typical logic gates (NAND, NOR and NOT) usually have fewer sensitive nodes to strikes for each input combination, resulting in a total SER lower than in other components.

In addition, in bulk technology, lower nodes have lower SER which may seem contradictory as in lower nodes Qcrit is usually reduced. However, the reduction in area has a stronger effect when the critical charge is already very low. Therefore, if we look at the SER/Area in Figure 6, both nodes of bulk planar are quite similar, being slightly higher the node of 16nm. Thus, if we put more elements the total SER of a 16nm chip will increase. The area of the cell in 22nm is $0.240\mu m^2$ while the cell in 16nm is $0.127um^2$. In the case of FinFETs, our results show that the critical charge of the 14nm node is lower than the one with 20nm. Therefore, adding the lower critical charge, the reduction in the sensitive area and the reduction in the collection efficiency, results in much lower SER values.

Figure 7 compares the SER of a 6T SRAM cell for different source voltages, temperatures and technologies. SER increases with lower operating voltages since the critical charge becomes smaller. Therefore, it is easier to flip the value. The SER may be as high as 70x as can be seen with the red arrows of the plot. On the other hand, SER increases with higher temperatures since the critical charge becomes smaller. Even if apparently the variation is low, it can be greater than 20% as indicated with the red arrows of the plot, but still has a low effect compared with the voltage variation. In the case of FinFET technology, the models used do not model the temperature accurately so the variations are very low and slightly oscillating.

Figure 8 shows neutron fluxes of different European locations relative to the reference flux from New York City at sea level. The higher neutron fluxes are located in Västerås as it closer to the pole while the lower is in Athens which is near the equator. These relative fluxes have been computed using the online calculator [21] with a medium solar activity of 50%. The relative fluxes can be multiplied directly by the Soft Error Rates (SER) obtained with the reference flux to obtain the SER of the desired location. We have computed the SERs of a 6T SRAM cell at different locations and altitudes as shown in Figure 9. The difference between cities is due the influence of the magnetic field of the Earth, where cities near the equator have lower SER. Moreover, there is an exponential increase of the SER when varying the altitude that can be as high as 650x.

To summarize, voltage and location are the operating conditions that have been proven to have an important impact in the reliability of a chip. Nowadays, the power consumption is the main focus of attention and consequently the voltage is reduced for lower power consumption. However, reliability is becoming an important parameter so it should be taken into account when deciding the voltage used in a processor. There is already a tradeoff between the power consumption and the performance, but the reliability should also be included. Location has the greatest impact in SER, especially when varying the altitude. Therefore, it is important to take location into account when developing electronic devices for airplanes. Finally, the most important trend has been seen in the technology comparison. According to the results, bulk FinFET is the most robust technology from the ones analyzed. Moreover, lower technology nodes of FinFET are even more robust to radiation induced failures. SOI planar also shows good results, and maybe the combination of both, SOI FinFET, could be the best option for reducing SER in the future.

TABLE VIII
NAND2 SERS

NAND2 with Typical Conditions (1V, 50C^o)	
Technology	**Total SER (FIT)**
22nm Bulk Planar	1.78E-06
22nm SOI Planar	5.33E-08
20nm Bulk FinFET	1.35E-09
16nm Bulk Planar	7.75E-07
14nm Bulk FinFET	2.02E-12

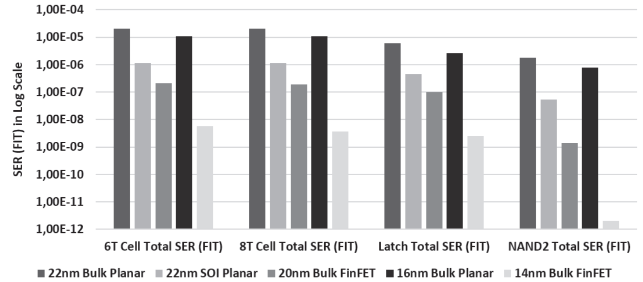


Fig. 5. SER Technology Comparison

V. CONCLUSIONS AND FUTURE WORK

This paper focuses on the characterization of soft errors due neutron strikes, which have been the major reliability concern of the industry in the last years and are also expected to be in the near future. Looking at the results, it is obvious that as bulk planar technology scales down, Qcrit is lower so the elements may become more vulnerable to soft errors. However, the scaled area and collection efficiency overcomes the reduction of Qcrit making the SER almost constant or even a bit lower. Nevertheless, taking into account the increase in the number of elements integrated in a chip when the technology scales down, the SER increases and becomes an important issue for the reliability of the device. On the other hand, newer technologies, such as multi-gate FinFETs, and newer materials, such as SOI, are more resistant to radiation effects. In addition, we have shown that environmental parameters, such as temperature and voltage, and the location, may have a huge impact on the soft error rates, specially the altitude, which may increase the SER by up to 650x. In conclusion, this study suggests that newer technologies can reduce soft error rates up to 100x whereas planar CMOS is becoming more vulnerable due to the scaling down of its components and the increased number of elements.

As part of our future work, we plan to incorporate III-V HEMT and SOI FinFET models. Also, we are currently studying Multi Cell Upsets (MCU) where a single strike flips the stored values of multiple SRAM cells. MCU effect occurs when the

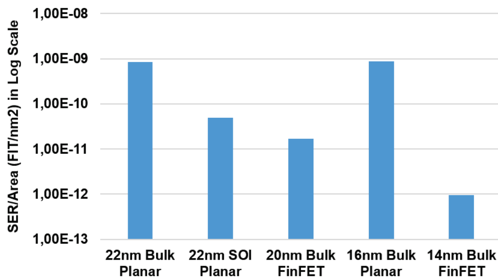


Fig. 6. SER Area Comparison

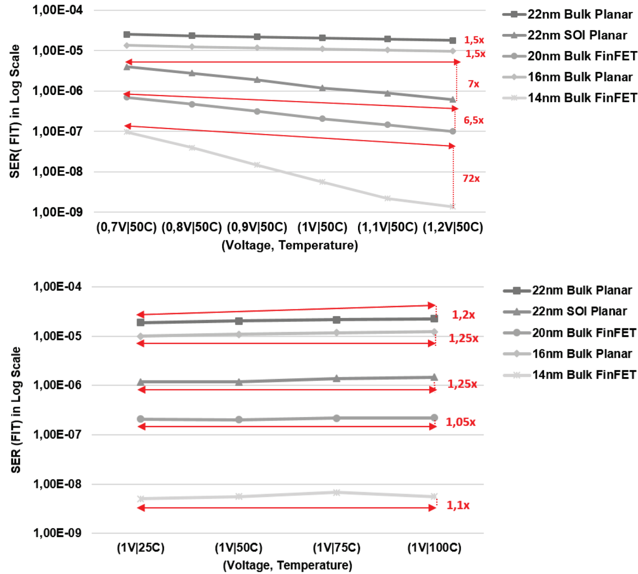


Fig. 7. SER Voltage and Temperature Comparison

charge cloud produced by one strike in a cell is large enough to affect the cells that are near and becomes more significant when technology shrinks since elements are closer.

Acknowledgments

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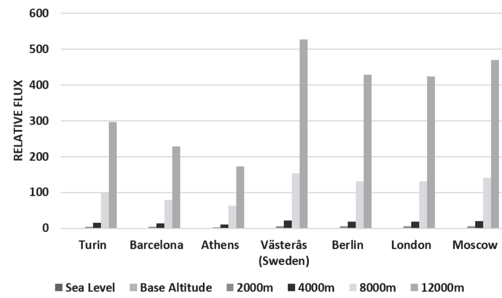

Fig. 8. Relative Neutron Fluxes

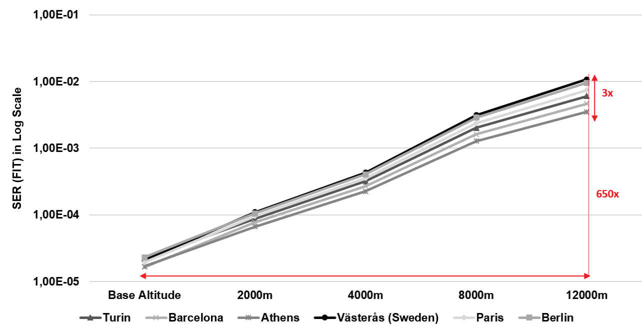

Fig. 9. SERs depending on the Location and Altitude

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