Analytical Design Optimization of Sub-ranging ADC Based on Stochastic Comparator

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***Abstract*—An optimal design method for a sub-ranging Analog to Digital Converter (ADC) based on stochastic comparator is demonstrated by performing theoretical analysis of random fluctuations in the comparator offset voltage. The proposed performance model is based on a simple but rigorous Probability Density Function (PDF) for the effective resolution of a stochastic comparator. It is possible to approximate the yield of a stochastic comparator by assuming that the correlations among different analog steps of the output transfer function are negligible. Comparison with Monte Carlo simulation shows that the proposed model precisely estimates the yield of the ADC when it is designed for a reasonable target yield of > 0.8, which is the most practical case while designing a high performance ADC. Application of this model to a stochastic comparator reveals that an additional calibration can significantly enhance the resolution, i.e. it can increase the Number of Bits (NOB) by approximately 2 bits under the same chip yield. Extending the model to a stochastic-comparator-based sub-ranging ADC indicates that the ADC design parameters can be tuned to find the optimal resource distribution between the deterministic coarse stage and the stochastic fine stage.**

***Index Terms:* Sub-ranging ADC, Stochastic comparator, Yield, Probability Density Function, optimization, Calibration**

I. Introduction

Analog-to-Digital Converter (ADC) is one of the most basic circuit components in modern systems. ADCs are, in general, composed of comparators that determines the relative level of an input signal by comparing it with a reference voltage. In recent years, the downsizing of circuit components in large scale systems has increased the impact of process variation. Process variation, together with other factors such as temperature and voltage variation, causes mismatches in the design parameters that eventually lead to threshold voltage fluctuation in these comparators [1]. This is called the offset voltage of a comparator circuit which causes nonlinearity and missing codes in the output of an ADC and thus seriously limits its performance. To overcome this problem, redundancy in the comparator circuit has been introduced [2]. This redundancy eventually led to the idea of a stochastic ADC, which implements a large number of comparators with the same design parameters and utilizes the distribution of the offset voltages to determine the input level. Although a number of implementations of a stochastic ADC have been reported [3], [4], a rigorous theoretical study demystifying the relation between various parameters such as effective resolution, Number of Bits (NOB), offset voltage Probability Density Function (PDF), etc., have not been done yet. We establish a rigorous quantitative relation among these parameters in this study. In addition, stochastic ADC normally has a nonlinear transfer function, which can be improved by inserting a calibration circuit [5]. A number of self-calibrating stochastic ADC have been implemented, but any analytical study which quantitatively describes the merit of calibration is yet to be reported. In section II of this paper, we propose a Probability Density Function for the effective resolution and the output code of a stochastic ADC by analyzing random fluctuations in the offset voltage considering only the static process variations and ignoring the dynamic noise components. These functions establish a clear connection among different parameters of a stochastic ADC and allow us to calculate its yield.

The measurement range of a stochastic ADC is limited by the offset voltage distribution of the comparators. To overcome this problem of a narrow measurement range, sub-ranging ADC dividing the measurement process in a coarse stage using conventional deterministic ADC and then in a fine stage using stochastic ADC has been proposed [6], [7]. But, as the characteristics of the stochastic part was not well understood, designing a sub-ranging ADC was done mainly on a trial-and-error basis. In section III, we applied our analysis to calculate the yield of a sub-ranging ADC and used it as an objective function to find an optimal balance in the NOB or other design parameters between the coarse and the fine stage. Although correlation among different analog steps corresponding to the LSB of the ADC was ignored, Monte Carlo Simulations confirmed that this method can precisely estimate the yield for practical ADC designs where yield > 0.8.

II. Yield of a Stochastic ADC

Stochastic ADC uses a lot of comparators with the same design parameters. The diagram of a typical stochastic ADC is shown in Fig. 1. When a lot of comparators are designed, process variation inevitably introduces variation in the offset voltages of these comparators which has a Probability Density Function denoted as $P_{\text{Offset}}(V)$. As a prior work verified with measurement [3], this offset variation can be modeled by a *Gaussian* distribution and many papers have employed it for their analyses [3]–[7]. Therefore, we will also assume a *Gaussian* distribution for $P_{\text{Offset}}(V)$ in our analysis as follows.

$$P_{\text{Offset}}(V) = \frac{1}{\sigma_{\text{Offset}}\sqrt{2\pi}} \exp\{-\frac{(V-\mu_{\text{Offset}})^2}{2\sigma_{\text{Offset}}}\} \tag{1}$$

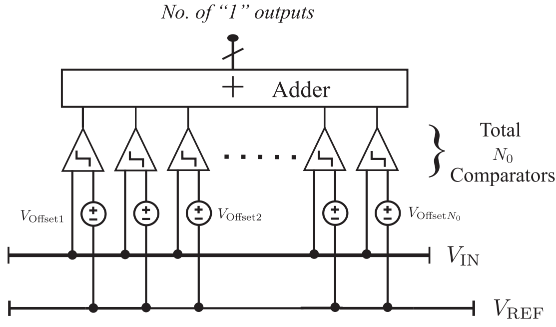


Fig. 1: Stochastic ADC architecture

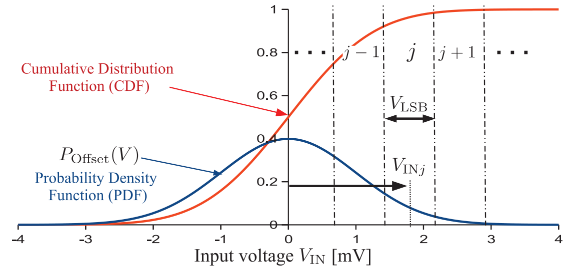


Fig. 2: Input voltage, V_{IN} and LSB, V_{LSB} in terms of comparator offset voltage probability density function.

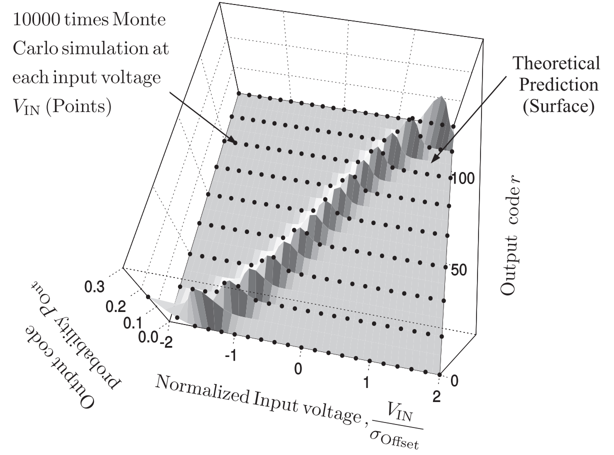


Fig. 3: Output code probability density function. Gray surface is from (3), the points represent Monte Carlo simulation result. Solid lines drawn to represent the error between these are invisible.

Here, σ_{Offset} is related to the comparator circuit area A and a process dependent constant k in the following manner [8].

$$\sigma_{\mathrm{Offset}} = \frac{k}{\sqrt{A}} \tag{2}$$

Note that the PDF can be an arbitrary distribution in our analysis as long as its Cumulative Distribution Function, ρ_{C} is known. If the offset variation need to be modeled by a non-*Gaussian* distribution, $P_{\mathrm{Offset}}(V)$ in (1) can be replaced by the specific distribution function. It can also be replaced by numerical values from circuit measurement results. Nevertheless, the nature of the distribution is not crucial for the results presented in this paper if the CDF of the distribution is defined appropriately.

When we use a relatively large number of comparators, the total number of comparators with output "1" at a given input voltage corresponds to the CDF of the offset voltage variation. We can either measure using an ideal comparator offset CDF or by recording a distinctive transfer curve for each chip. The former is called measurement without calibration and the latter is called measurement with calibration. "Calibration" in this paper means a mapping of the ADC output code (not a usual comparator offset calibration), which can be typically implemented by a mapping memory.

A. Output Code Probability

Let us assume that we have a total N_0 comparators in a stochastic ADC that has an offset voltage distribution as defined by (1). Then, we divide the input voltage range in small analog steps of $V_{\mathrm{LSB}} = 1\,\mathrm{LSB}$ and denote each step by a subscript j as shown in Fig.2. Now, for a given input voltage $V_{\mathrm{IN}j}$ the output r, which is defined as the total number of comparators with output "1," can be anywhere between $0 \sim N_0$. It follows a binomial distribution, $P_{\mathrm{Out}}(r)$ as given below where the probability of success $\rho_{\mathrm{C}j}$ is defined as the CDF of the offset voltage distribution at the input voltage level $V_{\mathrm{IN}j}$.

$$P_{\mathrm{Out}}(r) = \binom{N_0}{r} \rho_{\mathrm{C}j}^{r} (1-\rho_{\mathrm{C}j})^{N_0 - r}, \tag{3}$$

$$\text{where } \rho_{\mathrm{C}j} = \int_{-\infty}^{V_{\mathrm{IN}j}} P_{\mathrm{Offset}}(V)dV \tag{4}$$

The probability density function of the output code, together with Monte Carlo simulation is shown in Fig. 3 where we assumed that the comparator offsets follow a *Gaussian* distribution as given in (1). We have used the values $N_0 = 128$, $\sigma_{\mathrm{Offset}} = 3\,\mathrm{mV}$ and $\mathrm{LSB} = \sigma_{\mathrm{Offset}}/10$ here. The same values are used for subsequent simulations unless otherwise stated. The ideal transfer curve would be $N_0 \rho_{\mathrm{C}j}$. This is the mean value of the output code and it can be used to measure the input voltage. As this approach do not record the output transfer curve in a memory, it is regarded as the measurement method without calibration.

B. Probability of Effective Resolution

If we consider a small analog voltage step of V_{LSB} at an input voltage $V_{\mathrm{IN}j}$, the probability of having m comparator offset voltages within V_{LSB}, $P_{\mathrm{Comp}j}(m)$ is expressed as the following equation where $\rho_{\mathrm{D}j}$ is the probability of finding a comparator offset within V_{LSB} when only 1 comparator is used.

$$P_{\mathrm{Comp}j}(m) = \frac{N_0!}{m!(N_0-m)!} (\rho_{\mathrm{D}j})^m (1-\rho_{\mathrm{D}j})^{N_0-m}, \tag{5}$$

$$\text{where } \rho_{\mathrm{D}j} = \int_{V_{\mathrm{IN}j} - \frac{V_{\mathrm{LSB}}}{2}}^{V_{\mathrm{IN}j} + \frac{V_{\mathrm{LSB}}}{2}} P_{\mathrm{Offset}}(V)dV \tag{6}$$

This is a binomial distribution and it meets the normalization condition $\left(\sum_{m=0}^{N} P_{\mathrm{Comp}j}[m] = 1\right)$. The mean value is $N_0 \rho_{\mathrm{D}j}$

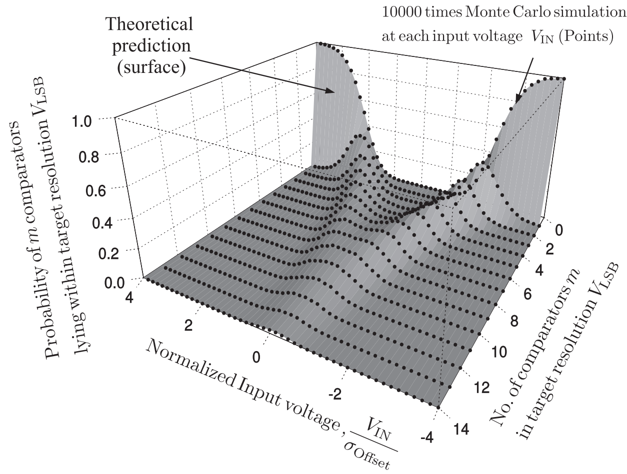


Fig. 4: Probability density function of having m comparator offsets within an analog step of $V_{\mathrm{LSB}} = \sigma_{\mathrm{Offset}}/10$. Gray surface is calculated from (7) and the points represent Monte Carlo simulation result. Solid lines drawn to show the error between these are almost invisible.

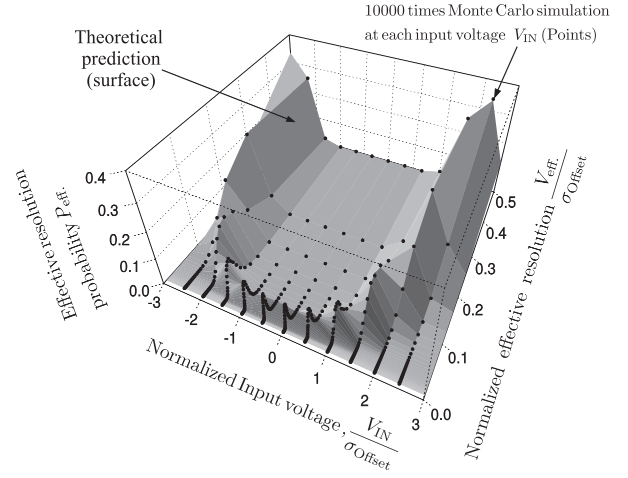


Fig. 5: Probability density function of effective resolution. Gray surface is from (8), points are for Monte Carlo simulation and the almost invisible solid lines are for the difference between them.

and the standard deviation is $\sqrt{N_0\rho_{\mathrm{D}j}(1-\rho_{\mathrm{D}j})}$. Note that $\rho_{\mathrm{D}j}$ is equivalent to $\rho_{\mathrm{C}j+1} - \rho_{\mathrm{C}j}$ which means that if the CDF, $\rho_{\mathrm{C}j}$ of a distribution is known, we can find $\rho_{\mathrm{D}j}$ as well.

The relation $\rho_{\mathrm{D}j} \ll 1$ holds because the small analog step of V_{LSB} is relatively small compared to the whole distribution range, i.e. $[-3\sigma_{\mathrm{Offset}}, 3\sigma_{\mathrm{Offset}}]$. Considering that N_0 is very large, the distribution in (5) reduces to a *Poisson* distribution with an average value of $\lambda = N_0\rho_{\mathrm{D}j}$ as showed in the expression below. Also, the probability density function is normalized because $\sum_{m=0}^{N} P_{\mathrm{Comp}j}[m] = 1$ when N_0 is large.

$$P_{\mathrm{Comp}j}[m] = \frac{\lambda^m e^{-\lambda}}{m!}\ ,\ \lambda = N_0\rho_{\mathrm{D}j} \tag{7}$$

In Fig. 4, the result of a Monte Carlo simulation observing how many comparator offset voltages fall within the small V_{LSB} region is compared with (7). From this figure, we understand that the probability of finding no comparator offset voltage within V_{LSB} is almost 1 when the input voltage is too far from the mean offset voltage (0 V). This marks the range of a stochastic ADC. Later, we will calculate the yield of a calibrated stochastic ADC from this result.

As many comparators may fall within the target V_{LSB} region, we can define another term called "effective resolution, $V_{\mathrm{eff.}}$" that stands for the difference in offset voltages of two adjacent comparators. We can find the probability density function of the effective resolution from the PDF of the number of comparator offset voltages lying within V_{LSB}. All we need to do is to divide V_{LSB} with the number of comparators m in this region. Hence, the probability of observing an effective resolution of $V_{\mathrm{eff.}} = \frac{V_{\mathrm{LSB}}}{m}$ is given by $P_{\mathrm{eff.}j}[V_{\mathrm{eff.}} = \frac{V_{\mathrm{LSB}}}{m}]$ as follows where $m = [0, N_0]$.

$$\begin{aligned} P_{\mathrm{eff.}j}[V_{\mathrm{eff.}} = \frac{V_{\mathrm{LSB}}}{m}] &= \frac{N_0!}{m!(N_0-m)!}(\rho_{\mathrm{D}j})^m(1-\rho_{\mathrm{D}j})^{N_0-m} \\ &= \frac{\lambda^m e^{-\lambda}}{m!}\ ,\ \lambda = N_0\rho_{\mathrm{D}j} \end{aligned} \tag{8}$$

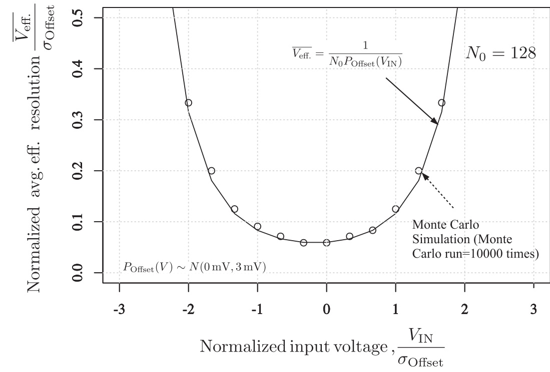


Fig. 6: Average effective resolution in terms of input voltage. Real line is from (8) and the points represent Monte Carlo simulation.

Although effective resolution is a continuous value, we observe it as a discrete value here because our observation itself is discrete, which has a step equal to the value of V_{LSB}. This would correspond to the resolution of the Digital-to-Analog Converter (DAC) used for measuring the stochastic ADC circuit. In Fig. 5, a Monte Carlo simulation result is compared to (8). As the solid lines that show the difference between the theory and the simulation are invisible, it is clear that (8) accurately predicts the probability density function of effective resolution. In fact, as (8) describes a *Poisson* distribution, the average effective resolution $\overline{V_{\mathrm{eff.}}}$, which is defined as the V_{LSB} that contains only 1 comparator on an average, is represented by the ridge line of Fig.5. From the definition ($\lambda = N_0\rho_{\mathrm{D}j} = 1$), we can find the expression for average effective resolution.

$$\overline{V_{\mathrm{eff.}}} = \frac{1}{N_0 P_{\mathrm{Offset}}(V_{\mathrm{IN}})} \tag{9}$$

A Monte Carlo simulation verifying (9) is shown in Fig. 6. For a *Gaussian* offset voltage distribution as given in (1),

the average effective resolution at the mean offset voltage, $\overline{V_{\text{eff.}}}|_{V_{\text{IN}}=\mu_{\text{Offset}}}$ is given below. This equation conforms to the previous reports of stochastic ADC resolution near the mean offset voltage [9]. (9) is a more general expression of it, which actually is the average value of the probability density function described in (8).

$$\overline{V_{\text{eff.}}}|_{V_{\text{IN}}=\mu_{\text{Offset}}} = \frac{\sqrt{2\pi}\sigma_{\text{Offset}}}{N_0} \tag{10}$$

C. Yield

Yield of an ADC describes the probability that the ADC would be capable of measuring the analog input signal with a resolution defined by the measurement range and the effective number of bit. Mathematically, yield is expressed as the probability that $-\frac{V_{\text{LSB}}}{2} < \text{INL}_j < \frac{V_{\text{LSB}}}{2}$ holds at all points within the measurement range.

Yield Without Calibration: A stochastic ADC without calibration uses the comparator offset CDF as a transfer curve to measure the input voltage. To calculate the yield of a non-calibrating stochastic comparator . We assume that r_j is the corresponding output code for input voltage $V_{\text{IN}j}$ and $r_{\text{Upper}j}$, $r_{\text{Lower}j}$ are the upper and the lower limits of the output code corresponding to the $\pm\frac{\text{LSB}}{2}$ limit of INL_j.

$$r_{\text{Upper}_j} = \lfloor N_0 \int_{-\infty}^{V_{\text{IN}j}+\frac{V_{\text{LSB}}}{2}} P_{\text{Offset}}(V)dV \rfloor \tag{11}$$

$$r_{\text{Lower}_j} = \lceil N_0 \int_{-\infty}^{V_{\text{IN}j}-\frac{V_{\text{LSB}}}{2}} P_{\text{Offset}}(V)dV \rceil \tag{12}$$

The probability $Y_{\text{NC}j}$ of meeting this INL condition at an analog step j is computed as follows.

$$\begin{aligned} Y_{\text{NC}j} &= P_{\text{INL}j}\left(-\frac{V_{\text{LSB}}}{2} < \text{INL}_j < \frac{V_{\text{LSB}}}{2}\right) \\ &= P_{\text{INL}j}\left(r_{\text{Lower}_j} \le r_j \le r_{\text{Upper}_j}\right) \\ &= \sum_{r_j=r_{\text{Lower}_j}}^{r_{\text{Upper}_j}} \binom{N_0}{r_j} \rho_{\text{C}j}^{r_j}(1-\rho_{\text{C}j})^{N_0-r_j} \end{aligned} \tag{13}$$

Here, the probability of output code r_j is calculated from (3). Next, we use an approximation here by assuming that each analog step j is independent of each other, ignoring their correlations. Otherwise, this equation becomes analytically intractable. As will be shown later, Monte Carlo Simulation shows that this approximation does not sacrifice the yield prediction accuracy for practical ADC designs. The total yield Y_{NC} can now be calculated by multiplying $Y_{\text{NC}j}$ at each step for the whole measurement range $2V_{\text{R}}$.

$$Y_{\text{NC}} = \prod_{j=1}^{n} Y_{\text{NC}j},\ n = \frac{2V_{\text{R}}}{V_{\text{LSB}}} \tag{14}$$

To see how well these equations predict the yield, Monte Carlo simulation of a stochastic ADC with a *Gaussian* offset distribution has been done and the result is summarized in

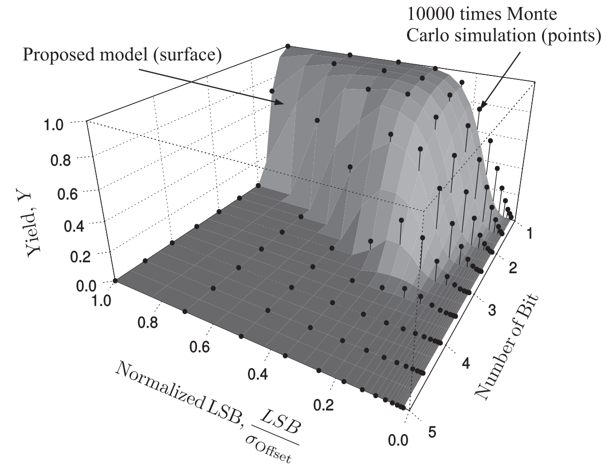


Fig. 7: Yield of a Stochastic ADC without calibration in terms of NOB and LSB. Gray surface stands for (14) and the points represent Monte Carlo simulation result. Error in (14) due to correlations among the analog steps is shown by the solid lines.

Fig. 7. We understand from this figure that the method of ignoring correlations between the small $V_{\text{LSB}} = 1\,\text{LSB}$ analog steps produces the same result as Monte Carlo simulation when yield, $Y > 0.8$, which is a reasonable situation for practical ADC designs.

Yield with Calibration: To calibrate a stochastic ADC, we use a known analog signal to map the ADC output code in a memory. Later, this mapped code is used instead of the comparator offset CDF to measure an unknown input voltage. Calculating the yield of a stochastic ADC with calibration is relatively complicated. Instead of calculating the probability of $P_{\text{INL}j}\left(-\frac{V_{\text{LSB}}}{2} < \text{INL}_j < \frac{V_{\text{LSB}}}{2}\right)$ directly, we will find the probability that "at least 1 comparator lies within $V_{\text{LSB}} = 1\,\text{LSB}$ throughout the measurement range." As the probability of having m_j comparator offsets within V_{LSB} at an input voltage $V_{\text{IN}j}$ is known from (7), we can calculate the total yield Y_{C} of a calibrated stochastic ADC as follows.

$$Y_{\text{C}} = \prod_{j=1}^{n} Y_{\text{C}j},\ n = \frac{2V_{\text{R}}}{V_{\text{LSB}}}\,, \tag{15}$$

$$\begin{aligned} \text{where}\quad Y_{\text{C}j} &= P_{\text{Comp}j}(m_j > 1) = P_j(m_j \neq 0) \\ &= 1 - P_{\text{Comp}j}(m = 0) \\ &= 1 - (1-\rho_{\text{D}j})^{N_0} = 1 - e^{N_0\rho_{\text{D}j}} \end{aligned} \tag{16}$$

In (15), we have ignored the correlations among the different j analog steps, treating them as independent from each other. For a calibrated stochastic ADC, the probability of having "at least 1 comparator" is equivalent to the probability of having an INL within $\pm\frac{\text{LSB}}{2}$ because this would ensure that there is a change in the ADC output code in the $\pm\frac{\text{LSB}}{2}$ range. A Monte Carlo simulation calculating the probability of meeting this condition is performed assuming a *Gaussian* offset distribution. The result is plotted in Fig. 8 together with the predicted value given by (15). From Fig. 8, we can understand that ignoring

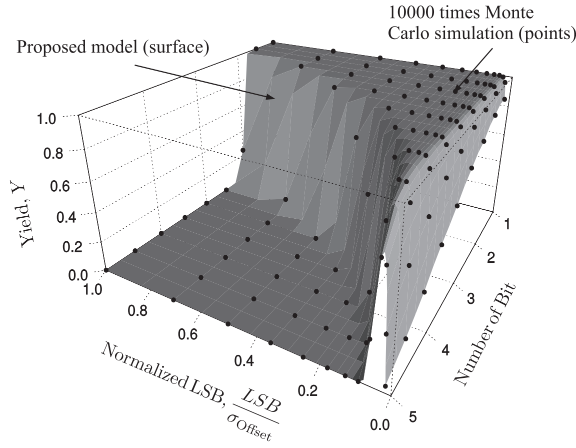


Fig. 8: Yield of a Stochastic ADC with calibration in terms of NOB and LSB. Gray surface is from (15) and the points represent Monte Carlo simulation result. Solid lines showing the error are invisible.

the correlations among the analog steps at different input voltages $V_{\mathrm{IN}j}$ does not affect the predicted result that much as in Fig. 7. One reason for this is that we are calculating the probability of "having at least 1 comparator," which has a very low correlation compared to the case of without-calibration where we have to calculate the probability of "the output code falling within $\pm\frac{\mathrm{LSB}}{2}$ range."

III. Application Example of Sub-ranging ADC Design Optimization

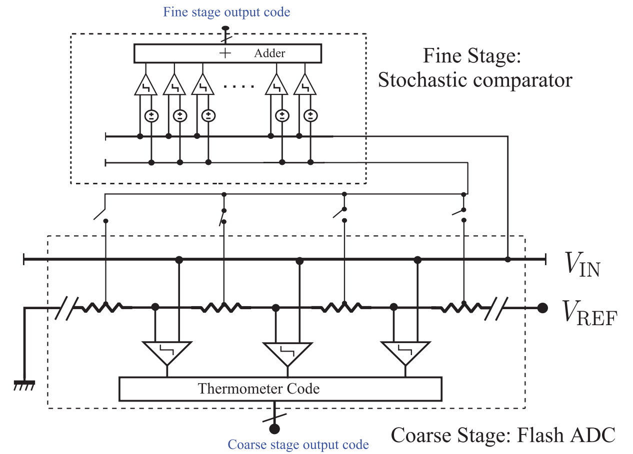
Stochastic ADC can realize extremely fine resolution, but its measurement range is limited by the spread of the offset voltage distribution. To increase the measurement range, a sub-ranging ADC architecture that uses a combination of the conventional and the stochastic ADCs can be used. The conventional deterministic ADC is used as the first stage to narrow down the input voltage. Then the second stage implements the stochastic part, which may have a *Gaussian* offset distribution or a more uniformly distributed offset configuration. We will refer to the stochastic ADC as "stochastic comparator" while it is used in a sub-ranging ADC. A basic example of such sub-ranging ADC architectures is shown in Fig. 9. Here, a conventional flash ADC architecture is used in the first stage and stochastic comparator with a *Gaussian* offset distribution is used in the second stage.

A. Total Yield as the Objective Function for Optimization

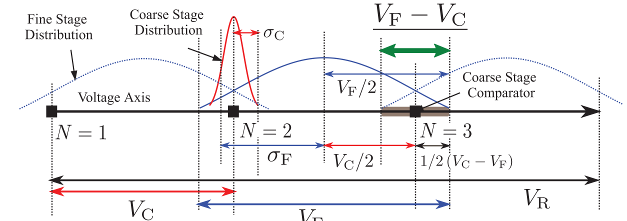
The total yield of a sub-ranging ADC with a calibrated stochastic comparator is given as follows.

$$Y_{\mathrm{SR}} = \left[\mathrm{erf}\left(\frac{(V_{\mathrm{F}}-V_{\mathrm{C}})}{k}\sqrt{\frac{(A_{\mathrm{T}}-A_{\mathrm{FT}})}{2(V_{\mathrm{R}}/V_{\mathrm{C}}-1)}}\right)\right]^{V_{\mathrm{R}}/V_{\mathrm{C}}-1} \times \prod_{j=1}^{n}\left(1-e^{N_0\rho_{\mathrm{D}j}}\right),\ n=\frac{2V_{\mathrm{F}}}{V_{\mathrm{LSB}}} \quad (17)$$

Here, A_{T} is the total area of all the comparators in a sub-ranging ADC. The area of resistor ladders and adders are not considered for optimization. A_{FT} is the total stochastic comparator area, V_{R} is the total measurement range, V_{F} is the stochastic measurement range, V_{LSB} is the stochastic comparator LSB defined by the ADC NOB, V_{C} is the coarse stage ADC LSB, A_{F} is the area of a unit comparator and k is a constant from (2). $\rho_{\mathrm{D}j}$ is calculated from (6). The first part in the equation is the yield of the coarse stage flash ADC and the second part is for the fine stage stochastic comparator. We have used (2) to account for the change in the offset voltage standard deviation due to an adjustment in a comparator circuit area [8]. From the relative distributions of the coarse and the fine stages comparator offsets, we find that all the comparator offsets of the coarse stages must fall within the $\pm\frac{V_{\mathrm{F}}-V_{\mathrm{C}}}{2}$ region as shown by the green arrow in Fig. 9-(b) rather than the conventional $\pm\frac{\mathrm{LSB}}{2}$ region. Otherwise, an error in the coarse stage would be left uncorrected by the fine stage. We can also calculate a similar total yield function for a sub-ranging ADC when the stochastic comparator is used without calibration. Only the second part of (17) will be replaced by (14) to account for the change in the fine stage architecture. The important thing to notice in (17) is that the total yield has a maximum point in terms of parameters like the total stochastic comparator area A_{FT}, stochastic measurement range V_{F}, etc. Hence, we can use the total yield of a sub-ranging ADC as an objective function for optimization. When optimization is done under a constant total comparator area condition, V_{F} and V_{C} should not be considered independent. Rather, their ratio



(a) Sub-ranging ADC architecture



(b) Relative offset distributions of fine and coarse stage comparators

Fig. 9: Sub-ranging ADC architecture includes a conventional flash ADC coarse stage and a stochastic ADC fine stage.

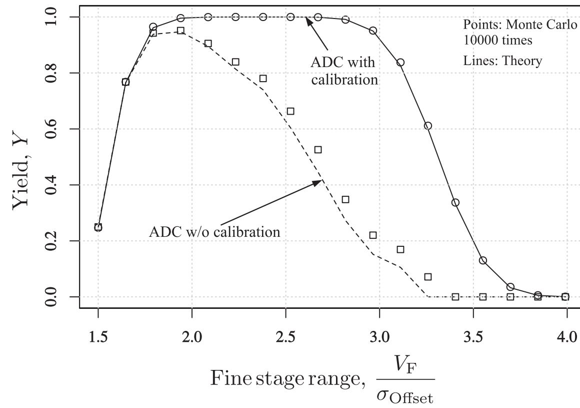


Fig. 10: Yield of a sub-ranging ADC in terms of fine stage range V_F. The lines are the predicted values and the dots represent Monte Carlo simulation. The area of the Stochastic comparator is 1500 units.

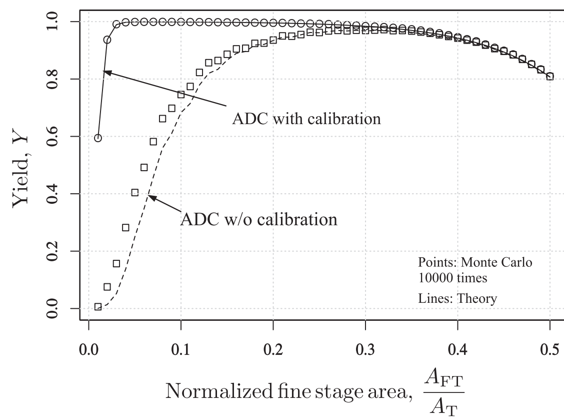


Fig. 11: Yield of a sub-ranging ADC and fine stage total area A_{FT}. The lines are predicted values and the dots are MC simulation results.

$\frac{V_F}{V_C}$ should be treated as a new parameter. Otherwise, changing the area of one stage would not influence the required area of the other stage under the same chip yield. The yield is also maximum when the smallest possible unit comparator is used.

B. Comparison with Monte Carlo Simulation

We have calculated the yield of both a calibrated and a non-calibrated sub-ranging ADC with a measurement range of 1.8 V and a resolution of 11 bits. The total area of the circuit is fixed at 7000 times of the unit comparator area and the offset voltage standard deviation σ_{Offset} of a unit comparator is assumed to be 3 mV. The total yield function for both the cases have been verified by comparing it with a 10000 time Monte Carlo simulation. The result is summarized in Figs. 10 and 11. Fig. 10 compares the total yield of a sub-ranging ADC when the fine stage measurement range V_F is changed. Fig. 11 compares the total yield function when the fine stage total area A_{FT} is changed. From these figures, it is evident that the equations developed here accurately predict the total yield of a sub-ranging ADC when $Y > 0.8$. The equations have little discrepancies compared to the Monte Carlo simulation results when the total yield is less than 0.8 ($Y \leq 0.8$). But this region of yield is anyway not useful when a practical system is considered, hence this is not an issue. It is also clear that the maximum yield point exists in terms of ADC design parameters. We can now use the values of different parameters in (17) and calculate the total yield. By solving the maximum value problem of this non-linear equation, we can find the optimal design parameters of a sub-ranging ADC.

IV. CONCLUSION

Sub-ranging ADC based on stochastic comparator can realize a wide measurement range with fine resolution while being robust to process variation. We have formulated a rigorous Probability Density Function to describe the effective resolution of a stochastic comparator. From this model, we can approximate the yield of a stochastic comparator and the total yield of a sub-ranging ADC. We have shown that the total yield function can be used as an objective function for optimizing the design parameters for a well balanced sub-ranging ADC. We have verified our calculations by performing Monte Carlo simulations and comparing the results. Our future work includes the analysis and optimization of some different types of stochastic ADCs that use non-*Gaussian* offset voltage distributions, e.g. a more uniformly distributed offsets using comparators with shifted reference voltages. In addition, dynamic noise contributions will be take into account to make the proposed model a comprehensive optimization method for practical sub-ranging ADC designs.

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