# RT Level Timing Modeling for Aging Prediction

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***Abstract*—The simulation of aging related degradation mechanisms is a challenging task for timing and reliability estimations during all design phases of digital systems. Some good approaches towards accurate, efficient and applicable timing models at the register transfer level (RTL) have already been made. However recent state-of-the-art models often have to access lower levels of abstraction, such as the underlying gate-level netlist for each timing estimation and require to repeat every analyzing step if parameters, input signals or designs are changed.**
**This work introduces a new RTL timing model concept that provides a separation of design analysis and aging estimation. It allows more efficient design evaluations with respect to aging. Although this is work in progress and systematic evaluations are still ongoing, early results indicate the applicability and capability of the approach to compete with recent models both in accuracy and efficiency.**

***Keywords*—Register Transfer Level, Timing Analysis, Aging Prediction, Separation, NBTI, Negative Bias Temperature Instability, Reliability**

## I. Introduction

Accounting for parameter variations is an important task in the design process of digital circuits to ensure their reliability. While the effect of variations in the manufacturing process and the operational environment are well known and controllable by introducing process corner cases and specifying operation ranges, the handling of variations introduced by aging effects is more challenging. When caused by negativ bias temperature instability (NBTI), aging leads to threshold voltage degradations within the PMOS transistors of the circuit which eventually lead to performance degradation and operational faults. The underlying physical mechanisms are well understood and can be simulated at transistor level [1], [2]. However most systems today are designed at RT-level or higher. At these levels of abstraction, transistor level aging simulations are virtually impossible due to the immense number of transistors. The introduction of safety margins ensuring a fault free operation is no good option either, as it reduces the advantages of moving to the next technology node.
Thus an RT-level aging model is needed which allows accurate and efficient aged timing estimation. This work presents a new RTL timing model that provides a separation of design analysis and aging estimation. Although the current model accounts only for NBTI, it should be easily adaptable to other timing altering aging effects like hot carrier degradation (HCD) and positive bias temperature instability (PBTI).
The remainder of this paper is structured as follows: The next section, provides an overview of the related work. Afterwards the model is presented in section III the results of the evaluation and the used methods are presented in section IV. The work is finally concluded in section V, which also provides an outlook.

## II. Related Work

NBTI causes a time dependent threshold voltage shift in PMOS transistors, leading to increasing switching delays and can therefor cause major problems in digital circuit timing.
At **transistor level** NBTI has long been modeled by so called reaction defusion models. Recently this paradigm has changed [2], and a two stage model [1], [3] was introduced. The two stage model suggests that defects (imperfections) within the silicon layer of a PMOS transistor can get charged with individual probabilities under stress, by emitting an electron. Depending on the used silicon technology up to a few thousand defects exist in a single transistor. The individual charge probabilities lead to different ”activation” times of the defects, causing a time dependent accumulation of positive charge resulting in a threshold voltage degradation of the PMOS. As the electrons can partially return when the stress is removed, the PMOS can partially recover with their individual relaxation times.
At **gate level** the findings of [4] however suggest that the non-aged delay between any gate inputs to one gate output can be described as an affine projection of the delay of an inverter. The equivilant network, to determine the delay, consists of one NMOS and one PMOS on the switching path. The other transistors of the gate are replaced by capacities and resistances. This abstraction will be used in this work, as well as for the gate level NBTI model [5] utilized by this work. The model presented in [5] utilizes [4] by suggesting, that it is enough to age one PMOS in each possible gate path (from an input to an output). The defects (or so called traps) are abstracted as capture/emission time maps like introduced in [2]. This allows to represent complex aging patterns by a few geometrical parameters instead of accounting for all traps individually.
Another **gate level** approach is presented in [6] and optimized to be efficiently applicable at **RT-level** in [7]. The circuits timing is analyzed by extracting the critical paths via static timing analysis (STA) and estimating the delay for each gate along the path. The optimization introduced in [7] reduces the number of paths to account for by evaluating them based on non-aged and worst case aged timing. The model introduced in [8] annotates duty cycles to each transistor in the RTL netlist and determines their individual threshold voltage degradation by a long term aging model. These voltage shifts are then used to determine the timing for each gate, using a gate level timing

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library. In a final step a STA is performed with the aged timing values to extract the critical path.
In contrast to the present work both models require to repeat all steps if only a single evaluation parameter is changed, do not utilize complex temperature and supply voltage profiles to determine the threshold voltage damages and have to access all the abstraction layers below RTL to calculate the aged delay estimation. So the models can be used for aging estimation at RT-level, but they are no pure RTL models.

## III. RTL-Timing Model

The model presented in this section was developed to enable timing analyzes of aged digital circuits at RTL. Analogue to the representation of a non-aged gate delay by an inverter delay from [4], the aged delay of an entire RT-component is represented by a affine combination of representative aged inverter delay function.

### A. Mathematical Description of the Appraoch

Starting from the results of [4] already discussed in section II (gate delay representation as affine projection of inverter delay), the **delay** $d_{GT}$ between any input and any output of a gate can be described as function of the **threshold voltage** $v_{th}$ of the PMOS transistor on that path, the input **slew rate** $Sr$ and the driven load **capacity** $C$.
We introduce aging, for the time being assumed to be exclusively caused by NBTI, in the form of PMOS threshold voltage $v_{th}$ degradation. This causes the threshold voltage $v_{th}$ to be a function of **lifetime** $t$, the input **signal probability** $P_{\mathtt{sig}}$ *(respectively duty cycle)*, the **temperature profile** $T(t)$ and the **supply voltage profile** $V_{dd}(t)$. Applying $v_{th}$ to the gate delay $d_{GT}$ and representing it as linear combination of aged inverter delay functions leads to (1) and (2). For this representation second order effects like the dependency of the slew rate on the threshold voltage were neglected.

$$d_{\mathrm{GT}}\Big(t\Big) = d_{\mathrm{GT}}\Big(v_{th}\left(t, T(t), V_{dd}(t), P_{\mathrm{sig}}\right), Sr, C\Big) \quad (1)$$

$$\approx \sum_{i,j,k}\Big(a_{i,j,k,\mathrm{GT}} \cdot d_{\mathrm{INV}}\big(t,i,j,k\big)\Big) \quad (2)$$

with

$$a_{i,j,k,\mathrm{GT}} := a_{\mathrm{GT}}\big(\left(P_{\mathrm{sig}}\right)_i, Sr_j, C_k\big) \quad (3)$$

$$d_{\mathrm{INV}}\big(t,i,j,k\big) := d_{\mathrm{INV}}\big(v_{th}\left(t, \left(P_{\mathrm{sig}}\right)_i\right), Sr_j, C_k\big) \quad (4)$$

The **coefficients** $a_{i,j,k,\mathrm{GT}}$ and the corresponding **inverter delay functions** $d_{\mathrm{INV}}(t,i,j,k)$ utilized in (2) are defined in (3) and (4). Both are depending on discrete basic values of $1 \leq i \leq I$ signal probabilities $(P_{\mathrm{sig}})_i$, $1 \leq j \leq J$ slew rates $Sr_j$ and $1 \leq k \leq K$ driven capacities $C_k$. The number of basic inverter delay functions needed to represent the gate delay is simply the product of $I$, $J$, and $K$. The signal probabilities are for now assumed to be static over the lifetime, resulting in only the inverter delay functions to be time dependent. As a result of that, the dynamic aging behavior is only encoded within the basic inverter delay functions, while the design dependencies *(so far only the gate type)* of the delays are encoded within the coefficients when this form of representation is chosen.
What first seems to be an overhead, becomes an advantage when *extending this approach to RTL*. An **aged path delay** $D_{\mathrm{PTH}}(t)$ between an input and an output of any RT-component, can be described as the sum of the gate delays along that path as shown in (5). Due to the small spatial distribution of the component, the temperature profile $T(t)$ and supply voltage profile $V_{dd}(t)$ is can be *assumed equal* for all gates along the path. This ensures that identical basic inverter delay functions are utilized for the representation of all gates when applying the representation from (2). With that the **N gate coefficients** $a_{i,j,k}$ corresponding to one particular inverter delay function can be summed up to **path coefficients** $A_{i,j,k}$ as shown in the transition from (6) to (7).

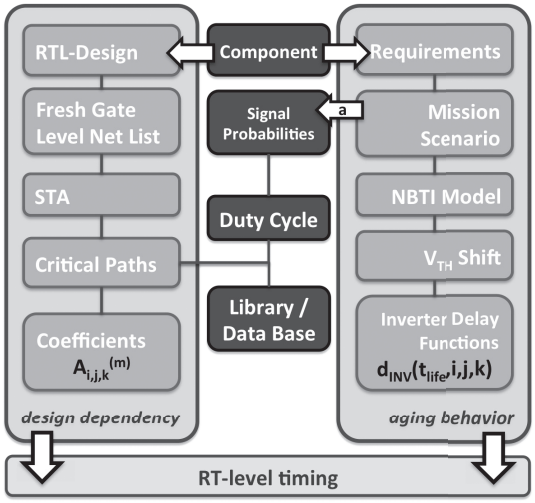


Fig. 1. **Schematic representation of the RT-level timing model flow** with separation of design dependency and aging behavior. The left-hand box displays the steps to extract the design dependency representing coefficients from the systems RTL-desing. The right-hand box displays the steps to extract the aging behavior representing inverter delay functions from the mission scenario, respectively the systems requirements. The RTL timing analysis is conducted by combining the coefficients and the corresponding inverter delay functions.

$$D_{\mathrm{PTH}}\big(t\big) = \sum_{l=1}^{N}\left(d_{\mathrm{GT}\,(l)}\left(v_{th}\left(T, P_{\mathrm{sig}}\right), Sr, C\right)\right) \quad (5)$$

$$= \sum_{l=1}^{N}\left(\sum_{i,j,k}\left(a_{i,j,k,\mathrm{GT}\,(1)} \cdot d_{\mathrm{INV}}\big(t,i,j,k\big)\right)\right) \quad (6)$$

$$=: \sum_{i,j,k}\left(A_{i,j,k} \cdot d_{\mathrm{INV}}\Big(t,i,j,k\Big)\right) \quad (7)$$

The **delay** of an **entire component** can now be defined, as the **maximum delay** of **all** possible **path delays** as in (8).

$$D_{\mathrm{RT}}(t) = \max_{1\leq m\leq M}\left(\sum_{i,j,k}\left(A_{i,j,k}^{(m)} \cdot d_{\mathrm{INV}}\Big(t,i,j,k\Big)\right)\right) \quad (8)$$

To reduce the effort one should perform a **static timing analysis (STA)** to reduce the number of paths before applying the model. Note that there is no particular critical path, but a lifetime dependent component delay. Which path exactly causes the component delay is irrelevant as it is defined as a time dependent maximum of path delays (8). This approach supports to account for switching critical paths by design. Also note that the separation between static design dependencies and dynamic aging behavior is still intact.

### B. Model Flow

In order to extract the coefficients $A_{i,j,k}$ of RT-Components and to calculate the basic inverter delay

functions $d_{\mathrm{INV}}(t,i,j,k)$ the model uses the flow which is described below and displayed in Figure 1.

Starting with the **determination** the **basic inverter delay functions**, shown on the right hand side of Figure 1 the requirements of the component are defined by the expected application. The expected application (e.g. component is part of cell phone, automotive, interstellar probe, ...) defines the **mission scenario**, which can be very divergent for different applications. The **mission scenario** contains the ambient **temperature profiles**, the **supply voltage profiles**, idle and power-down times and, if they are known, specific **input signal probabilities**. The **input signal probability** is defined as the probability that a digital "1" occurs at the corresponding input of the component. They determine the duty cycles of the gates PMOS which can be calculated by logical analysis. The **NBTI model** from [5] is then applied to $I$ basic inverters with different signal probabilities for the described mission scenario to extract the corresponding threshold voltage degradation. The extraction is done for $N$ discrete time steps. In the final step the $N$ threshold voltage shifts for each of the $I$ signal probabilities are applied to a basic inverter and the delay is determined for $J$ slew rates and $K$ driven capacities. A function is then fitted to the $N$ values for each of the $I \cdot J \cdot K$ possible parameter combinations. Now all inverter delay functions are determined for that specific mission scenario. There is no dependency of the delay functions, and therefore the ***aging behavior*** on the design of the RT-component.

To perform the **coefficient extraction**, shown on the left hand side of Figure 1, the RT-component is first analyzed by state-of-the-art software tools. The **RTL design** is used to synthesize the **fresh** (non-aged) **gate level net list** of the circuit. After that a **static timing analysis (STA)** is performed to extract paths with critical timing. The **critical paths** are now available as complete gate level net lists, with corresponding slew rates and driven capacities. As described in section III-A, aging and therefore **delay degradation** along the **path** only depends on the **gate types** and **duty cycle**, as temperature profiles and supply voltage profiles are the same for all gates. To annotate the **duty cycles** to the gates, input signals with generic statistics are applied to the component and a logic analysis is performed. Generic signals can be used as for the common case the exact input signals are unknown during the design phase. With gate types, capacities, slew rates and duty cycles now known, the gates can be represented as in (2). For that purpose the gate's delay functions are fitted to the basic inverter functions for a generic mission scenario. This implies the assumption, which has yet to be shown, that the gate level coefficients are independent to the mission scenario. Anyhow this is a reasonable assumption as the basic inverters always suffer the same mission scenario as the gates they represent. This assumption also allows to build up a **data base** from preliminary analyzed gate coefficients which depend only on duty cycle and gate type. With that gate representations can simply been looked up. In the finals step the gate coefficients of every path are **summed** up by their corresponding inverter functions. The result is the **M sets of path coefficient** $A_{i,j,k}^{(m)}$ from (8).

With the assumptions allowing utilization of generic mission scenarios to determine the gate level coefficients and generic input signals to calculate the annotated duty cycles, one could state that the coefficients exclusively ***depend on the components design***.
However, sometimes the application determines a very specific input signal pattern, e.g. if the component is part of a counter. In that case, the specific signal probabilities (arrow (a) in Figure 1) can be used to improve the timing estimation, by adopting the coefficients to the specific component application. With both coefficients and delay functions finally calculated **RT-level timing analyses** can be performed.

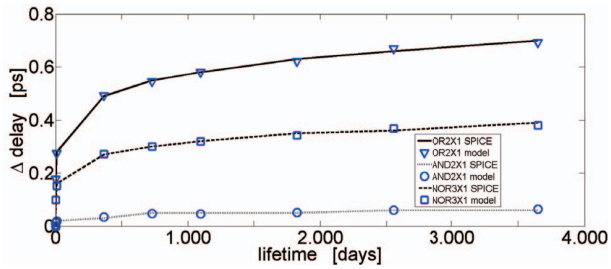


Fig. 2. **Modelling gate delay increase over lifetime**. SPICE measured delays and their corresponding model estimated delays of three gates. AND2X1: Duty cycle = 0.03, driven capacity = 1.6638 fF, RMS = 0.27%; NOR3X1: Duty cycle = 0.5, driven capacity = 1.7145 fF, RMS = 0.53%; OR2X1: Duty cycle = 0.97, driven capacity = 1.7002 fF, RMS = 0.53%;

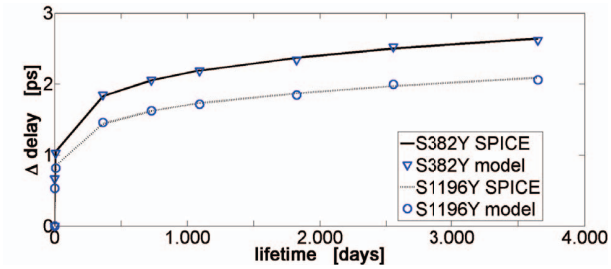


Fig. 3. **Modelling path delay increase over lifetime**. SPICE measured delays and their corresponding model estimated delays of paths extracted from S382Y and S1196Y circiut (ISCAS89 benchmark circuits). S382Y: RMS = 1.79%, driven capacity = 1.7002 fF; S1196Y: RMS = 1.92%, driven capacity = 1.7002 fF. It was assumed that both paths would drive an inverter.

## IV. Evaluation and Results

The described model flow has yet to be automatized. Hence, the transition from step to step during the model's evaluation was partially done manually and/or altered w.l.o.g.

### A. Evaluation

To prove the models concept two tests have been conducted. To simplify the tests, the basic inverter functions were limited to $I = 4$ duty cycles $\{0, 0.1, 0.9, 1\}$, $J = 1$ slew rate $\{0.041\mathrm{ns}\}$ and $K = 1$ capacity $\{3.7556\mathrm{fF}\}$. Furthermore the wire loads of the circuits were neglected and the mission scenario utilized to calculate the duty cycle dependent threshold voltage degradation [5] has been kept simple. It was chosen to have constant temperature $T = 398\mathrm{K}$ and constant supply voltage $1.25\mathrm{V}$ over the entire lifetime. As time steps the following values have been chosen: time steps $\{1\mathrm{d}, 365\mathrm{d}, 730\mathrm{d}, 1095\mathrm{d}, 1825\mathrm{d}\, 2555\mathrm{d}, 3650\mathrm{d}\}$. The tests were

conducted with 65nm technology. To create realistic input slopes, every analyzed circuit (single gates or paths) was extended by three inverters at the switching input.
As preparation each basic inverter was implemented in the SPICE circuit simulator utilizing the BSIM 4.7 MOSFET model and delays were measured for each threshold voltage damage calculated by [5].
After that the **first test** was conducted by implementing individual gates in SPICE, with individual driven capacities, duty cycles were assigned and their delays were measured for each threshold voltage degradation, to calculate reference values. To extract model coefficients a linear regression was performed with MATLAB to map the gate delays to the basic inverter delay functions. In the **second test** a critical path from the *ISCAS89 Benchmark circuits* S382Y and S1196Y each was analyzed analogue to the single gates. To extract the critical path state-of-the-art synthesis tools were used and a STA was performed. After that, the paths were implemented in SPICE and duty cycles were assigned to each gate on the path together with their corresponding threshold voltage degradation manually. Finally the path delays were measured and a linear regression was performed with MATLAB to determine the model coefficients for the path, so that the path delays were mapped to the basic inverter delay functions. This is not yet the bottom up approach described in III-B, where the path delays is the sum of the gate delays.

### B. Results

Figure 2 shows the delay increase over lifetime of three gates from for one particular duty cycle each and their corresponding inverter delay representations. The representations show an overall maximum RMS of 0.53%.
Figure 3 shows the delay increase over lifetime for each of the two paths from S382Y and S1196Y and their corresponding inverter delay representations. The representations show an overall RMS of 1.79% and 1.92%.

## V. Conclusion

Although systematic evaluations of the model still have to prove the competitiveness with respect to the state-of-the-art approaches, the independence of the model coefficients to the mission scenarios and that the path delay coefficients are the sum of the gate delay coefficients, this work suggests that the aged delay of an critical path of an RT Component can be described accurately as linear combination of aged basic inverter delays. This leads to the conclusion that the modeling approach is correct and a separation between design dependencies and aging behavior is possible at register transfer level. Although the evaluation was carried out at 65nm technology which is not very prone to the NBTI-effect and therefore only suffers a maximum delay increase of approximately 5% the model should perform equally good at technology nodes below 65nm. At 15nm NBTI can cause threshold voltage damages two magnitudes larger than those at 65nm.

### A. Outlook

As the included NBTI model supports complex mission scenarios, the RTL timing model should allow for an impact evaluation of sophisticated and realistic aging scenarios on the aged timing behavior.
The dependencies of every gate's delay to driven capacity, slew rate and threshold voltage degradation are all strictly increasing. That indicates a proportional dependency between the path representing coefficients $A_{ijk}$ and the corresponding path delays as well, allowing the application of a Pareto front analysis to reduce the number of paths needed to be considered for the timing analysis. This could significantly boost the model's efficiency.
Since the entire approach is capable of representing design dependencies and complex aged timing behaviors individually and relatively compact, the model should be extendable to a black box RTL timing model allowing to combine individually analyzed aging scenarios and designs. This would allow the designer to stay at RTL if the needed or similar scenarios and designs, or similar ones have already been analyzed individually before.
Similar to NBTI, hot carrier degradation (HCD effects NMOS and PMOS) and positive bias temperature instability (PBTI effects NMOS) also leads to threshold voltage shifts over circuit life time. As the model is designed to map delays to these voltages shifts, it should easily be adaptable to support HCD and PBTI.
The initial test showcased a significant dependency of the input slope type (rising or falling slope) to the aged delay, which should be explored further in future evaluations.

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