Enabling Simultaneously Bi-Directional TSV Signaling for Energy and Area Efficient 3D-ICs

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***Abstract*—This paper presents an analytic and experimental study on a simultaneously bi-directional (SBD) TSV interconnect capable of energy and area efficient 3D-IC vertical signaling. We first explore TSV channel characteristics that differ from well-known off-chip channel properties, then analyze circuit design tradeoffs for SBD TSV signaling in terms of energy, bandwidth and noise margin. Based on this analysis, we propose a novel SBD TSV signaling circuit optimized for our system-level design goals and given TSV technology. Measurement results on a 28nm CMOS test chip show that the proposed SBD TSV interconnect enables 10.3−31.1% lower energy at 34.4% less area than two equivalent uni-directional TSVs. Although our single SBD TSV has 12.5% lower bandwidth than two uni-directional TSVs, the SBD TSV can support up to 9.1Gb/s/TSV bi-directional signaling (*i.e.* 4.55GHz maximum clock speed) at 1.05V.**

I. Introduction

Three-dimensional integrated circuits (3D-ICs) have emerged as an appealing alternative to planar 2D counterparts since 3D-ICs provide higher die-to-die bandwidth, smaller form factor and heterogeneous die integration. The heart of such 3D-ICs is a through silicon via (TSV)[1] that cuts across thinned silicon substrates to offer inter-die connectivity. In general, TSVs can provide two types of 3D vertical signaling depending on die stacking topologies: face-to-face (F2F) and face-to-back (F2B). F2F TSVs feature lower signaling energy and delay due to smaller parasitic lumped capacitance than F2B TSVs, but support two-tier 3D-IC integration only. On the other hand, F2B TSVs allow for any multiple-tier 3D-IC integration, thus enabling scalable 3D-IC chip architectures.

Such scalable F2B TSVs, however, face the following design challenges. First, F2B TSVs consume substantial transmission energy due to their high parasitic capacitance, *e.g.* about 200fF/TSV in IBM technology [8] or 80−120fF/TSV in IMEC technology [13]. While F2B TSVs still hold an energy advantage over off-chip interconnects (typically on the order of tens of pF), F2B TSVs incur 10−20x higher parasitic capacitance than F2F TSVs [5], [10]. Second, F2B TSV landing pads occupy considerable silicon area, *e.g.* 7μm×7μm in Tezzaron TSV technology [10]. Lastly, current F2B TSV fabrication technologies impose non-negligible fault rates, leading to lower yield than standard 2D chip fabrication [9]. For reliable signaling, such low-yield 3D-IC chips require redundant TSVs such as spare TSV arrays [5], twin TSVs [6] or shared spare TSVs [4], thereby further exacerbating the energy and area overheads of F2B TSV interconnects.

[1]The semiconductor industry has developed 3D-ICs in many different technologies, leading to various definitions of 3D-ICs; wire-bonded 3D-ICs, microbump-only 3D-ICs, contactless (capacitive or inductive) 3D-ICs or TSV-based 3D-ICs. In this paper, we refer to the TSV-based chip cubes as 3D-ICs.

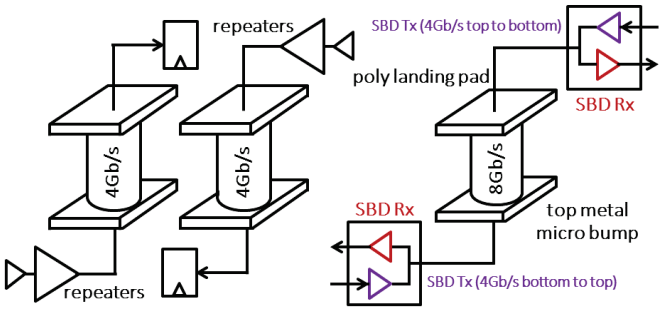

Fig. 1. Two uni-directional TSVs versus one simultaneously bi-directional (SBD) TSV operating at the same clock speed (4GHz in this example).

To tackle these challenges, we explore simultaneously bi-directional (SBD) signaling that can transmit and receive data at the same time though a single F2B TSV. Figure 1 shows the concept of such SBD signaling. When operating at the same clock speed, one SBD TSV delivers the same amount of data as two uni-directional TSVs. The reduced TSV counts through SBD signaling lead to less parasitic capacitance (hence lower dynamic energy) and smaller footprint.

Depending on the circuit design of a SBD transmitter (Tx) and a SBD receiver (Rx), the TSV signaling performance significantly varies in terms of energy, bandwidth and noise margin. This paper analyzes such performance tradeoffs, to help design a SBD TSV signaling circuit optimized for given system-level design goals and TSV technology. Then, as a case study, we present a novel SBD TSV signaling circuit. Since there have been no SBD signaling studies on a F2B TSV to the best of our knowledge, we demonstrate the functionality and performance of SBD TSV signaling through chip prototyping.

The rest of the paper is organized as follows: Section 2 analyzes TSV channel characteristics and circuit design tradeoffs for SBD TSV signaling. In Section 3, we first state our system-level design goals, then propose a SBD TSV link design optimized for such design goals and given TSV technology. Section 4 details experiment results on a test chip and Section 5 concludes this paper.

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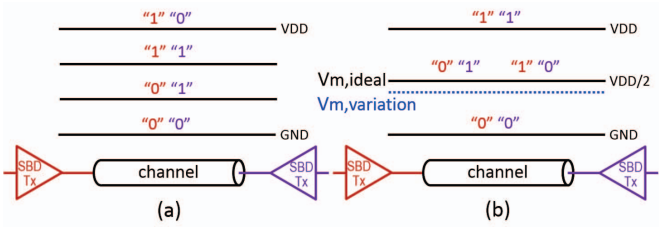

Fig. 2. Tradeoff between dynamic energy and noise margin: 4 voltage-level SBD signaling transmits bi-directional data with lower voltage swing than 3 voltage-level SBD signaling, resulting in less dynamic energy (advantage) and smaller noise margin (disadvantage).

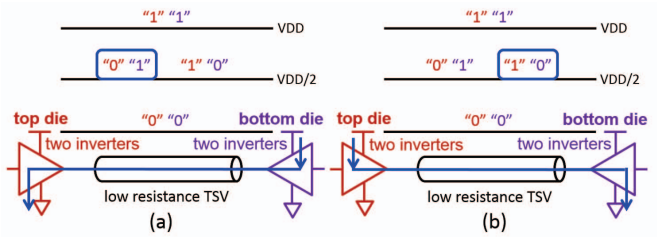

Fig. 3. Static die-to-die current paths through a *low resistance* TSV in SBD signaling.

II. Analysis: TSV Channel Characteristics and Design Tradeoffs

While there have been studies on off-chip (chip-to-chip) SBD signaling circuits [7], [11], [14], this work is arguably the first to explore SBD signaling on a F2B TSV whose channel characteristics are quite distinct from off-chip channels. Accordingly, a natural next step is to compare and analyze well-known off-chip links and TSV links. Here, we highlight the key differences:

- While off-chip links require accurate impedance matching, TSV signaling does not. This is because TSV transmission delay is generally negligible compared to the clock period. For instance, the IBM TSV interconnect can transmit 6Gb/s/TSV data without any impedance matching circuits [8].
- Unlike off-chip interconnects, TSV links do not need complicated, power-hungry equalization circuits since TSVs' RC constant is much smaller than that of off-chip links due to TSVs' negligible parasitic resistance.
- SBD TSV signaling circuit requires larger voltage step ratio (*i.e.* bigger noise margin ratio) between a power supply voltage and a ground voltage than off-chip counterparts, because the off-chip power rail is typically at 2.5V or 1.8V while the on-chip rail is powered at ∼1.0V. As shown in Figure 2, four voltage-level SBD signaling leads to 1/3 voltage noise margin ratio whereas three voltage-level SBD signaling has 1/2 noise margin ratio.
- Most importantly, SBD TSV signaling circuits should minimize inter-die static current flowing through a low resistance TSV when TSV voltage is driven to middle-level voltages *e.g.* bi-directional data 01 and 11 in Figure 2 (a), or bi-directional data 01 and 10 in Figure 2 (b). While the static current required for SBD signaling in off-chip links does not dissipate significant power due to their highly resistive channel, SBD TSV signaling can lead to substantial static current through a low resistance TSV. This will be explained in detail in Subsection II-B.

A. Dynamic energy versus noise margin

A straightforward implementation of 2-bit SBD signaling is to use four voltage levels between a power supply voltage (the highest voltage in a chip) and a ground voltage (the lowest voltage in a chip), mapping each of them to four possible SBD symbols. Figure 2 (a) shows such four voltage-level SBD signaling. An alternative is to share one voltage level between two SBD symbols [11], *e.g.* 01 and 10 as shown in Figure 2 (b). There exists an obvious tradeoff between these two schemes: Three voltage-level SBD signaling incurs higher voltage swing between adjacent SBD symbols than four voltage-level SBD signaling, thus consuming more dynamic energy with bigger noise margin. In other words, the bigger noise margin of three voltage-level SBD signaling is obtained at the cost of dynamic signaling energy. When a 3D-IC chip experiences little CMOS variation (*e.g.* mature CMOS technology nodes) or endures signaling errors to a certain degree through error-tolerant schemes (*e.g.* resilient NoCs [1], [2]), we can choose four voltage-level SBD signaling to further reduce dynamic energy. On the other hand, if a TSV signaling error is unacceptably expensive to detect and correct in a given system, or if a 3D-IC chip requires low voltage mode in a DVFS system, three voltage-level SBD signaling featured with bigger noise margin is preferred.

B. Static energy versus bandwidth

Figure 3 shows die-to-die static current paths in the three voltage-level SBD TSV where a TSV driver is implemented using a simple repeater (composed of two inverters). Once a top die driver transmits logic 0 with a pulled-down NMOS and a bottom die driver transmits logic 1 with a pulled-up PMOS, a static current path is formed from the bottom die PMOS through a TSV to the top die NMOS. Similarly, when a top die driver transmits logic 1 and a bottom die driver transmits logic 0, another static current path flows from a top die to a bottom die. Since the parasitic resistance of a TSV is much smaller than that of an off-chip interconnect, die-to-die static current flowing through a TSV can incur significant energy overheads.

To lower the die-to-die static current, threshold voltage can be increased or smaller repeater transistors can be used. This leads to a proportional loss in bandwidth though. In other words, we can intentionally make our SBD TSV channel more resistive in order to reduce static energy at the expense of bandwidth. This tradeoff will be demonstrated on a test chip in Subsection IV-C.

C. Dynamic energy versus static energy

Since F2B TSVs generally incur relatively high capacitance and low parasitic resistance, both dynamic and

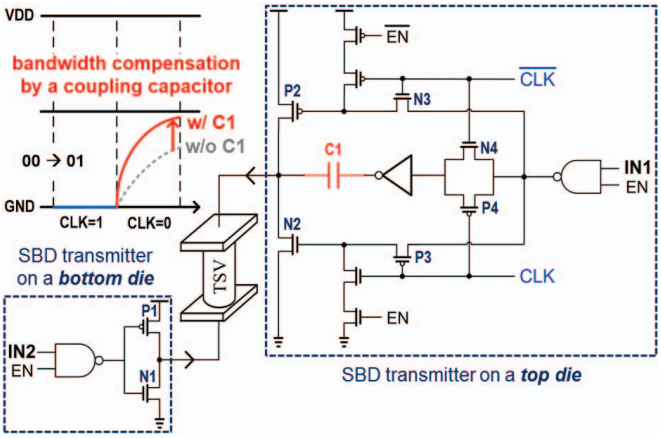

Fig. 4. Proposed SBD transmitter circuit. While a half-clocked driver on a top die enables the die-to-die static current reduction at the cost of bandwidth, a coupling capacitor (C1) compensates such bandwidth loss without adding to static current.

static energy (consumed by die-to-die static current) are important in SBD TSV signaling. However, the relative importance varies depending on TSV technology and data transition rates. For instance, highly capacitive TSVs or higher data transition rates make dynamic energy more important in SBD signaling, while less resistive TSV channels or lower data transition rates make static energy more important. Our test chip results will demonstrate such static/dynamic energy variations (Subsection IV-B).

Design choice wise, when dynamic energy far outweighs static energy in SBD signaling at a given TSV channel and input data, we can sacrifice static energy to increase TSV bandwidth. This is because such a static energy increase is relatively small when considering total energy consumption. However, if static energy takes a considerable portion of the total signaling energy, SBD TSV signaling has to pay substantial energy cost for bandwidth enhancement.

III. Design: Proposed SBD TSV Circuit

In this section, we present a SBD TSV signaling circuit that aims to achieve our system-level design goals as well as energy and area savings at given F2B TSV technology. The design goals are as follows:

- **Reliability:** We consider TSV signaling reliability as our top design priority. Specifically, the target TSV interconnect should function *error free* at all possible process variation corners in a 28nm low-power (LP) CMOS process. In this case study, we do not assume any system-level error-tolerant schemes to detect and correct TSV signaling errors.
- **Bandwidth:** Our target TSV interconnect should deliver 8Gb/s bi-directional data through a single TSV. We assume bandwidth-hungry, high-performance 3D-IC chip design whose clock speed can be boosted up to 4GHz.
- **Delay:** One possible caveat of SBD interconnects is longer signaling delay than uni-directional interconnects, because SBD interconnects need extra delay to sense and convert the middle voltage into full-swing logic level. In this case study, we aim to design the single-cycle TSV link even at its highest clock speed by minimizing such extra delay. In other words, the target TSV interconnect should have signaling delay of less than single cycle across all operating clock frequencies.
- **No static energy on idle TSVs:** The target SBD TSV interconnect should not consume any static energy when there is no data to be transmitted through a TSV. This allows 3D-IC chips to incorporate our SBD TSV link regardless of TSV utilization rates.

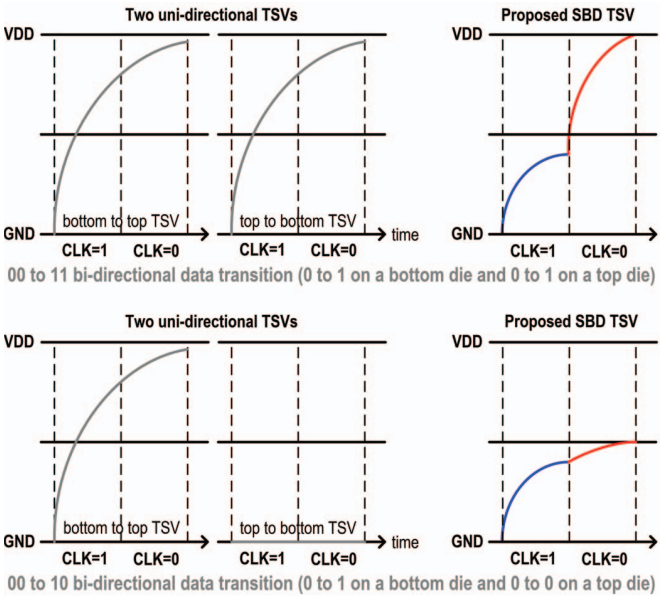

Fig. 5. Conceptual waveforms of conventional uni-directional TSVs and the proposed SBD TSV.

A. SBD Transmitter Design

Figure 4 shows the proposed Tx circuit that enables the die-to-die static current reduction along with bandwidth compensation. Once there is no data to be transmitted through a TSV (EN=0), both sides of a TSV are connected to GND, consuming no static and dynamic energy. When a TSV has bi-directional data to be transmitted (EN=1), a TSV is driven in a different manner during the first half clock period than during the second half clock period.

During the first half clock period (CLK=1), a bottom die driver acts as a repeater composed of two inverters. On the other hand, on a top die, there is no path between an input (IN1) and a TSV. Hence, a TSV is driven by a bottom die pull-up PMOS (P1) or pull-down NMOS (N1) regardless of a top die input, consuming dynamic power only. For energy efficiency, P1 and N1 were sized such that they enabled half voltage swing at a given TSV capacitance and a target data rate.

When a clock signal goes from high to low, N4 and P4 are turned on, generating a signaling path between a top die input (IN1) and a TSV. Accordingly, during the second half clock period, a top die driver also acts as a

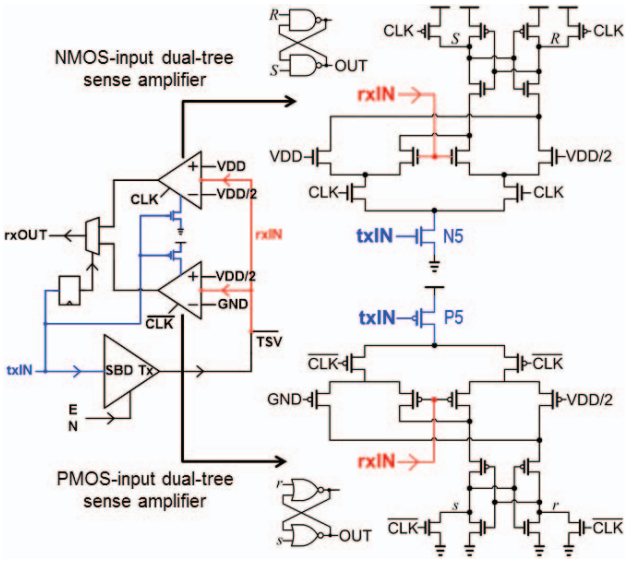

Fig. 6. Switched dual-tree sense amplifier capable of single cycle link traversal and error-free sensing at all process variation corners.

repeater (a NAND gate with EN=1 is the first inverter while the second inverter consists of N2 and P2). Since there are no changes on a bottom die, a TSV is driven by a top die driver and a bottom die driver together. When a TSV delivers bi-directional data of (IN1, IN2) = (0, 1) or (1, 0), a die-to-die static current path is formed to drive TSV voltage to the middle voltage. While the die-to-die current path generated only during the half clock period enables lower static power than the straightforward SBD Tx design using repeaters only, it results in a proportional loss in maximum data rate when a top die input transition causes TSV voltage swing. In order to compensate such bandwidth loss, our top die driver has one more signaling path through a coupling capacitor (C1) that adds dynamic current for faster voltage swing. Since this current through a coupling capacitor only flows during clock transitions (*i.e.* a coupling capacitor functions like a high-pass filter), this design compensates the bandwidth loss without adding to any static current. As will be demonstrated on a test chip in Section IV, the coupling capacitor scheme enables 33.8% bandwidth enhancement with the total energy overhead of less than 6%.

B. SBD Receiver Design

To meet our delay design goal (single cycle link traversal), our SBD Rx should minimize its sensing delay. In terms of small-signal sensing delay, an NMOS-input sense amplifier is optimized for higher input common mode voltage while a PMOS-input sense amplifier is ideally fitted for lower common mode voltage. Thus, a possible Rx circuit implementation is to switch such two sense amplifiers according to the TSV common mode voltage, in a similar way as the reconfigurable sensing network proposed in [12].

In our three voltage-level SBD signaling, the TSV common mode voltage is given by the transmitted data as described in Figure 2 (b). If the transmitted data is 0, the SBD TSV voltage should be GND or VDD/2 (*i.e.* lower common mode voltage). When the transmitted data is 1, the SBD TSV voltage should be VDD or VDD/2 (*i.e.* higher common mode voltage). Thus, based on the transmitted data, we can choose between an NMOS-input sense amplifier and a PMOS-input sense amplifier.

Figure 6 shows such a switched Rx scheme. When the transmitted data (txIN) is 1, an NMOS-input sense amplifier is activated to speed up the sensing operation with higher common mode voltage while a PMOS-input sense amplifier is turned off for energy saving. Similarly, once the transmitted data is 0 (*i.e.* our SBD Rx senses the voltage difference between VDD/2 and GND), a PMOS-input amplifier is switched on for low sensing delay of lower common mode voltage whereas an NMOS-input sense amplifier is turned off. Measurement results show that this switched Rx scheme can support single-cycle SBD TSV signaling at its highest clock speed of 4.55GHz.

Reliability wise, the widely-used sense amplifier designs [12] may incur signaling errors when applying to our SBD Rx circuit; using a reference voltage between VDD and VDD/2 (or GND and VDD/2) as another input of sense amplifiers reduces the sensing noise margin into *half* of the SBD symbol noise margin (*i.e.* VDD/4). Across all possible process variations, the sensing noise margin of VDD/4 will be further reduced. For instance, as shown in Figure 2 (b), a weak PMOS and a strong NMOS decrease the middle level voltage ($V_{m,ideal}$ to $V_{m,variaion}$), making actual noise margin less than VDD/2.

To increase the sensing noise margin of SBD Rx circuits, we present dual-tree sense amplifiers. Figure 6 shows two types of dual-tree sense amplifiers. In this design, the tail current difference of cross-coupled inverters is the result of directly comparing the TSV voltage (rxIN) with VDD/2 and VDD (or GND). Accordingly, its sensing noise margin is equal to the SBD symbol noise margin (*i.e.* VDD/2), whereas the traditional sense amplifier designs [12] have *half* of the SBD symbol noise margin (*i.e.* VDD/4) as their sensing noise margin. Simulated with a 28nm CMOS process design kit (PDK), our dual-tree sense amplifiers achieved error-free sensing functionality across all possible process corners, whereas traditional sense amplifier designs [12] (whose transistors were equivalently-sized with the dual-tree sense amplifiers) incurred errors at some process corners. This is mainly because the input offset of sense amplifiers, which is caused by on-die variations, is bigger than the reduced sensing noise margin.

IV. Test: Chip Prototyping and Results

Our CMOS-on-CMOS 3D-IC test chip was implemented using a 28nm low-power (LP) CMOS process and face-to-back (F2B) TSV technology. As shown in Figure 7, F2B TSVs are connected with top metal micro bumps on a bottom die and poly layer landing pads on a top die.

To fairly compare area, bandwidth and energy of the proposed SBD TSV link versus uni-directional TSVs, both

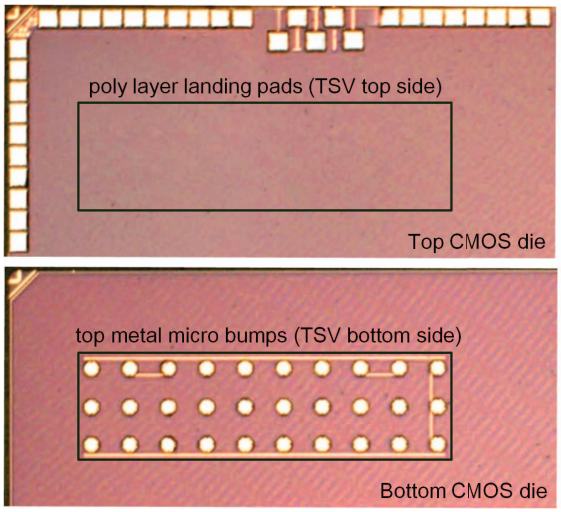

Fig. 7. Die Photo of our 2-tier 3D-IC test chip.

signaling circuits were implemented in the test chip. In addition, to demonstrate the impact of a half-clocked SBD Tx and a coupling capacitor, two baseline SBD TSV links were also included in our chip prototype; the first baseline SBD link employs straightforward Tx implementation using repeaters, while the second SBD link incorporates the same Tx circuit as the proposed design except for the coupling capacitor. Figure 8 shows such four fabricated TSV links along with normalized area and measured bandwidth at 1.05V.

A. Area benefit

The SBD TSV can transmit and receive data at the same time through a single TSV, and accordingly it occupies smaller area than uni-directional TSVs. While such an area benefit is ideally 50% (2 TSVs versus 1 TSV), our proposed SBD TSV link incorporates a half-clocked driver (which is bigger than a uni-directional repeater Tx) and a switched dual-tree sense amplifier (which is also bigger than a conventional flip-flop Rx) so that the actual area benefit is 34.4%. Considering current F2B TSV technology that imposes substantial area overheads due to its poly layer landing pads, this 34.4% area benefit is quite profitable in designing 3D-ICs. For instance, we can take advantage of the saved TSV area for extra signaling TSVs to improve reliability against TSV faults or more power TSVs to enhance power delivery performance.

B. Energy Savings

Figure 9 shows the TSV energy efficiency measured at 1.05V (the nominal power supply voltage of our 28nm LP CMOS process) and 4.55GHz clock speed (the maximum clock speed of the proposed SBD TSV). In order to observe the impact of the data transition rates, four different input sequences were tested.

Experiment results show that the input sequence with a higher data transition rate achieves the best energy saving over two uni-directional full-swing TSVs (31.1% lower energy) whereas the lower data transition input sequence leads to the lowest energy saving (10.3% lower energy). This is because, as analyzed in Subsection II-C, more data transitions make TSV dynamic energy saving (achieved by reduced voltage swing and TSV counts) more dominant over the static energy overhead in SBD signaling.

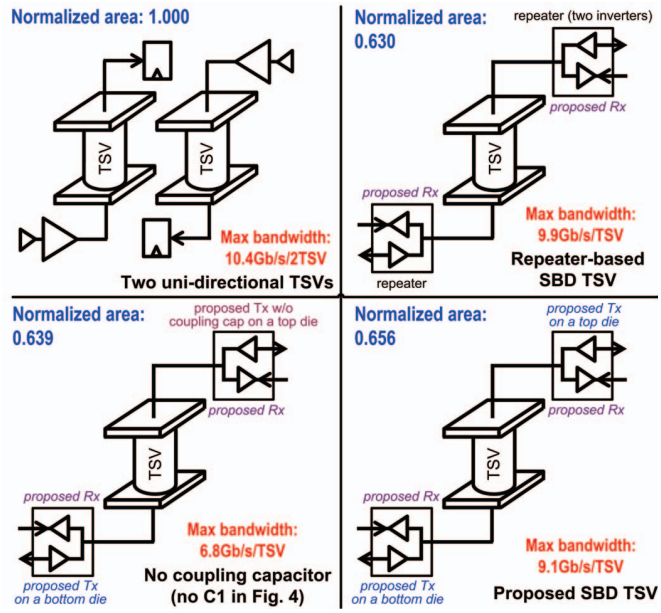

Fig. 8. Normalized area and measured bi-directional bandwidth of four fabricated TSV links: Three baseline designs (uni-directional TSVs and two baseline SBD TSVs) and the proposed SBD TSV.

C. Bandwidth Penalty

Test chip results show that two uni-directional TSVs achieve the maximum data rate of 10.4Gb/s whereas the proposed SBD signaling circuit attains 9.1Gb/s maximum data rate through a single TSV at its highest clock speed of 4.55GHz (12.5% lower bandwidth than two uni-directional TSVs). In other words, the proposed SBD TSVs can deliver $(100-12.5)\times 2-100 = 75\%$ more bi-directional data than uni-directional TSVs with the same TSV counts.

While the repeater-based SBD Tx design achieves the maximum data rate of 9.9Gb/s, the same SBD signaling circuit as our proposed design except for the coupling capacitor has much smaller bandwidth, 6.8Gb/s/TSV. This bandwidth loss explicitly shows the static energy and bandwidth tradeoff analyzed in Subsection II-B. To compensate such a bandwidth loss without adding to static energy, we proposed the coupling capacitor Tx scheme. Experiment results demonstrate that this circuit design enables a 33.8% increase (6.8Gb/s to 9.1Gb/s) in bi-directional bandwidth. Even though the compensated bandwidth is still less than 9.9Gb/s, the 9.1Gb/s SBD TSV satisfies our bandwidth design goal (8Gb/s bi-directional bandwidth) with a 13.7% margin.

V. Related Work

There are only a few TSV interconnect studies at circuit level with actual chip prototypes [3], [8]. Futoshi Furuta

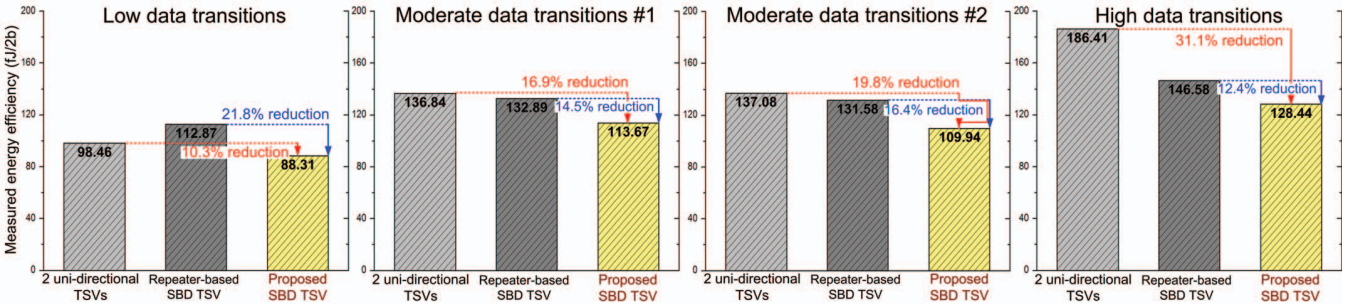

Fig. 9. Measured TSV interconnect energy efficiency with various input data sequences.

	Futoshi Furuta *et al.* [3]	Yong Liu *et al.* [8]	This work
TSV Interconnect Feature	Low-Swing Signaling	Low-Swing Signaling	SBD Signaling
Energy Reduction over Full-Swing TSVs	27%	27 to 53%	10.3 to 31.1%
Voltage Swing (Noise Margin)	0.4V	0.19 to 0.3V	0.505V (half swing)
Process Corner Simulations	Error Free	N/A	Error Free
2nd Power Supply Required	Yes	Yes	No
Area Reduction	No (a little overhead)	No (a little overhead)	Yes (34.4% reduction)
Signaling Type	Single-ended	Single-ended	Single-ended
TSV Lumped Capacitance	$\sim$ 200fF/TSV	$\sim$ 200fF/TSV	N/A
TSV Landing Pad Size	50um×50um	N/A	N/A
Max Clock Frequency	2GHz	6GHz	4.55GHz
3D-IC Stacks	2-tier 3D-ICs	6-tier 3D-ICs	2-tier 3D-ICs
CMOS Technology	65nm CMOS	45nm CMOS	28nm LP CMOS
F2B TSV Technology	N/A	IBM	MediaTek

Table I. Comparison of energy-efficient face-to-back (F2B) TSV interconnects.

et al. demonstrated low-swing TSV circuits featured with adaptive timing control to deal with variations of TSV parasitic lumped capacitance [3]. In their design, low-swing signaling was generated by an inverter with lower power supply voltage, 0.4V, consuming 27% lower energy than an equivalent full-swing TSV. While the 0.4V voltage swing provided enough noise margin, the inverter-based low-swing signaling caused weaker driving strength, resulting in significant bandwidth loss; their uni-directional TSVs were able to deliver 2Gb/s/TSV at most. Yong Liu *et al.* presented a 6-tier 3D-IC chip prototype of low-swing TSV circuits that achieved 27−53% energy savings over full-swing TSVs with 0.19 to 0.3V voltage swing. While the gated-diode sense amplifier enables single-ended low-swing signaling, their small noise margin (0.19 to 0.3V voltage swing) is vulnerable to PVT variations.

While these low-swing TSV interconnects achieve energy saving only, our SBD TSV link achieves area reduction as well as energy saving. Table I compares our SBD TSV with the low-swing TSV signaling circuits [3], [8].

VI. Conclusion

This paper explored SBD TSV signaling to simultaneously tackle the energy and area overheads of F2B TSVs. We first analyzed TSV channel characteristics and design tradeoffs to help design a SBD TSV signaling circuit optimized for given TSV technology (given parasitic capacitance and resistance of TSVs) and target design goals (bandwidth, delay and noise margin). Then, we presented a case study of SBD TSV link design along with test chip results. We believe our analysis, proposed design and silicon-proven results will be useful to the 3D-IC and interconnect research community.

Acknowledgment

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