University Booth

The University Booth is organised during DATE and will be located in booth 15 of the exhibition area. All demonstrations will take place from Tuesday, March 15 to Thursday, March 17, 2016 during DATE. Universities and public research institutes have been invited to submit hardware or software demonstrators.

The University Booth programme is composed of 49 demonstrations from 18 different countries, presenting software and hardware solutions. The programme is organised in 11 sessions of 2 or 2.5 h duration and will cover the topics:

- 5G wireless network Prototypes
- 3D-IC integration Prototypes
- FD-SOI Prototypes
- IoT Prototypes
- Electronic Design Automation Prototypes
- Hardware Design and Test Prototypes
- Automotive System Prototypes
- Secure System Prototypes

The University Booth at DATE 2016 invites you to booth 15 to find out more about the latest trends in software and hardware from the international research community.

Several demonstrators will be shown more than once, giving visitors more flexibility to come to the booth and find out about the latest innovations.

We are sure that the demonstrators will give an attractive supplement to the DATE conference program and exhibition. We would like to thank all contributors to this programme.

More information can be found online at http://www.date-conference.com/exhibition/u-booth. A University Booth programme flyer will be included in the conference bags. The following demonstrators will be presented at the University Booth.

6CH-SDR-PLATFORM: 6 CHANNEL SDR PROTOTYPING PLATFORM FOR VEHICLE SELF-LOCALIZATION
Presenter:
Marko Rößler, Technische Universität Chemnitz, DE
Authors:
Marko Rößler[1], Ulrich Heinkel[1], Daniel Fross[1] and Ahmad El-Assaad[2]
[1]Technische Universität Chemnitz, DE; [2]Novero GmbH, DE
Abstract: *Many modern applications depend on location information. Precision and availability out- and indoor get more and more crucial. Acquisition of this information from radio links used for wireless data transfer is logical step. Link-availability, RSSI, timing or phase shifts are byproducts that carry knowledge about the distance between communication endpoints. Extensive signal processing, advanced receiver setups and statistical algorithms allow the extraction of reliable position information. We present a high performance multichannel SDR platform based on FPGA that allows the quick development of respective technology parts. It is based on KC705-Board connecting a Linux PC via PCIe. Featuring three RF-Frontends (AD-FMCOMM-S3) we are able to control six independent paths time synchronous. With 50 MSa/s at 12 bit resolution a data stream of 7.2 Gbit/s can be processed. We target for radio frequency based vehicle self-localization using smart array antennas.*

A CIRCUIT EXTRACTION TOOL FOR FULL CUSTOM DESIGNED MEMS SENSORS
Presenter:
Axel Hald, Robert Bosch GmbH, DE
Authors:
Axel Hald[1], Johannes Seelhorst[1], Mathias Reimann[1], Juergen Scheible[2] and Jens Lienig[3]
[1]Robert Bosch GmbH, DE; [2]Reutlingen University, DE; [3]Technische Universität Dresden, DE
Abstract: *In contrast to IC design, MEMS design still lacks sophisticated component libraries. Therefore, the physical design of today's MEMS sensors is mostly done by simply drawing polygons. Hence, the sensor structure is only given as plain graphic data which hinders the identification and investigation of topology elements. The growing complexity of future MEMS designs demands a deep and detailed analysis of the sensor structures and the topology elements in order to get a better understanding of the coupling capacitances and parasitics. Our tool is able to extract a circuit out of a*

MEMS sensor designed in a polygon based design flow. The key feature of this tool is a rule based structure recognition algorithm which identifies the topology elements of the sensor. Thereafter, the electrostatic RC-extraction is performed by a commercial field solver. The extracted lumped elements can be used for further simulation and optimization tasks during the design phase.

A-LOOP: AMP SYSTEM WITH A DUAL-CORE ARM CORTEX A9 PROCESSOR WITH LINUX OPERATING SYSTEM AND A QUAD-CORE LEON3 PROCESSOR WITH LINUX OPERATING SYSTEM, OPENMP LIBRARY AND HARDWARE PROFILING SYSTEM

Presenter:
Giacomo Valente, Università Degli Studi Dell'Aquila, IT
Authors:
Giacomo Valente and Vittoriano Muttillo, Università Degli Studi Dell'Aquila, IT

Abstract: *Isles of computational elements with different characteristics can be exploited for separate tasks with different non-functional requirements. This can drive to realization of smart System On Modules (SoM). In such a context, SoC with FPGA can be viewed as platforms useful to prototype these architectures. This demo shows a SoM prototype for aerospace applications developed on Zynq7000 SoC, composed of dual-core ARM Cortex A9 with Linux operating system (isle#1) able to interface with external data, and quad-core Leon3 with SMP Linux operating system (isle#2), able to execute parallel applications based on OpenMP library. These 2 computational isles share an external DDR memory, so that isle#1 can provide data and collect results from isle#2. Moreover, isle#1 is able to monitor performance of isle#2 without introducing software overhead (i.e. no SW instrumentation) by using a hardware profiling system. The whole system that executes a MANET localization algorithm will be presented.*

AGAMID: A TLM FRAMEWORK FOR EVALUATION OF HARDWARE-ENHANCED MANY-CORE RUN-TIME MANAGEMENT

Presenter:
Daniel Gregorek, University of Bremen, DE
Authors:
Daniel Gregorek and Alberto Garcia-Ortiz, University of Bremen, DE

Abstract: *The advent of many-core processors raises novel demands to system design. Power-limitations and abundant parallelism require for efficient and scalable run-time management. But the design of a many-core run-time manager generally suffers from exhaustive evaluation time. AGAMID is a novel research framework for design space exploration of hardware-enhanced many-core run-time management. In this demo, we use AGAMID for the interactive analysis of many-core architectures and run-time management systems. We perform hands-on comparison of RTM architectures, RTM algorithms and HW/SW partitionings. We also give insights into the design and architecture of the framework itself.*

AHLS_DESYNC: DESYNCHRONIZATION TOOL FOR HIGH-LEVEL SYNTHESIS OF ASYNCHRONOUS CIRCUITS

Presenter:
Jean Simatic, TIMA Laboratory, FR
Authors:
Jean Simatic, Rodrigo Possamai Bastos and Laurent Fesquet, TIMA Laboratory, FR

Abstract: *We present a tool for the high-level synthesis (HLS) of event-driven (asynchronous) circuits. Our approach first uses an existing HLS tool, AUGH, to generate a synchronous finite state machine (FSM) and a data-path. Then, the presented tool desynchronizes solely the FSM in 5 steps: 1. Parse the FSM to build a state graph containing the control signal assignments. 2. Separate multiplexer control and register control signals by analyzing the data-path. 3. Generate an event-driven FSM netlist by mapping the state graph on a dedicated set of asynchronous controllers. 4. Synthesize the data-path thanks to a commercial synthesis tool (Design Compiler). 5. Estimate the delays in the data-path with a static timing analysis tool (PrimeTime). Insert delays in the controller accordingly. Our demonstration will exhibit two testbenches: a GCD algorithm to expose the basic concepts and a non-uniform sampling FIR filter more representative of real-life applications.*

AIPHS: ADAPTIVE PROFILING HARDWARE SUB-SYSTEM

Presenter:
Luigi Pomante, Università degli Studi dell'Aquila, IT
Authors:
Luigi Pomante[1], Giacomo Valente[2] and Vittoriano Muttillo[2]
[1]Università degli Studi dell'Aquila, IT; [2]Università Degli Studi Dell'Aquila, IT

Abstract: *Run-time monitoring systems on reconfigurable logic have the advantage that they can be customized with respect to specific applications: in the context of automated testing, this can lead to powerful scenarios. This demo presents a smart monitoring system by showing both a customization for stalls identification in a message passing scenario*

(based on four MicroBlaze that executes a bare-metal FFT application), and a customization for bus utilization monitoring in a symmetric multi-processing system scenario (based on four Leon3 running a custom Linux kernel). The whole development flow (and related prototypal EDA tools), that starts exploiting a library of elements to compose the desired hardware profiler, that leads to the introduction of such a profiler in the target architecture, and that allows profiling data collection and analysis will be shown. Moreover, a comparison among different functionalities will be illustrated. Both systems will be illustrated by using Zynq7000 SoC.

ALPT: A FAST PROTOTYPING METHODOLOGY WITH CONSTRAINED FLOORPLANING ON ANALOG LAYOUT GENERATION

Presenter:
Po-Cheng Pan, National Chiao Tung University, TW

Authors:
Po-Cheng Pan, Hung-Wen Huang and Hung-Ming Chen, National Chiao Tung University, TW

Abstract: *Layout generation in the recent analog design is challenging by its critical layout dependent effect (LDE). Based on the same netlist design, different layouts lead distinct performances. Therefore, it is necessary to observe and avoid the LDE during generation. Traditionally, the strategies of analog layout generation mostly count on experienced designers. However, the experience is based on time-consuming manually try-run, which is inefficient and unreliable. In this work, we develop a fast prototyping for analog layout generation. In our approach, we apply a fast floorplanning algorithm, for multi-layout generation and select the feasible results w.r.t. the analog constraints pre-decided. For practical usage, we implement this approach embedded on the EDA-tool so that layout designers are able to design with such prototypes for efficiency. The demonstration includes layout prototyping generation, the integration between our program and EDA-tool and the resulting layout prototypes.*

ANALYSIS AND VERIFICATION OF COMMUNICATION FABRICS

Presenter:
Frank Burns, Newcastle University, UK

Authors:
Frank Burns, Danil Sokolov and Alex Yakovlev, Newcastle University, UK

Abstract: *xMASCraft is a tool for visual modelling, analysis and verification of GALS xMAS circuits. The tool is based on a structured approach which provides unique visual feedback about complex deadlocks occurring at both global and local levels. The deadlocks are identified by a novel unfolding algorithm that relies on structured occurrence nets driven by synchronisation policy. For deadlock analysis a new representation is used based on blocking/idle relations through which relational analysis can be made based on querying. This is fed back to the interface in the form of unique textual/graphical feedback providing detailed relational information. This enables enhanced visualisation of the causality of the deadlocks to be worked out. In particular it reveals vulnerable parts of the system which are susceptible to shut down, point-to-point causes of deadlock occurring between different modules and the original sources of deadlocks.*

AUTOMATED REFINEMENT OF ANALOG/MIXED-SIGNAL SYSTEMC MODELS BY NON-FUNCTIONAL EFFECTS

Presenter:
Georg Gläser, IMMS, DE

Authors:
Georg Gläser[1], Hyun-Sek Lukas Lee[2], Eckhard Hennig[3], Markus Olbrich[2] and Erich Barke[2]
[1]IMMS, DE; [2]Leibniz Universität Hannover, DE; [3]Reutlingen University, DE

Abstract: *Virtual prototyping of analog/mixed-signal (A/MS) systems is a key concern in the modern design process. The main challenge is performing the verification of functional properties with respect to non-functional effects, e.g. signal and power integrity. System architects are challenged by identifying critical scenarios where these effects possibly degrade or even destroy the system's functionality. We demonstrate a method to automatically extend an existing functional model by non-functional effects. Combined with an accelerated, piecewise-linear (PWL) simulation scheme (PRAISE), we explore the resulting system acceptance regions and identify critical scenarios.*

BIOVIZ: AN INTERACTIVE VISUALIZATION ENGINE FOR MICROFLUIDIC BIOCHIPS

Presenter:
Oliver Keszöcze, University of Bremen, DE

Authors:
Oliver Keszöcze[1], Jannis Stoppe[2], Robert Wille[3] and Rolf Drechsler[2]
[1]University of Bremen, DE; [2]DFKI and University of Bremen, DE; [3]Johannes Kepler University, AT, DFKI and University of Bremen, DE

Abstract: *In order to shorten the required time for the analysis of medical substances, digital microfluidic biochips (DMFBs) have been suggested. Issues such as routing and layouting are complex and currently being investigated. Alt-*

hough first automatic solutions assist the designers, the results are usually provided in a complex and non-intuitive fashion. Creating solutions requires testing of different setups, comparing the results and debugging of algorithms. Solutions, while being technically correct, often include negative aspects such as e.g. unnecessary cell usage. These aspects are difficult to spot without being able to visually inspect the design. Still, while designers would benefit from visualization tools, no dedicated tools have been built yet. We present BioViz, an interactive visualization tool for DMFBs that explicitly addresses these problems.

CHIMPANC: CHANGE MANAGEMENT USING CHIMPANC

Presenter:
Jannis Stoppe, DFKI and University of Bremen, DE
Authors:
Jannis Stoppe, Martin Ring and Rolf Drechsler, DFKI and University of Bremen, DE

Abstract: *One approach to remedy the issue of increasing complexity in the hardware design process is to provide designers with more abstract languages that allow systems to be designed top-down, starting with an abstract model of the system and its requirements. Several of these languages such as SysML and SystemC are being used today. We propose the Change Impact Analysis and Control Tool (ChImpAnC) to handle these challenges. ChImpAnC extracts the relevant information from the models on the different levels and constructs mappings between them, thus allowing to check consistency and refinements, and moreover calculating the impact of changes. Thus, ChImpAnC ensures that e.g. a written specification or documentation is not made obsolete by changes in the implementation without being warned about it.*

CLASH: DIGITAL CIRCUITS IN CλASH

Presenter:
Christiaan Baaij, University of Twente, NL
Authors:
Christiaan Baaij and Jan Kuper, University of Twente, NL

Abstract: *CλaSH is a novel compiler system for generating digital circuits as described by a mathematical/functional specification of the architecture. We will demonstrate several applications written in CλaSH: * Tunneling ball device: With a minimal amount of acceleration, a fast spinning metal disk is either sped up or slowed down so that a falling ball can fall through one of the metal disk's two holes. * Music synthesizer and spectrum analyser: An audio CODEC samples music being played from either an MP3 player or a computer. We can apply several digital filters which affect the music. The effects of these filters can be both seen on a monitor, and heard through speakers connected to the FPGA board. * Multi-processor system: The system is used in a compiler construction course, where the compiler is written in the Haskell. Because CλaSH is proper subset of Haskell, students can build and experiment with the compiler and the multi-processor system in the same environment.*

COMPSOC: VIRTUALISING CONTROL APPLICATIONS ON A DISTRIBUTED COMPSOC PLATFORM

Presenter:
Kees Goossens, Eindhoven University of Technology, NL
Author:
Kees Goossens, Eindhoven University of Technology, NL

Abstract: *In our University Booth we will demonstrate that multiple real-time control applications can be developed independently even though they share platform resources. We show that they can run together with other applications on a wireless network of multiple CompSOC platforms, where each platform has multiple processors, NOC, and a complete microkernel, streaming software, and resource management stack. We will also show that (control) applications can be quickly and safely loaded and started without interference to other (real-time control) applications, thus implementing a network of MPSOCs for distributed mixed time-criticality applications.*

CONTINUOUS CHF MONITORING: AN INTEGRATED, LOW-POWER PLATFORM FOR CONTINUOUS CONGESTIVE HEART-FAILURE MONITORING

Presenter:
Shahzad Muzaffar, Masdar Institute, AE
Authors:
Shahzad Muzaffar, Ibrahim (Abe) M. Elfadel and Jerald Yoo, Masdar Institute, AE

Abstract: *The demo presents a novel ultra-low power wearable system for Congestive Heart Failure (CHF) monitoring using the continuous measurement of a patient's weight to detect changes in body mass and fluid composition. Shoe-mounted sensors are used to continuously measure the weight, and an electronic digital assistant is used to analyze the acquired measurements in real time. To achieve ultra-low power operation, the human body is used as a communication medium between the sensors and the digital assistant. The single-channel behavior of the human body is accommodated with a novel, simple yet robust single-wire signaling technique, Pulsed-Index Communication (PIC), that significantly*

reduces the system footprint and its overall power consumption as it eliminates the need for circuitry dedicated to clock and data recovery. The CHF system prototype, which integrates models for footwear, body area network (BAN), and back-end digital electronics, has been rigorously and successfully tested.

CONTREP: A SINGLE-SOURCE FRAMEWORK FOR UML-BASED MODELLING AND DESIGN OF MIXED-CRITICALITY SYSTEMS

Presenter:
Fernando Herrera, University of Cantabria, ES
Authors:
Fernando Herrera and Eugenio Villar, University of Cantabria, ES

Abstract: *Mixed-criticality systems integrate applications, platform resources and requirements with different criticality. A criticality reflects the impact of either a failure of a component or a violation of a requirement, which can range from irrelevant to catastrophic effects. This booth presents the CONTREP framework, which supports UML/MARTE based modeling, analysis and design of mixed-criticality embedded systems. The booth shows a model of a quadcopter control system which integrates safety critical (e.g. flight control), mission-critical (e.g., a video processing payload), and non-critical (e.g., monitoring) functions. The booth shows how mixed-criticality is captured, together with the description of the functional architecture, and of the multi-core embedded platform where the system is implemented; how CONTREP automates different design activities, i.e. model validation, performance assessment and design space exploration, exploiting mixed-criticality information in every case.*

COSSIM: A NOVEL, COMPREHENSIBLE, ULTRA-FAST, SECURITY-AWARE CPS SIMULATOR

Presenter:
Antonios Nikitakis, Technical University of Crete, GR
Authors:
Antonios Nikitakis and Andreas Brokalakis, Technical University of Crete, GR

Abstract: *Nowadays, Cyber Physical Systems (CPS) are growing in capability at an extraordinary rate, promoted by the increased presence and capabilities of electronic control Units as well as of the sensors and actuators and the interconnecting networks. One of the main problems CPS designers face is the lack of simulation tools and models for system design and analysis. This is mainly because the majority of the existing simulation tools for complex CPS handle efficiently only parts of a system (only the processing or network) while none of them support the notion of security. The presented system is a "Novel, Comprehensible, Ultra-Fast, Security-Aware CPS Simulator" (COSSIM). COSSIM is the first known simulation framework that allows for the simulation of a complete CPS utilizing complex SoCs interconnected with sophisticated networks. Finally, the COSSIM system support accurate power estimations while it is the first such tool supporting security as a feature of the design process.*

D-VASIM: TIMING ANALYSIS OF GENETIC LOGIC CIRCUITS USING D-VASIM

Presenter:
Hasan Baig, Technical University of Denmark, DK
Authors:
Hasan Baig and Jan Madsen, Technical University of Denmark, DK

Abstract: *A genetic logic circuit is a gene regulator network implemented by re-engineering the DNA of a cell, in order to control gene expression or metabolic pathways, through a logic combination of external signals, such as chemicals or proteins. As for electronic logic circuits, timing and propagation delay analysis may also play a very significant role in the designing of genetic logic circuits. In this demonstration, we present the capability of D-VASim (Dynamic Virtual Analyzer and Simulator) to perform the timing and propagation delay analysis of a single as well as cascaded genetic logic circuits. D-VASim allows user to change the circuit parameters during runtime simulation to observe their effects on circuit's timing behavior. The results obtained from D-VASim can be used not only to characterize the timing behavior of genetic logic circuits but also to analyze the timing constraints of cascaded genetic logic circuits.*

DAC GENERATOR: A DAC STAGE ANALOG CIRCUIT GENERATOR FOR UDSM AND FD-SOI TECHNOLOGIES

Presenter:
Benjamin Prautsch, Fraunhofer Institute for Integrated Circuits IIS, Design Automation Division EAS, DE
Authors:
Benjamin Prautsch, Sunil Rao, Uwe Eichler, Ajith Puppala and Torsten Reich, Fraunhofer Institute for Integrated Circuits IIS, Design Automation Division EAS, DE

Abstract: *The design of analog integrated circuits requires extensive manual work which is error-prone and inefficient. With advanced ultra-deep sub-micron (UDSM) technologies, the manual design effort increases further dramatically. This work presents the application of a rethought generator approach for the efficient reusable design of a 12 bit current steering DAC. The current mirror stage of the DAC, which is arranged in the complex Q² random walk scheme for high*

intrinsic matching [1], is realized by a circuit generator which automatically creates schematic, symbol, and layout of the required cells within few minutes. Originally focused on a 28 nm bulk technology, the generator code was also executed in a 28 nm FD-SOI technology with minor migration effort due to the generic nature of our tool. In addition, the fast circuit generation enables an efficient layout optimization showcasing the benefit of analog circuit generators for "bottom-up" design [2] in advanced technology nodes.

DIGITALLY DRIVEN TOP-DOWN METHODOLOGY FOR MIXED SIGNAL CIRCUIT DESIGN

Presenter:
Markus Mueller, University of Heidelberg, DE
Authors:
Markus Mueller, Maximilian Thuermer and Ulrich Bruening, University of Heidelberg, DE

Abstract: *In this methodology,synthesizable modules and full custom blocks are first described in an HDL in a top-down approach. For analog cells, real number based models are created.Once the complete mixed signal model is done, each cell in the design is completely described concerning interface and behavior. The models then serve as specification for the full custom cell development.Schematics which don't include any primitives are automatically generated from the HDL description by a scripted flow to ensure consistency.Design space exploration can be done fast and very efficient this way. Cells which can be reused at different places in the design are identified and problems arising from interactions on the system level are found early in the design phase.This methodology accelerates the design process significantly, avoids errors and provides higher flexibility for design changes. A digital centric design example of a High Speed SerDes IP is demonstrated using the described methodology.*

ELECTRO-, STRESS- AND THERMOMIGRATION: THREE FORCES, ONE PROBLEM

Presenter:
Steve Bigalke, Technische Universität Dresden, DE
Authors:
Steve Bigalke and Jens Lienig, Technische Universität Dresden, DE

Abstract: *It is well-known that the downscaling of microelectronic structures ("Moore's Law") reduces the reliability due to an increase in potential material migration. Electro-, stress- and thermomigration have been identified as the main causes of materiel dislocation in integrated circuits (ICs). They are driven by current densities, stress and temperature gradients, respectively, but they also depend on common parameters like material constants. While each of these three driving forces causes migration, they can compensate or amplify each other, resulting in various overall material dislocations. These interactions are poorly understood which complicates the prevention of migration processes in ICs. Our software demonstrator presents a basic approach to identify the predominate migration within various circuit conditions including the interaction of all three forces. Our approach can also be adjusted to three-dimensional circuits (3D ICs) and alternating conditions.*

ELECTRO-THERMAL SIMULATOR FOR CHIP DESIGN

Presenter:
Vladyslav Ladonkin, Reutlingen University, DE
Authors:
Vladyslav Ladonkin and Juergen Scheible, Reutlingen University, DE

Abstract: *The software product developed by "Robert Bosch Center for Power Electronics" allows an IC designer to easily carry out electro-thermal simulations of a chip design. The software package consists of the electro-thermal simulator "XtSI", its integration in Cadence Virtuoso and a comfortable GUI. XtSI is an industry proven simulator, which precisely calculates the electro-thermal behavior of a packaged IC. The integration software provides different functions for processing of simulation results, calculations and data storing. The communication between the GUI and Cadence Virtuoso is based on Cadence Interprocess Communication with SKILL macros. The GUI itself is developed using the Qt framework, which allows for an easy adaption to different operating systems. The software allows for an easy and exact electro-thermal simulation in early design phases and thus helps the customer to significantly save design effort and increase design quality due to electro-thermal behavior.*

ETEAK: ASYNCHRONOUS DATAFLOWS SYNTHESIS ONTO FPGAS USING THE ETEAK FRAMEWORK

Presenter:
Mahdi Jelodari Mamaghani, The University of Manchester, UK
Authors:
Mahdi Jelodari Mamaghani, Jim Garside and Steve Furber, The University of Manchester, UK

Abstract: *We exploit eTeak (De-Elastisation [DATE'15] enabled) to synthesise asynchronous dataflow descriptions in Balsa into synchronous structure loadable onto FPGA. We will be also able to demonstrate the software realisation of the same architecture running on a laptop and let the audience compare the hardware vs. software concurrency. A brief ex-*

periment conducted in our recent study where a prime number generator (aka sieve of Eratosthenes) is implemented both in software using the CSP compiler and hardware using eTeak: On average the hardware implementation runs 90-120x faster than its software counterpart while the processor clock speed is almost the same as the hardware clock speed (1.2GHz). This allows us to plan ahead and exploit eTeak toward energy-efficient synthesis. According to EPSRC's research portpolio this work falls under the most growing research subject of "Energy Efficiency" which aims to achieve an energy reduction of 26-43% by exploiting ICT.

EXTRA-FUNCTIONAL PROPERTY SIMULATION WITH VIRTUAL PLATFORMS

Presenter:
Ralph Görgen, OFFIS - Intitute for Information Technology, DE
Authors:
Ralph Görgen, Kim Grüttner and Sören Schreiner, OFFIS - Intitute for Information Technology, DE

Abstract: *The demo shows the usage of virtual platforms and model-based design to perform early analyses of extra-functional properties in a mixed-critical scenario. The application shown is a quadro-copter equipped with a camera system. The copter's flight controller is safety critical; the video processing is less critical. Both parts of the system are implemented in a single chip, a Xilinx ZNQ SoC. The video processing is implemented in the ARM dual-core, the flight controller is realized in the FPGA part and based on two MicroBlaze cores. This platform has been modeled as an OVP-based virtual platform, which is extended by more fine grain timing models as well as power models. Furthermore, it can be coupled with a model of the quadro-copter physics and environment realized in iXtronics CamelView. We will show how to use this setup to analyze timing, power, and temperature behavior of the system and the interference between the high- and low-critical parts with respect to these properties.*

FORMAL VERIFICATION OF CLOCK DOMAIN CROSSING USING GATE-LEVEL MODELS OF METASTABLE FLIP-FLOPS

Presenter:
Ghaith Tarawneh, Newcastle University, UK
Authors:
Ghaith Tarawneh, Andrey Mokhov and Alex Yakovlev, Newcastle University, UK

Abstract: *We present a first prototype of a gate-level tool that enables simple and intuitive verification of multi-clock designs. The tool's underlying methodology (described in the paper "Formal Verification of Clock Domain Crossing using Gate-level Models of Metastable Flip-Flops" to be presented in the conference) relies on transforming gate-level netlists so that they can reproduce problematic CDC behaviour digitally. Processed netlists can then be passed to formal verification tools to identify and debug CDC faults. The tool is at an early development stage but consists of a functional Verilog parser and CDC transformation functions that can be invoked from the command line. The demo will showcase the tool using simple sender-receiver circuits. Synthesized netlists will be processed by the tool and then fed to a formal verification tool to identify CDC issues (e.g. missing synchronizers, path convergence). Verification output from source and processed netlists will be compared.*

GPCDS: AN INTERACTIVE TOOL FOR CREATING SCHEMATIC MODULE GENERATORS IN ANALOG IC DESIGN

Presenter:
Matthias Greif, Reutlingen University, DE
Authors:
Matthias Greif and Juergen Scheible, Reutlingen University, DE

Abstract: *While digital design automation is highly developed, analog design automation still remains behind the demands. Previous approaches of circuit creation, which are usually based on optimization algorithms, do not satisfy industrial requirements. A promising alternative is given by procedural approaches, which imitate the solution strategy of a human expert. We are working on parameterized generators (such as PCells) for analog circuit and layout modules, special kinds of such procedures. We present "gPCDS", a novel tool for the creation of schematic generators for analog circuit design. Associated with a common design environment, gPCDS offers a sophisticated interactive design flow for the development of schematic PCells. gPCDS thus substitutes the crucial process of manual code writing by an intuitive graphic-based way of schematic PCell creation. The GUI of gPCDS provides a variety of useful functions, such as defining parameter ranges or placing predefined building blocks.*

GRIP: GRAPH-REWRITING-BASED IP-INTEGRATION (GRIP) - AN EDA TOOL FOR SOFTWARE DEFINED SOC DESIGN

Presenter:
Munish Jassi, Technische Universität München, DE
Authors:
Munish Jassi, Yong Hu, Jian Lyu, Daniel Mueller-Gritschneder and Ulf Schlichtmann, Technische Universität München, DE

Abstract: *The GRIP tool – Graph-Rewriting-Based IP-Integration - provides system engineers with a comprehensive platform that takes care of their IP-integration concerns for IP-centric SoC designs, also referred to as SW-defined SoCs. The tool uses the standardized meta-data IP-XACT format for HW descriptions and encodes the design IP-integration knowledge as a set of integration rules based on graph rewriting and grammar theory. The tool automates and encodes the step-by-step integration of IPs to build a desired system architecture. Multiple sequential IP-integration steps can be compiled to iteratively generate new architectures. For design space exploration (DSE), constraints can be given to generate a desired subset of candidate SoCs. Code generation generates the design files for each architecture. This is demonstrated as DSE for OpenCV CV application running on a Xilinx Zynq chipset based Zedboard. GRIP additionally generates the HW-drivers for both non-OS and Linux-based systems.*

HIGH-END 122GHZ MINIATURE RADAR SENSOR FOR AUTONOMOUS AIRCRAFTS

Presenter:
Federico Nava, Heinz Nixdorf Institute - Universität Paderborn, DE
Authors:
Federico Nava[1] and Christoph Scheytt[2]
[1]Heinz Nixdorf Institute - Universität Paderborn, DE; [2]Heinz Nixdorf Institute - Paderborn, DE

Abstract: *The importance of high precision sensors, sensors-arrays and the concept of sensor fusion are rising interest in the field of scientific research for autonomous vehicles. For this reason the System and Circuit Technology group at the Heinz Nixdorf Institute is currently developing a highly integrated radar module as a sensor for Unmanned Aerial Vehicle applications. The presented system is composed of a radar IC (130nm SiGe) with in-package antennas and operating frequency of 122GHz mounted on a FLEX-PCB including a CORTEX M4 MCU for a total size of 30x30mm. The presentation will show the FMCW/CW radar functions of the device, allowing the tracking of velocity and distance for multiple objects. The results of the radar measurements will be presented on a screen showing the raw data acquired in time domain and a FFT representation. Different objects will move simultaneously in the area of reception of the sensor. The results of the tracked distances will be then plotted on screen.*

HYPERDIMENSIONAL COMPUTING FOR TEXT CLASSIFICATION: AN EFFICIENT SOFTWARE IMPLEMENTATION

Presenter:
Fateme Rasti Najafabadi, Sharif University of Technology, IR
Authors:
Fateme Rasti Najafabadi[1], Abbas Rahimi[2], Pentti Kanerva[2] and Jan Rabaey[2]
[1]Sharif University of Technology, IR; [2]University of California, Berkeley, US

Abstract: *The mathematical properties of high-dimensional spaces show remarkable agreement with behaviors controlled by the brain. Hyperdimensional computing explores the emulation of cognition by computing with hypervectors as an alternative to computing with numbers. Hypervectors are high-dimensional (e.g., 10,000 dimensions) and holographic, and they appear randomly. These properties provide an opportunity for efficient computing, while aligning well with undesirable hardware variations in nanoscale fabrics. We focused on an application of hyperdimensional computing for text classification. Accordingly, we developed an algorithm to classify news stories from a stream of letters. Using pentagrams, the algorithm achieved a classification accuracy of above 95% for eight news topics that surpasses the other reported techniques in the literature including Bayes, K-NN, and SVM. We demonstrated a fully software framework that enables execution of such algorithms on the contemporary hardware fabrics.*

IDDD: AN INTERACTIVE DEPENDABILITY DRIVEN DESIGN SPACE EXPLORATION

Presenter:
Stefan Scharoba, Brandenburg University of Technology Cottbus-Senftenberg, DE
Authors:
Stefan Scharoba, Jacob Lorenz and Heinrich T. Vierhaus, Brandenburg University of Technology Cottbus-Senftenberg, DE

Abstract: *Due to the downscaling of transistor feature sizes, today's integrated circuits are much more likely to be affected by transient or permanent faults. In order to still meet certain dependability requirements, many different fault tolerance techniques have been developed, which can handle these faults in the field. Each of these techniques is associated with distinct costs and benefits. As a consequence, finding the fault tolerant implementation of the system that meets the actual requirements best represents a challenging task. We propose a tool that supports this process. It offers a set of hardware based fault tolerance techniques that can be applied to a given VHDL model. Afterwards, costs and benefits of the respective design choice are estimated automatically. Thus several fault tolerant versions of the design can be evaluated and compared with each other without implementing them manually. Finally, the VHDL code of the preferred design candidate can be generated by the tool.*

IN-NODE PROCESSING: MODELLING FRAMEWORK FOR IN-NODE PROCESSING IN INDUSTRIAL SENSOR AND ACTUATOR NETWORKS.

Presenter:
Qaiser Anwar, Mid Sweden University, SE
Authors:
Qaiser Anwar, Muhammad Imran and Mattias O´Nils, Mid Sweden University, SE
Abstract: *Architecting efficient systems with on-board sensing capabilities with a growing number of sensing devices is a challenging task, in particular because of the range of the technological field, as well as the diversity and complexity of requirements. We present a novel modeling framework, which can describe different implementation strategies for computation of data locally. In this framework, we first describe the systems in Architecture Analysis and Design Language (AADL), following which the described system is exported to XML which is then given input to java based software program. This program automatically generates different implementation options, illustrates different parameters such as processing energy, communication energy, latency and design complexity. To show a proof-of-concept, we have modelled a real-life system in a modelling framework, which shows that the framework can be of use in automated design space and architecture exploration for in-node processing.*

INVADESIM: A SIMULATOR FOR HETEROGENEOUS MULTI-PROCESSOR SYSTEMS-ON-CHIP
Presenter:
Sascha Roloff, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE
Authors:
Sascha Roloff, Frank Hannig and Jürgen Teich, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE
Abstract: *Innovative simulation mechanisms at system-level are a key for embedded hardware designers and parallel software developers to predict performance. This is important especially in a very early development phase where design space exploration (DSE) helps to guide design decisions in proper directions. In case of modern MPSoCs, DSE can be very costly and time consuming depending on the underlying simulation techniques. We present InvadeSIM, a parallel execution-driven simulator for fast functional and timing simulation of heterogeneous NoC-based MPSoCs. For this purpose, InvadeSIM combines a fast direct-execution simulation approach with different parallelization strategies. We will showcase our work by simulating a stream processing application from computer vision domain on a tiled MPSoC architecture in real-time. In particular, we present an object tracking chain that continuously captures frames from a robot camera, followed by object detection, and a control loop back to the camera.*

LISA: ENABLING LAYERED INTEROPERABILITY FOR INTERNET OF THINGS THROUGH LISA
Presenter:
Behailu Shiferaw Negash, University of Turku, FI
Authors:
Behailu Shiferaw Negash[1], Amir-Mohammad Rahmani[1], Tomi Westerlund[1], Pasi Liljeberg[1] and Hannu Tenhunen[2]
[1]University of Turku, FI; [2]University of Turku, FI and Royal Institute of Technology (KTH), SE
Abstract: *There is high expectation towards the changes that come with the implementation of the Internet of Things (IoT). However, this vision is limited by the heterogeneous nature of IoT devices. This led to vertical application silos that are incapable of working together. To ease this problem of heterogeneity, we have developed a lightweight interoperability framework, LISA, to hide variations in communication technology and data formats and provide a uniform API for programmers. LISA is inspired by Network on Terminal Architecture (NoTA), an open framework from Nokia Research Center. There are few frameworks for interoperability of IoT. However, these frameworks fail to address the resource limitations of the majority of IoT devices. To the best of our knowledge, LISA is the first framework designed for resource constrained devices. This demonstration shows LISA in action, helping heterogeneous devices interoperate through a gateway in the fog layer between the devices and the cloud.*

LLBMC / QPR-VERIFY: HIGH-PRECISION BOUNDED MODEL CHECKING FOR AUTOMOTIVE SOFTWARE
Presenter:
Carsten Sinz, Karlsruhe Institute of Technology (KIT), DE
Authors:
Carsten Sinz, David Farago, Florian Merz and Reimo Schaupp, Karlsruhe Institute of Technology (KIT), DE
Abstract: *LLBMC (the low-level bounded model checker) is a static software analysis tool for finding bugs in C (and, to some extent, in C++) programs. It is mainly intended for checking low-level system code and is based on the technique of Bounded Model Checking. LLBMC is fully automatic and requires minimal preparation efforts and user interaction. It supports all C constructs, including not so common features such as bitfields. LLBMC models memory accesses (heap, stack, global variables) with high precision and is thus able to find hard-to-detect memory access errors like heap or stack buffer overflows. LLBMC can also uncover errors due to uninitalized variables or other sources of non-deterministic behavior. Due to its precise analysis, LLBMC produces almost no false alarms (false positives). LLBMC is developed at Karlsruhe Institute of Technology, and will soon be commercially available via a university spin-off, QPR Technologies.*

LOOPINVADER: A COMPILER FOR TIGHTLY COUPLED PROCESSOR ARRAYS

Presenter:
Alexandru Tanase, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE

Authors:
Alexandru Tanase, Michael Witterauf, Ericles Sousa, Vahid Lari, Frank Hannig and Jürgen Teich, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE

Abstract: *In today's coarse-grained reconfigurable architectures (CGRAs), application performance depends mostly on exploiting loop level and instruction level parallelism. However, it is tedious and error-prone to program such architectures in machine language manually. Here, only a compiler can make such architectures feasible. For solving this problem, we present a compiler for programming massively parallel processor arrays in particularly for so-called tightly processor arrays (TCPAs).By using a domain-specific language as design entry, our compiler symbolically parallelizes the code by using symbolic loop tiling techniques in the polyhedron model. Then, by replacing the parameters, e.g., with the desired number of processors elements (PEs), the compiler generates assembly code and interconnect configuration for different PEs which are combined to one binary. Finally, we demonstrate our tool flow for several selected examples.*

MCC: CONTRACT-BASED AUTOMATED INTEGRATION FOR COMPONENT-BASED CRITICAL SYSTEMS

Presenter:
Johannes Schlatow, TU Braunschweig, DE

Authors:
Johannes Schlatow, Marcus Nolte, Rolf Ernst and Markus Maurer, TU Braunschweig, DE

Abstract: *In the scope of the research unit Controlling Concurrent Change, we developed a contract-based middleware to autonomously manage and ensure the safety, availability and security properties of a component-based run-time environment. It guarantees that any change to the system is formally analysed beforehand and only applied if it does not violate any of the contracts, thereby enabling in-field updateability of complex critical systems. For this purpose, a Multi-Change Controller (MCC) aggregates component contracts and invokes viewpoint-specific analysis engines to evaluate change requests and find feasible system configurations. The MCC is specifically designed for extensibility so that analysis engines can be added and combined dependent on the application domain. We show a demonstrator that showcases and illustrates this contract-based process for an automated integration of an automotive system. Our demonstrator is built upon the Genode OS Framework and Xilinx Zynq-7000 SoCs.*

MICROTESK ARMV8 EDITION: SPECIFICATION-BASED TEST PROGRAM GENERATOR

Presenter:
Andrei Tatarnikov, Russian Academy of Sciences (RAS), RU

Authors:
Andrei Tatarnikov, Alexander Kamkin and Artem Kotsynyak, Russian Academy of Sciences (RAS), RU

Abstract: *This work presents a test program generation tool for ARMv8 microprocessors. The tool consists of two parts: an architecture-independent test program generation core and ARMv8 specifications. The specifications provide information on the instruction set architecture and the memory management unit of an ARMv8 microprocessor. Test programs are generated on the basis of test templates provided by users and testing knowledge extracted from the specifications. Test templates describe scenarios to be covered in terms of test situations, while testing knowledge specifies constraints that should be satisfied in order for these situations to occur. The architecture-independent test program generation core implements a wide range of test generation techniques including random generation, combinatorial generation, constraint solving and symbolic execution. Flexible architecture of the tool allows integrating different generation methods and extending the test generation core with new engines.*

NEURODSP: A MULTI-PURPOSE ENERGY-OPTIMIZED ACCELERATOR FOR NEURAL NETWORKS

Presenter:
Jean-Marc PHILIPPE, CEA LIST, FR

Authors:
Jean-Marc PHILIPPE, Alexandre CARBON and Renaud SCHMIT, CEA LIST, FR

Abstract: *Deep Neural Networks (e.g. Convolutional Neural Networks) is a promising approach to design smart machines for a wide range of application domains (automotive, home automation, industry, etc.). Due to their structure, these processing chains are compute intensive and difficult to embed into low power systems. To tackle this challenge, CEA LIST investigated the NeuroDSP hardware accelerator IP, able to be embedded into FPGA- or ASIC-based systems. Providing the system with a dramatic performance/watt ratio improvement, the IP can sustain 450GMACS/W in FDSOI 28nm technology, meeting the requirements of high-end embedded applications. The proposed demonstration features a comparison between three implementations of a CNN processing chain used to detect faces in a large image database. It shows that a single cluster FPGA-based implementation of the NeuroDSP IP at 100MHz is able to outperform both a Raspberry Pi 2 and an Odroid-XU3 board by a factor of respectively 10 and 6 in performance.*

PFPSIM: A PROGRAMMABLE FORWARDING PLANE SIMULATOR

Presenter:
Gordon Bailey, Concordia University, CA
Author:
Gordon Bailey, Concordia University, CA

Abstract: *We demonstrate PFPSim, a host-compiled simulator for early validation and analysis of packet processing applications on programmable forwarding plane architectures, used in software defined networks. The simulation model is automatically generated from a high-level description of the hardware/software architecture of the forwarding device and the behavioral description of the various modules in the architecture. Our high-level architectural description language is capable of defining many-core network processors as well as reconfigurable pipelines. The behavior of the fixed-function processing elements in the architecture is defined in C++. The code targeted for the processor cores, or reconfigurable pipeline stages, is compiled from P4, an emerging programming language for packet processing applications. Network dataplane programmers can use PFPSim as a virtual prototype to simulate and debug their applications before hardware availability.*

PSMGEN: AUTOMATIC GENERATION OF POWER STATE MACHINES

Presenter:
Alessandro Danese, University of Verona, IT
Authors:
Alessandro Danese[1], Graziano Pravadelli[1] and Daniel Lorenz[2]
[1]University of Verona, IT; [2]OFFIS - Institute for Information Technology, DE

Abstract: *Power State Machines are a well-known approach to model and simulate the time-based energy consumption of IP cores for early virtual prototyping of SoCs. However, in the most of the works either the presence of PSMs is assumed or they are manually defined starting from a more or less precise knowledge of the functional blocks composing the target IP. To allow a tighter definition of PSMs, we present PSMGen, a tool implementing an automatic methodology for PSMs' generation and an efficient statistical approach for their simulation. The tool requires as input a set of functional traces exposing the IP's behaviours and the corresponding set of power traces over time that represent the golden model of the IP's energy consumption.It then generates PSM's states and transitions through a mining procedure that extracts the IP behaviours from the functional traces, analyses power changes on the power traces and annotate each PSM's state with the corresponding power characterization*

Q27: PUTTING QUEENS IN CARRY CHAINS

Presenter:
Thomas Preußer, Technische Universität Dresden, DE
Author:
Thomas Preußer, Technische Universität Dresden, DE

Abstract: *The N-Queens Puzzle is a fascinating combinatorial problem. Up to now, the number of distinct valid placements of N non-attacking queens on a generalized NxN-chessboard cannot be computed by a formula. Solution counts obtained from extensive explorations of the solution space are currently known for all N up to 26. The parallelization of this exploration is embarrassingly simple and is achieved by pre-placing the queens of a certain board region. This very flexible partioning approach makes the N-Queens Puzzle a great show-off case for tremendously parallel computation approaches. This demo illustrates an approach to compute the next, yet unknown solution count for the 27-Queens Puzzle that is based on a coronal pre-placement that does not only partition the overall computation but also cuts the size of the search space significantly by exploiting inherent symmetries. It presents higly effective hardware solvers that back an ongoing tremendously parallel computation.*

RC3E: DESIGN AND TEST AUTOMATIZATION IN THE CLOUD

Presenter:
Patrick Lehmann, Technische Universität Dresden, DE
Authors:
Patrick Lehmann, Oliver Knodel, Martin Zabel and Rainer G. Spallek, Technische Universität Dresden, DE

Abstract: *Cloud computing is getting more and more interesting for companies, caused by its flexibility to provide apparently endless resources and nouveau services, while reducing he total cost of ownership for the user. Fields of applications reach from web technologies over storage solutions to complex business processes. The domain of chip and system design is well known for offloading resource intensive and long running synthesis or simulation task onto centralized servers. As hardware designs grow in an exponential way and verification requirements were strengthened, cloud services are investigated to compensate these needs. Anyway, in the end real hardware tests cannot be avoided. Our RC3E eco system brings close to the hardware prototype development and automated hardware testing into the cloud, continu-*

ing the principle of "test often and test early". The architecture offers virtualized and shared FPGA resources for prototyping, with automated remote debugging capabilities.

RESECU_4_AMBRAMS: TOWARDS INCREASED RELIABILITY AND HARDWARE SECURITY USING AMBRAMS

Presenter:
Petr Pfeifer, TU Liberec, CZ
Author:
Petr Pfeifer, TU Liberec, CZ

Abstract: *AmBRAMs-The new method and developed advanced Analysis Tool and Framework for Advanced Measurements and Reliability Assessments on Modern Nanoscale FPGAs creates revolutionary new set of tools enables complex lab-on-chip solutions in nanoscale FPGAs.AmBRAMs has been enhanced of advanced measurements and data processing supporting platform identification and security support functionality including tampering detection preferably in modern nanoscale programmable devices.It will be presented on VLIW soft processor cores equipped with a security IP,and showing also POF solutions and related functionality.Detection of power voltage variation using AmBRAMs technology is incorporated in the processor application and demonstrating it on a complex processor system.Presented on 28nm LP or 20nm HP UltraScale Xilinx FPGA devices.The 28nm FPGA solution will also show simple HW adjustments enabling support of power supply change required the demonstrator and for adaptive control presented as well.*

RETRASCOPE: TOOLKIT FOR ANALYSIS AND VERIFICATION OF HDL DESIGNS

Presenter:
Sergey Smolov, Russian Academy of Sciences (RAS), RU
Authors:
Sergey Smolov, Alexander Kamkin and Mikhail Lebedev, Russian Academy of Sciences (RAS), RU

Abstract: *Retrascope is an open-source toolkit for Reverse Engineering and TRAnsformation of digital hardware designs described in such hardware description languages as Verilog and VHDL. The toolkit allows analyzing HDL descriptions, reconstructing the underlying models (guarded actions, extended finite state machines, high-level decision diagrams etc.) and using the derived models for test generation, property checking and other tasks. Retrascope is organized as an extendible framework with the ability to add new types of models as well as tools for their analysis and transformation. The primary application domain of the toolkit is functional verification of hardware at the unit level.*

RT-POWMODS: RUN-TIME CPU POWER MODELS FROM REAL DATA

Presenter:
Matthew Walker, University of Southampton, UK
Authors:
Matthew Walker[1], Stephan Diestelhorst[2], Andreas Hansson[2], Geoff Merrett[1] and Bashir Al-Hashimi[1]
[1]University of Southampton, UK; [2]ARM Ltd., UK

Abstract: *Being able to accurately estimate CPU power consumption is a key requirement for both controlling online CPU energy-saving techniques and design-space exploration. Models built and validated using measured data from an actual device are valuable as their accuracy is known and trusted. We present our techniques and freely available software tools for running experiments on mobile development boards and using the recorded data to build accurate run-time power models. Our novel methodology uniquely considers the stability of the model and we demonstrate how it allows the models to achieve a higher accuracy on a wider range of workloads. We show how our tools are able to predict run-time power of an ARM Cortex-A15 CPU with an average error of less than 3% when validated with over 50 workloads.*

SRAM-BASED PHYSICAL UNCLONABLE KEYS FOR BLE SMART LOCK SYSTEMS

Presenters:
Iluminada Baturone and Miguel Ángel Prada-Delgado, University of Seville, ES
Authors:
Iluminada Baturone[1], Miguel Ángel Prada-Delgado[1], Alfredo Vázquez-Reyes[1], Laurentiu Acasandrei[2], Diego Fernández-Barrera[2] and Javier Prada-Delgado[2]
[1]University of Seville, ES; [2]OCLOSE S.L., ES

Abstract: *Nowadays, several smart lock systems use Bluetooth Low Energy (BLE) to recognize when a smartphone, conveniently authenticated by a digital key, is near. The keys can be shared and are managed by web apps, so that system security depends on how the software prevents an attacker from discovering the keys. In order to increase security by a two-factor method ('something you have' in addition to 'something you know'), the BLE smart lock system prototype shown in this demonstrator recognizes when a user wearing an authenticated BLE chip (in a key fob, wristband, etc.) is near. The digital keys are not stored but they are regenerated on the fly by only the trusted chip. This is possible by using the start-up values of the SRAM in the BLE chip, which act as a physical unclonable function (PUF), so that the chip*

cannot be cloned. The SRAM start-up values of the BLE chip are also exploited as true random numbers to derive fresh keys for each transaction with the lock.

T-RIDE: A MOBILE-HEALTH NEURODIAGNOSTIC SYSTEM BASED ON SPATIO-TEMPORAL P300 MONITORING: DESIGN, DEVELOPMENT AND TEST IN VIVO

Presenter:
Valerio Francesco Annese, Politecnico di Bari, IT
Authors:
Valerio Francesco Annese, Giovanni Mezzina and Daniela De Venuto, Politecnico di Bari, IT

Abstract: *A mobile health solution for neuro-cognitive impairment monitoring based on P300 spatio-temporal characterization achieved by tuned Residue Iteration Decomposition (t-RIDE) has been presented. The m-health service proposed allows remote monitoring of neuro-cognitive impairment through a 'plug and play' application, while doctor customization and data collection are allowed by cloud bridging. The developed t-RIDE method overcomes the limitations of the previous approaches (ICA; PCA; grand average; etc.). Its testing has been performed on 8 subjects performing three different cognitive tasks of increasing difficulty. P300 amplitude ranges (3.6uV – 11uV), latencies (280ms-390ms) and frontal-cortex spatial evidence (Pz, Fz, Cz) fully match medical references. T-RIDE convergence is reached in 148 iteration ensuring a 80% accuracy in P300 amplitude using only 13 trials (worst case) on single channel.*

UCAF TOOL: AN OPTIMIZATION-BASED DESIGN METHODOLOGY FOR ULTRA-LOW VOLTAGE ANALOG INTEGRATED CIRCUITS

Presenter:
Lucas Severo, Federal University of Pampa, BR
Authors:
Lucas Severo[1] and Wilhelmus Noije[2]
[1]Federal University of Pampa, BR; [2]University of São Paulo, BR

Abstract: *This work presents an Ultra-Low Voltage (ULV) analog integrated circuit design methodology. This methodology is able to sizing analog circuits using an exploration in design space with Simulated Annealing optimization heuristic and an electrical simulator for the specifications estimation. This exploration includes the analysis of Process, Voltage and Temperature variations in order to reduce the effect of these variations in the circuit specifications. The methodology implementation is optimized to ULV circuits and has several testbenches, making possible to design a large number of circuit topologies. Parallel simulations are used to decrease the execution time. As an application of this methodology a 0.6 V fully differential Operational Transconductance Amplifier (OTA) is designed. In a second time, using a bottom-up approach, an active low pass filter is designed using the previously designed OTA. The filter results is in according with the IEEE 802.15.4 standard requirements.*

VISUALNOC: VISUALIZATION NETWORK-ON-CHIP DESIGN FRAMEWORK

Presenter:
Junshi Wang, Unversity of Electronics Science and Technology of China, CN
Authors:
Junshi Wang[1], Letian Huang[1], Guangjun Li[1] and Axel Jantsch[2]
[1]Unversity of Electronics Science and Technology of China, CN; [2]Technology University of Vienna, AT

Abstract: *Simulations are the most common approach to evaluating Network on Chip (NOC) designs and many simulators at different abstraction levels have been developed. However, developers have to spend a considerable amount of time and energy to extract meaningful information from the simulator reports. Visualization of simulation is a sensible approach in the study of NoC design. We introduce a Visualization Network-on-Chip Design Framework (VisualNoC) that can connect with any NoC simulator. It tracks the event trace files of the simulator recording the behavior of routers and packets in the network based on an event-based model. VisualNoC operates with cycle-accuracy in analyzing the status of the network and can complement traditional tools to facilitate efficient debugging and analysis helping to reduce the number of design iterations.*

WORKCRAFT: FRAMEWORK FOR INTERPRETED GRAPHS

Presenter:
Danil Sokolov, Newcastle University, UK
Author:
Danil Sokolov, Newcastle University, UK

Abstract: *A large number of models that are employed in the field of concurrent systems' design, such as Petri nets, gate-level circuits, dataflow structures, etc. - all have an underlying static graph structure. Their semantics, however, is defined using additional entities, e.g. tokens or node/arc states, which in turn form the overall state of the system. We jointly refer to such formalisms as interpreted graph models (IGMs). Workcraft is designed to provide a flexible common*

framework for development of IGMs, including visual editing, (co)simulation and analysis. The similarities between the IGMs allow for links between different formalisms to be created, either by means of adapter interfaces or by conversion from one model type into another. This greatly extends the range of applicable modelling and analysis techniques.

See you at the University Booth!

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