

EVENT OVERVIEW

MONDAY

- Educational Tutorials
- Fringe Meetings & Co-Located Workshops
- Welcome Reception & PhD Forum, hosted by EDAA, ACM SIGDA, and IEEE CEDA

TUESDAY

- Opening Plenary, DATE Awards Ceremony and Keynote Addresses
- Technical Conference
- Vendor Exhibition & Exhibition Theatre
- Executive Sessions
- University Booth
- Fringe Meetings & Co-Located Workshops
- Exhibition Reception

WEDNESDAY

- Technical Conference
- Vendor Exhibition & Exhibition Theatre
- Special Day on “Automotive Systems” and Keynote
- University Booth
- Fringe Meetings & Co-Located Workshops
- DATE Party – Networking Event

THURSDAY

- Technical Conference
- Vendor Exhibition & Exhibition Theatre
- Special Day on “Secure Systems” and Keynote
- Fringe Meetings & Co-Located Workshops
- University Booth

FRIDAY

- Special Interest Workshops

CONTACTS

DATE 2016 Event Secretariat

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Registration & Accommodation

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0800 – Registration and Tutorial Welcome Refreshments at
0930 Conference Level, foyer

Breaks 1100-1130 Morning Coffee Break
1600-1630 Afternoon Coffee Break

	Konferenz 1	Konferenz 2	Konferenz 3	Konferenz 4	Konferenz 5
0930 – 1300	M01 Design solutions: Evolutionary computing in circuit synthesis, optimization and approximation	M02 Power efficiency: Getting the Current In and the Heat Out – Power Delivery and Thermal Challenges for Mobile Computing Systems	M03 Internet-of-Things: Design Methodologies and Tools for the Internet-of-Things	M04 Secure systems: Design Automation, Test, and Error Recovery: Towards Secure, Dependable, and Adaptive Microfluidic Biochips	M05 Test and diagnosis: Hierarchical Test for Today's SOC and IoT

1300 – 1430 Lunch Break

1330 Conference registration begins

	Konferenz 1	Konferenz 2	Konferenz 3	Konferenz 4	Konferenz 5
1430 – 1800	M06 Design solutions: Modern clocking strategies	M07 Power efficiency: Power efficiency in the design of Smart IoT devices	M08 Internet-of-Things: Virtual Platforms in the Internet-of-Things Era – State of the art and perspectives	M09 Secure systems: Emerging Technologies and Hardware Security: Prospects and Challenges	M10 Test and diagnosis: Board-level functional fault diagnosis: industry needs and research solutions

1800 – 2100 Welcome Reception & PhD Forum in Saal 1

TUESDAY 15 MARCH

DATE 16

March 14–18, 2016, Dresden, Germany

TUE

0730	Registration, Entrance area Speaker's Breakfast, Saal 1			
0830–1030	1.1 Opening Session: Plenary, Awards Ceremony & Keynote Addresses			
1030 – 1130	Exhibition and Coffee Break			
	TRACK 1	TRACK 2	TRACK 3	TRACK 4
	Saal 2	Konferenz 6	Konferenz 1	Konferenz 2
1130 – 1300	2.1 Executive Track Panel: Enabling a Connected World via Internet of Things	2.2 Embedded Tutorial: The Dark Silicon Problem: Technology to the Rescue?	2.3 Automotive Systems and Smart Energy Systems	2.4 Physical Design for Cutting-edge Lithography
1300 – 1430	Lunch Break			
	Saal 2	Konferenz 6	Konferenz 1	Konferenz 2
1430 – 1600	3.1 Executive Track Panel: New Opportunities in Automotive Electronics	3.2 Hot Topic: 3D ICs: Leap Forward to 1,000X Performance	3.3 On-Chip Security Testing	3.4 Application-specific Low-power Techniques
1600 – 1700	Coffee Break IP1 Interactive Presentations			
	Saal 2	Konferenz 6	Konferenz 1	Konferenz 2
1700 – 1830	4.1 Executive Track Panel: Trends & Challenges to Ensure Security	4.2 Hot Topic: Nanoelectronic Design Tools Addressing Coupled Problems for 3D-IC Integration	4.3 Firmware Security	4.4 System-level Energy Management
1830 – 1930	EXHIBITION RECEPTION			

PLENARY SESSION	SPECIAL & EU SESSION	D-TRACK
EXECUTIVE SESSION	IP SESSION	A-TRACK
	EXHIBITION THEATRE	T-TRACK
		E-TRACK

Registration, Entrance area Speaker's Breakfast, Saal 1				0730
1.1 Opening Session: Plenary, Awards Ceremony & Keynote Addresses				0830–1030
Exhibition and Coffee Break				1030 – 1130
TRACK 5	TRACK 6	TRACK 7		
Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre	
2.5 Energy Efficient Systems and Architectures	2.6 Fault-Tolerant Embedded Systems	2.7 Variability Challenges in Nanoscale Designs	2.8 Revolutionising the Teaching of Computer Architecture and System on Chip Design	1130 – 1300
Lunch Break				1300 – 1430
Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre	
3.5 Emerging Devices and Methodologies for Energy Efficient Systems	3.6 Timing Analysis and Measurement	3.7 Dealing with Runtime Failures	3.8 Highlights from Exhibition Campus "Ultra-Low Power Technologies (FDSOI)"	1430 – 1600
Coffee Break IP1 Interactive Presentations				1600 – 1700
Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre	
4.5 Ultra-low Energy Memory Devices	4.6 Managing Multi-Core and Flash Memory	4.7 Modeling of Devices and Mixed-Signal Circuits	4.8 Highlights from Exhibition Campus "Automotive Systems"	1700 – 1830
EXHIBITION RECEPTION				1830 – 1930

0730 Registration, Entrance area Speaker's Breakfast, Saal 1				
	TRACK 1	TRACK 2	TRACK 3	TRACK 4
	Saal 2	Konferenz 6	Konferenz 1	Konferenz 2
0830–1000	5.1 SPECIAL DAY Hot Topic: Building Confidence in Advanced Driver Assistance Systems	5.2 Hot Topic: In-memory Computing: Status and Trends	5.3 Physical Attacks and Countermeasures	5.4 Architectural-level Low-power Design
1000–1100	Coffee Break IP2 Interactive Presentations			
	Saal 2	Konferenz 6	Konferenz 1	Konferenz 2
1100–1230	6.1 SPECIAL DAY Hot Topic: Formal Methods for Automotive Software	6.2 Panel: Looking Backwards and Forwards	6.3 Anti-aging and Error protection using Checkpointing and DVFS	6.4 Power Modeling and Power Aware Synthesis
1230–1430	Lunch Break 7.0 SPECIAL DAY Keynotes, 1400–1430, Saal 2			
	Saal 2	Konferenz 6	Konferenz 1	Konferenz 2
1430–1600	7.1 SPECIAL DAY Panel: Which EDA Solutions can the Automotive Domain Reuse? Very Few or All?	7.2 EU Projects Special Session: Energy Efficiency drives Design	7.3 Low Power Devices and Methods for Healthcare and Assisted Living	7.4 System-Level Synthesis
1600–1700	Coffee Break IP3 Interactive Presentations			
	Saal 2	Konferenz 6	Konferenz 1	Konferenz 2
1700–1830	8.1 SPECIAL DAY Hot Topic: Connectivity in the automotive domain: From micro to macro	8.2 EU Projects Special Session: Towards better EU-projects - Success Stories	8.3 Hot Topic: Managing Heterogeneous Computing Resources at Runtime	8.4 Advanced Methods in High-Level Design
1930–2300	DATE Networking Event (DATE Party)			

Registration, Entrance area Speaker's Breakfast, Saal 1				0730
TRACK 5	TRACK 6	TRACK 7		
Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre	
5.5 Alternative Computing Models	5.6 Efficient System Modeling with SystemC	5.7 RF, Power Converters, and ADC: Innovative Design and Test Solutions	5.8 Model Based Design and Verification Day - Exhibition Keynote and Application Talk	0830–1000
Coffee Break IP2 Interactive Presentations				1000 – 1100
Konferenz 3	Konferenz 4	Konferenz 5		
6.5 Biochips	6.6 Modelling and Control of Cyber-Physical Systems	6.7 Fault tolerant systems and methods	6.8 Highlights from Exhibition Campus "5G Wireless Networks"	1100 – 1230
Lunch Break 7.0 SPECIAL DAY Keynotes, 1400 – 1430, Saal 2				1230 – 1430
Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre	
7.5 Emerging Memory Architectures	7.6 Statistical and Symbolic Techniques for the Analysis and Testing of Embedded Software	7.7 Aging mitigation to improve system robustness	7.8 Highlights from Exhibition Campus "IoT and Secure Systems"	1430 – 1600
Coffee Break IP3 Interactive Presentations				1600 – 1700
Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre	
8.5 Non-volatile Memory Design Methodologies	8.6 Dataflow Modeling and Natural Language Processing	8.7 Test Methods Handling Unknowns, 2.50 Integration and Realistic Memory Defects	8.8 Model Based Design and Verification Day - Tutorial: An Industry Approach to FPGA/ARM System Development and Verification	1700 – 1830
DATE Networking Event (DATE Party)				1930 – 2300

0730	Registration, Entrance area Speaker's Breakfast, Saal 1			
	TRACK 1	TRACK 2	TRACK 3	TRACK 4
	Saal 2	Konferenz 6	Konferenz 1	Konferenz 2
0830–1000	9.1 SPECIAL DAY Embedded Tutorial: Embedded Systems Security	9.2 Managing the Traffic Jam in NoC	9.3 Industrial Experiences	9.4 Optimization for Logic and Physical Design
1000–1100	Coffee Break IP4 Interactive Presentations			
	Saal 2	Konferenz 6	Konferenz 1	Konferenz 2
1100–1230	10.1 SPECIAL DAY Hot Topic: Lightweight Security for Embedded Processors	10.2 Does it Work or NoC?	10.3 Design Experiences for Multimedia and Communication Applications	10.4 Stochastic Methods for Circuit Analysis & Synthesis
1230–1400	Lunch Break Best IP Award Presentation, 1315–1330, Saal 2 11.0 SPECIAL DAY Keynote, 1330–1400, Saal 2			
	Saal 2	Konferenz 6	Konferenz 1	Konferenz 2
1400–1530	11.1 SPECIAL DAY Hot Topic: Embedded Security Applications	11.2 Beating New Technology Paths for NoC	11.3 Microarchitec- tures and Work- load Allocation for Energy Efficiency	11.4 Automating Test Generation, Assertions and Diagnosis
1530–1600	Coffee Break IP5 Interactive Presentations			
	Saal 2	Konferenz 6	Konferenz 1	Konferenz 2
1600–1730	12.1 SPECIAL DAY Hot Topic: Design Methods for Security and Trust	12.2 Hot Topic: Exploit- ing New Transis- tor Technologies to Enhance Hard- ware Security (without PUFs!)	12.3 System Support for Resilience and Robustness	12.4 Simulating Everything: From Timing to Instructions

D-TRACK

SPECIAL SESSION

A-TRACK

IP SESSION

T-TRACK

EXHIBITION THEATRE

E-TRACK

Registration, Entrance area Speaker's Breakfast, Saal 1				0730
TRACK 5	TRACK 6	TRACK 7	TRACK 8	
Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre	
9.5 Formal Bit Precise Reasoning	9.6 Real-Time Scheduling	9.7 Temperature Awareness in Computing Systems	9.8 Embedded Tutorial: Analog-/ Mixed-Signal Verification Methods for AMS Coverage Analysis	0830 – 1000
Coffee Break IP4 Interactive Presentations				1000 – 1100
Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre	
10.5 Enhancing Memory in Next-Generation Platforms	10.6 Compilers and Tools for GPUs and MPSoCs	10.7 Reliable System Design	10.8 Highlights from Exhibition Campus "3D-IC Integration"	1100 – 1230
Lunch Break Best IP Award Presentation, 1315 – 1330, Saal 2 11.0 SPECIAL DAY Keynote, 1330 – 1400, Saal 2				1230 – 1400
Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre	
11.5 Design of Efficient Microarchitectures	11.6 Applications of Reconfigurable Computing	11.7 Naked Analog Synthesis	11.8 Launch of the Worldwide MEMS Design Competition	1400 – 1530
Coffee Break IP5 Interactive Presentations				1530 – 1600
Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre	
12.5 Accelerator Design and Heterogeneous Architectures	12.6 Reconfigurable Computing Platforms and Architectures	12.7 Formal System Level Verification	12.8 N.N.	1600 – 1730

0730 –
0830 Workshop Registration and Welcome Refreshments

Breaks Please see individual workshop programmes
for lunch and break times

0830–1700 Konferenz 6	0830–1620 Konferenz 1	0830–1700 Konferenz 5	0830–1500 Konferenz 2
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W01 TRUDEVICE 2016: Workshop on Trustworthy Manufacturing and Utilization of Secure Devices	W02 3rd Workshop on Design Automation for Understanding Hardware Designs, DUHDe 2016	W03 2nd Workshop on Model- Implementation Fidelity, MiFi'16	W04 IMPAC: Getting more for less: Innovative MPSoC Architecture Paradigms for Analysability and Composability of Timing and Power
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0830–1700 Seminar 5-6	0830–1715 Konferenz 3	0815–1700 Konferenz 4	0830–1630 Seminar 3-4
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W05 ERMAVSS: Workshop on Early Reliability Modeling for Aging and Variability in Silicon Systems	W06 The 2nd International Workshop on Optical/Photonic Interconnects for Computing Systems (OPTICS Workshop)	W07 International Workshop on Emerging Memory Solutions	W08 First Workshop on Resource Awareness and Application Autotuning in Adaptive and Heterogeneous Computing
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DATE 17

CONFERENCE 27–31 MARCH
EXHIBITION 28–30 MARCH
LAUSANNE, SWITZERLAND