Read/Write Robustness Estimation Metrics for Spin Transfer Torque (STT) MRAM Cell

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Abstract — **The rapid development of low power, high density, high performance SoCs has pushed the embedded memories to their limits and opened the field to the development of emerging memory technologies. The Spin-Transfer-Torque Magnetic Random Access Memory (STT-MRAM) has emerged as a promising choice for embedded memories due to its reduced read/write latency and high CMOS integration capability. Under today aggressive technology scaling requirements, the STT-MRAM is affected by process variability making robustness evaluation an important concern. In this paper, we provide new metrics for robustness prediction of an STT-MRAM memory cell. Independent *Robustness Margin* metrics are defined for Read Operation and Write Operation based on the electrical characteristics of the memory cell and the fabrication induced variability. These metrics are used to estimate the extreme parameter variation causing the cell failure, Current Noise Margins and the Failure Probability of the STT-MRAM cell.**

Index Terms—STT-MRAM, Robustness, Process Variability, Robustness Margin Metrics

I. INTRODUCTION

The Spin-Transfer Torque Magnetic Random Access Memory (STT-MRAM) is a promising candidate for next generation embedded memories [1]. It offers faster read and write access time and better CMOS integration than other available technologies with similar features. However, the STT-MRAM cell fabrication is facing a set of challenges that impact performance and reliability. These issues are mainly related to process variations of MOS and MTJ devices ([2][3][4][5]), to the high write power consumption ([6][7]), and to the thermal fluctuations in the MTJ switching ([8]).

Process variation effects on STT-MRAM cell have been extensively studied. For instance, [2] provides an overview of the interrelationship between design parameters and parametric failures of STT-MRAM cells in presence of process variations. The authors present a theoretical analysis for modeling the read and write failures of a cell due to the parametric variations of current pulse width and cross-section area. In [3], a magnetic- and electric- level STT-MRAM cell model is proposed. The model is used to evaluate the effect of both thermal fluctuation and switching currents on the switching time of the device. The variations affecting the parameters of the NMOS transistor are not taken into consideration.

Several circuit techniques have been proposed to improve the robustness of an STT-MRAM memory, like multi-terminal structures [9], new design paradigm decoupling conflicting design requirements between read stability and writability [10], or using complementary polarizers in the cell design for self-referencing and improved write current [11]. Traditionally, the robustness of the STT-MRAM cell is expressed in terms of *read stability* and *writability*, concepts based on the operation current.

In this paper, we introduce a new methodology for robustness estimation. The proposed methodology is based on evaluating the electrical characteristics of a memory cell affected by fabrication variability and on defining and evaluating *Robustness Margin* (*RM*) metrics during read/write operations.

The proposed methodology is intended to support design and test engineers during predictive device simulation and memory characterization. Moreover, such methodology enables a significant understanding of design limits and can be integrated with the well-established statistical analyses to provide accurate information about the circuit limitations under process variability. We use the *Robustness Margin* metrics (*RM*) to determine whether a faulty operation can occur, to estimate maximum allowed process variability for correct operation, to extract current noise margins when the fabrication induced process variability is known, and to estimate the failure probability when the fabrication induced process variability causes faulty behavior.

Given the current trend on cell designs with high magnetic bit thermal stability [17], this paper is focused on this class of STT-MRAM cells. The characterization is thus performed on a memory cell designed with large thermal stability. In this way the behavior of the memory cell and block in data retention are stable [13].

This paper is organized as follows. In Section II, the operation principles of an STT-MRAM cell are briefly described, while the failure mechanisms caused by parameter degradation are described in the third section. The fourth section describes the proposed *Robustness Margin* metrics and their evaluation methodology. Section V presents some simulation results for *RM* estimation and discussion on cell robustness. Finally, Section VI concludes the paper.

II. STT-MRAM CELL: OPERATION PRINCIPLE AND ELECTRICAL MODEL

In this section, the STT-MRAM cell operation principle is described, and its reliability estimated under the concurrent effects of process variability and aging effects.

A. Operation Principle

In an STT-MRAM memory, information is stored into a magnetic tunneling junction (MTJ) device. Typically, an MTJ element consists of one oxide barrier layer sandwiched between two ferromagnetic layers (FLs), characterized by their magnetic orientation. One of the two magnetic layers, referred to as *pinned layer*, has a fixed magnetic orientation set at fabrication time, whereas the other, referred to as *free layer*, has a freely rotating magnetic orientation that can be dynamically changed by forcing sufficiently large tunneling currents across the device. The relative magnetic orientations of the two layers defines the conductance of such a tunneling junction. This effect is called *tunneling magnetoresistance* effect (TMR) and it is characterized by means of the *TMR ratio*, which is defined as the relative resistance change between the two magnetized states.

B. Electrical Model of STT-MRAM

When the relative magnetization directions of the two ferromagnetic layers are parallel, the MTJ device exhibits high conductance (low electrical resistance, $R_{MTJ} = R_L$). When, on the other hand, their relative magnetization directions are antiparallel, the MTJ device exhibits low conductance (high electrical resistance, $R_{MTJ} = R_H$). The logic value '0' is associated with the parallel state and the logic value '1' is associated with the anti-parallel state (see Fig. 1(a)). The TMR ratio is therefore defined as: $TMR = (R_H - R_L)/R_L$.

Several STT-MRAM cell implementations have been proposed. In this work we target the popular 1T-1MTJ structure. In this topology, the memory cell consists of one MTJ device connected in series with one NMOS transistor. The cell is accessed by the corresponding control lines, i.e., Bit Line (BL), Source Line (SL) and Word Line (WL). The equivalent electric circuit of a 1T-1MTJ STT-MRAM cell is given in Fig. 1(c).

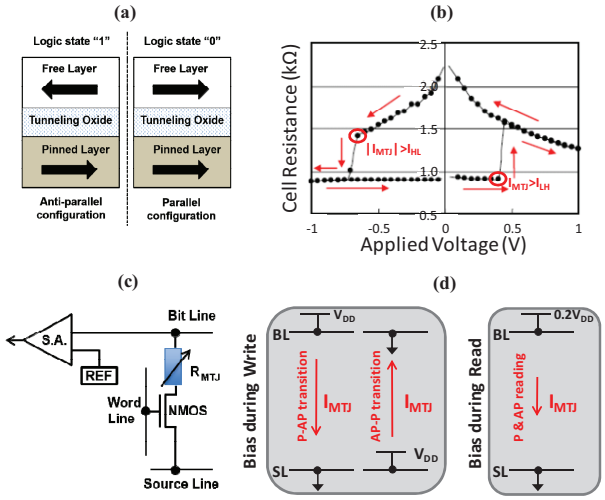

Fig. 1. STT-MRAM Cell basics: a) The MTJ device configurations; b) The $R_{MTJ} - V_{MTJ}$ hysteresis characteristic; c) The electrical model of the 1T1MTJ STT-MRAM cell and d) The bias conditions during write and read operations.

We focus our analysis on the memory cell, hence the peripheral circuitry (sense amplifier – SA and reference cell – Ref) are assumed ideal. The MTJ element is modeled as a variable electrical resistance whose value changes with the voltage applied across the device.

The voltage-resistance dependence of the MTJ device exhibits a hysteresis behavior [12], which, in this work, is modeled using a piecewise linear simplification, as shown in Fig. 1(b). In the same figure, the switching conditions for the magnetic state of the cell are indicated with small circles. Here, I_{HL} represents the switching threshold current from anti-parallel to parallel state, while I_{LH} represents the switching threshold current from parallel to anti-parallel state. The Spin Transfer Torque efficiency is weaker in the parallel to anti-parallel transition than in the anti-parallel to parallel, i.e., $I_{LH} > I_{HL}$.

The switching threshold current ($I_{HL,LH}$) can be calculated as [1][13]:

$$I_{LH,HL} = I_{c0}^{LH,HL} \cdot \left\{ 1 - \frac{k_B \cdot T}{\Delta E} \ln\left(\frac{\tau}{\tau_0} \right) \right\} \quad (1)$$

where $I_{c0}^{LH,HL}$ is the critical switching current at $T=0K$ (for low to high, and high to low transition, respectively), ΔE is the energy barrier height, k_B is the Boltzmann constant, T is the temperature of operation, τ is the width of the write pulse, and τ_0 is the inverse of the attempt frequency.

1) Writing operation of the cell

In order to change the magnetic state of the STT-MRAM cell, there must be sufficient current (I_{MTJ}) flowing through the MTJ element long enough to be able to switch the magnetic orientation of the free-layer [14]. The value of the current required for writing the cell depends on several factors, including the physical dimensions of the cell and the materials used, the temperature of operation, and the duration of the applied voltage signal [15].

When a transition from anti-parallel to parallel relative magnetizations, i.e., a writing '0' operation (*W0*), is desired the power supply voltage (V_{DD}) is applied to Source Line (*SL*), while Bit Line (*BL*) is grounded (Fig. 1(d)), hence a current I_{MTJ} flows in the MTJ device. Provided that $I_{MTJ} > I_{HL}$, the cell switches to the parallel state, in which case, R_{MTJ} becomes equal to R_L. When a transition from parallel to anti-parallel relative magnetizations is desired, i.e., a writing '1' operation (*W1*), the power supply voltage (V_{DD}) is applied to Bit Line (*BL*), while Source Line (*SL*) is grounded (Fig. 1(d)). Provided that the resulting current $I_{MTJ} > I_{LH}$, the cell switches to the anti-parallel state ($R_{MTJ} = R_H$).

2) Reading operation of the cell

During the read operation, a small bias voltage is applied on the control lines (Fig. 1(d)), resulting in a current (I_R). Based on this current a decision is made on the memorized state by comparing it against a reference value (I_{REF}) (Fig. 1(c)). A reading current higher than the reference value ($I_R > I_{REF}$) translates in a read '0' operation, while a reading

current lower than the reference value ($I_R<I_{REF}$) translates in a read '1' operation.

III. Failure Mechanisms of the STT-MRAM Cell

The major sources of process variations in the MTJ electrical response include variations in the tunneling oxide thickness and the cross-section area of the free ferromagnetic layer. Variations in these parameters result in a spread of R_H and R_L values. In addition, the NMOS transistor may also suffer from process parameter variations, which impact its threshold voltage (V_{TH}), resulting in variations of operation current. Under these hypothesis, we perform our analysis starting from a three dimensional space of parameter variations (R_L, R_H, V_{TH}). In this 3D space, the correct/faulty response of the cell has been characterized as explained below.

An STT-MRAM cell can fail due to an unsuccessful write operation (write failure – WF), a destructive read operation (read disturb – RD) or a wrong decision during the read operation (read failure – RF), or due to spontaneous magnetic direction flip during data retention (data retention failure – DRF). In this work, we assume the probability of data retention failure and read disturb to be insignificant, since our analysis and the proposed methodology are focused on a STT-MRAM cell designed with high thermal stability factor [16].

Since the MTJ is in fact the data storing device, and the NMOS transistor acts as the control device, we first focus on the analysis of the constraints to be imposed on the R_{MTJ} for guaranteeing correct cell operation. Once this analysis is concluded, we evaluate the constraints on the NMOS threshold voltage variations as well.

1) Failure mechanisms during write operation

In the case of a writing operation, the current flowing through MTJ has to be large enough, and of sufficiently long duration, to allow the switching of the magnetization direction of the free ferromagnetic layer. To allow for a correct write operation (sufficient current) the high and low values of the MTJ electrical resistance must be below $R_{HMAX\text{-}W}$ and $R_{LMAX\text{-}W}$, respectively.

$$\begin{cases} R_H < R_{HMAX-W} = \dfrac{V_{MTJ}}{I_{HL}} = \dfrac{(V_{BL}-V_{SL})_W}{I_{HL}} - R_{NMOS-W} \\ R_L < R_{LMAX-W} = \dfrac{V_{MTJ}}{I_{LH}} = \dfrac{(V_{SL}-V_{BL})_W}{I_{LH}} - R_{NMOS-W} \end{cases} \quad (2)$$

where V_{MTJ} is the voltage drop on the MTJ element; I_{HL} and I_{LH} are the switching threshold currents for write '0' and write '1' operations, respectively; the $(V_{BL}\text{-}V_{SL})_W$ and $(V_{BL}\text{-}V_{SL})_W$ are the bias voltages during write operation (in our case study, they are equal to the supply voltage (V_{DD})), and $R_{NMOS\text{-}W}$ is the electrical resistance of the NMOS transistor during write operation.

The region in the MTJ resistance space in which the R_H values are higher than $R_{HMAX\text{-}W}$ indicates incorrect low state writing operation (write '0' fault: *W0F*), while the one in which R_L values are higher than $R_{LMAX\text{-}W}$ indicates incorrect high state writing action (write '1' fault: *W1F*). Furthermore, (R_L, R_H) pairs must guarantee that $R_H > R_L$ (*TMR>0%*). All these boundaries are shown in Fig. 2(a) in the two dimensional space of the MTJ resistance.

2) Failure mechanisms during read operation

During read operation the current flowing through the cell (I_R) is compared with a reference value (I_{REF}). The reference current is assumed ideal and equal to the average current flowing through two ideal cells in complementary states, biased for read operation [17]:

$$I_{REF} = \frac{I_{RH} + I_{RL}}{2} \quad (3)$$

where I_{RH} is the read current of the nominal cell in anti-parallel magnetization, while I_{RL} is the read current of the nominal cell in parallel magnetization.

If $I_R<I_{REF}$, the state is read as '1', i.e., the MTJ is in its anti-parallel state, $R_{MTJ}=R_H$. In this case, R_H must be high enough ($>R_{HMIN\text{-}R}$) for the current condition to be satisfied (otherwise a read '1' fault occurs: R1F in Fig. 2(a)). If $I_R>I_{REF}$, the state is read as '0', i.e., the MTJ is in its parallel state ($R_{MTJ}=R_L$). In this case, R_L must be small enough ($<R_{LMAX\text{-}R}$) for the current condition to be satisfied (otherwise a read '0' fault occurs: R0F in Fig. 2(a)).

$$\begin{cases} R_H > R_{HMIN-R} = \dfrac{V_{MTJ}}{I_{REF}} = \dfrac{(V_{BL}-V_{SL})_R}{I_{REF}} - R_{NMOS-R} \\ R_L < R_{LMAX-R} = \dfrac{V_{MTJ}}{I_{REF}} = \dfrac{(V_{BL}-V_{BL})_R}{I_{REF}} - R_{NMOS-R} \end{cases} \quad (4)$$

where V_{MTJ} is the voltage drop on the MTJ element; I_{REF} is the reference current; the $(V_{BL}\text{-}V_{SL})_R$ is the bias voltage during read operation, and, in our case study, it is equal to $20\%V_{DD}$; and $R_{NMOS\text{-}R}$ is the electrical resistance of the NMOS transistor during read operation.

It can be observed that (4) be rewritten as:

$$R_L < R_{LMAX-R} = R_{HMIN-R} < R_H \quad (5)$$

i.e., the intersection between the $R_{LMAX\text{-}R}$ and $R_{NMIN\text{-}R}$ lines lies on the *TMR=0* line (Fig 2(a)).

In order to assure sufficient separation between the I_R currents for read '0' and read '1' operations, the MTJ should have a TMR ratio of 100% or higher (*TMR=1* in Fig. 2(a)). TMR values lower than 100% do not imply read failure, just devices sensitive to perturbations, sense amplifier variability, and so on.

The union of faulty write and faulty read operation regions (red regions in Fig. 2(a)) represents the overall failure region for the cell under analysis, while the remainder of the parameter space represents the acceptance region (green region in Fig. 2(a)), the region in the MTJ resistance space, where the cell operates correctly.

The NMOS transistor also suffers from process variations mainly affecting its threshold voltage. For a more comprehensive characterization of the cell failure mechanisms in the parameter space, a 3rd dimension is added (for the V_{TH}), as depicted in Fig. 2(b). The considerations on the R_{MTJ} do not change; the acceptance region is bounded by the same constraints. However, the

values of these constraints (i.e., R_{HMAX-W}, R_{LMAX-W}, R_{LMAX-R} and R_{HMIN-R}) are dependent on the driving capability of the NMOS transistor (the resistances R_{NMOS-R} and R_{NMOS-W} in (2) and (4)). A low value V_{TH} means higher driving capability of the NMOS, which translates into relaxation of write operation constraints (R_{HMAX-W} and R_{LMAX-W}) and also read operation constrains (R_{HMIN-R} and R_{LMAX-R}). This leads to a larger acceptance region (as shown in Fig. 2(b) bottom cross-section). The situation is reversed when the NMOS threshold voltage is large (see Fig. 2(b) upper cross-section).

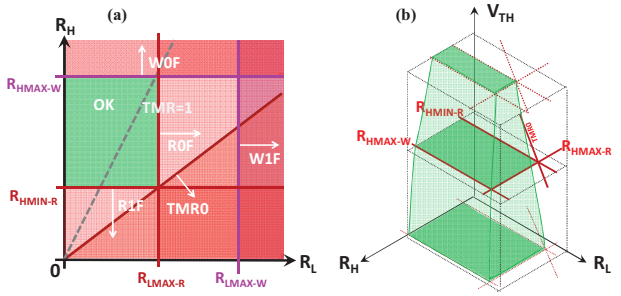

Fig. 2. a) 2D illustration of failure mechanisms constraints during read and write operations of the 1T-1MTJ STT-MRAM. Here *W0F* represents the write '0' failure region, *W1F* represents the write '1' failure region, *R0F* represents the read '0' failure region, *R1F* represents the read '1' failure region, *TMR0* represents the region where TMR<0, and ***OK*** represents the NO failure region, i.e., the acceptance region; b) 3D representation of acceptance region in the (R_L, R_H, V_{TH}) parameter space. Three 'slices' are emphasized: the middle one corresponding to nominal value for V_{TH}, while the top and bottom ones correspond to $V_{TH\text{-}MAX}$ and $V_{TH\text{-}MIN}$, respectively.

IV. Robustness Margin Metrics for STT-MRAM Cell Characterization

In the previous section we have described the failure mechanisms of an 1T-1MTJ STT-MRAM cell during read and write operations and we have defined the extreme operation conditions in terms of MTJ electrical resistance. Building on this failure analysis, we propose metrics for robustness characterization, based on the device electrical resistance. We define the robustness of an STT-MRAM cell as the degree to which the correct operation conditions are satisfied. In this section we introduce and describe our proposed metrics for robustness evaluation (*Robustness Margins - RM and Current Noise Margins - INM*).

1) Robustness Margin Metrics

The *Robustness Margin* metric is evaluated in the MTJ electrical resistance space for single cell (the designed cell, i.e. nominal) and for a cell set (the set of cells resulted after device fabrication).

We define the *Robustness Margin* of one STT-MRAM cell as the minimum distance between its resistance value and the corresponding resistance margin for read and write operation, respectively (Fig. 3(a) and Fig. 3(b)).

$$\text{Read operation}: \begin{cases} RM_{R0} = \min(R_{LMAX-R} - R_L) \\ RM_{R1} = \min(R_H - R_{HMIN-R}) \end{cases} \quad (6)$$

$$\text{Write operation}: \begin{cases} RM_{W0} = \min(R_{HMAX-R} - R_H) \\ RM_{W1} = \min(R_{LMAX-R} - R_L) \end{cases} \quad (7)$$

If the *Robustness Margins* take positive values, the cell can be correctly written and read from, while a negative *RM* signals a failing operation.

The *RM* defines the *variability margins* of a memory cell set for which the statistical distributions of fabrication induced variability of the two resistances are known. In this case, the *Robustness Margins* are evaluated as the minimum distance between the maximum resistance variation point and the first resistance value causing a failure for each operation (Fig. 3(c)).

2) Current Noise Margin Metric

The *RM* can be used to define the *noise margins* of a memory cell, i.e., the maximum current noise tolerated by a cell affected by process variability, before a failure is observed. Starting from (2), (4), (6) and (7), we define the current noise margin metrics (*INM*) as:

$$\text{Read operation}: \begin{cases} INM_{R0} = \dfrac{(V_{BL} - V_{SL})_R - V_{NMOS-R}}{R_{LMAX-R} - RM_{R0}} - I_{REF} \\ INM_{R1} = I_{REF} - \dfrac{(V_{BL} - V_{SL})_R - V_{NMOS-R}}{R_{HMIN-R} - RM_{R1}} \end{cases} \quad (10)$$

$$\text{Write operation}: \begin{cases} INM_{W0} = \dfrac{(V_{SL} - V_{BL})_W - V_{NMOS-W}}{R_{HMAX-W} - RM_{W0}} - I_{HL} \\ INM_{W1} = \dfrac{(V_{BL} - V_{SL})_W - V_{NMOS-W}}{R_{LMAX-W} - RM_{W1}} - I_{LH} \end{cases} \quad (11)$$

where $INM_{R0,1}$ are the current noise margins during the two read operations, $INM_{W0,1}$ are the current noise margins during the two write operations, $V_{NMOS-R,W}$ are the voltage drops over the NMOS transistor during read and write operation, respectively.

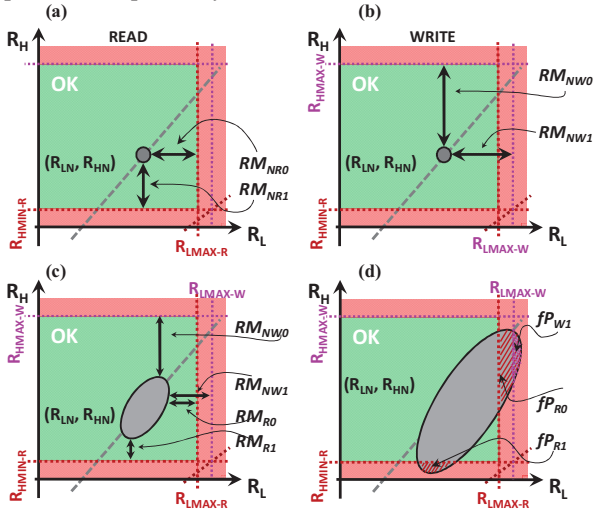

Fig. 3. Graphical representation of the proposed *Robustness Margin* metrics (*RM*): a) RMs defined for read 0 and read 1 operation, respectively; b) RMs defined for write 0 and write 1 operation, respectively, c) RMs defined for read 0, read 1, write 0 and write1 operations no failures occur for a *cell set* d) Failure probability estimation when some of the RM metrics take negative values for a *cell set*.

If one or all *RM* takes negative values, we estimate the *failure probability* under fabrication induced process variability for each operation mode with negative *RM* and

the total cell failure probability. We say that a memory operation if faulty if its corresponding *Robustness Margin* takes negative values. In this case, the *failure probability (fP)* is estimated by integrating the probability distribution function defining the variability of the *MTJ* resistance over the area belonging to the failure region (Fig. 3(d)).

V. Simulation Results

In this section, we provide the robustness analysis of a 1T-1MTJ STT-MRAM memory cell. Its relevant geometrical and electrical parameters are extracted from literature [13][18][19] and summarized in Table I. All parameters are assumed to follow Gaussian distributions.

TABLE I. Parameters of the STT-MRAM Cell

Parameters	Mean(μ)	σ/μ
NMOS threshold voltage (V_{TH})	365mV	10%
Low MTJ resistance (R_{L0}) at zero current	1230 Ω	9.3%
High MTJ resistance (R_{H0}) at zero current	2650 Ω	10.3%
Low state roll-off slope (S_L)	$5x10^4$Ω/A	10%
High state roll-off slope (S_H)	$3x10^6$Ω/A	10%
Critical switching current P-AP (I_{c0}^{LH})	110μA	-
Critical switching current AP-P (I_{c0}^{HL})	60μA	-
Reference current (I_{REF})	31.4μA	-

The nominal values of the MTJ resistances under read and write conditions are extracted from HSPICE simulations, and the characteristic hysteresis curve:

$$\begin{cases} R_{LN-R} = 1225\Omega;\ R_{HN-R} = 2483\Omega; \\ R_{LN-W} = 1199\Omega;\ R_{HN-W} = 2303\Omega. \end{cases} \quad (13)$$

where $R_{L,HN-R}$ represents the nominal electrical resistance of the MTJ in parallel and anti-parallel magnetization, respectively, during read operation (V_{BL}-V_{SL}=*0.2V*), and $R_{L,HN-W}$ represents the nominal electrical resistance of the MTJ in parallel and anti-parallel magnetization, respectively, during write operation ($|V_{BL}$-$V_{SL}|$=*1V*).

Based on this data, on data extracted from HSPICE simulations, and on evaluating (1) - (4), the extreme values of the high and low resistances (boundaries of the acceptance region) together with the resulting *Robustness Margins* are estimated for the cell under analysis. These values are summarized in Table II for different values of thermal stability coefficient (*Δ*) and access time during write operation (*τ*). The thermal stability coefficient (*Δ*) is dependent on the volume of the free layer and on the temperature of the device. Therefore, maintaining the same area (*A*), the thermal stability can be modified by modifying the thickness of the free layer. In this way, the electrical resistance of the MTJ is not affected, since it is only affected by variations of the area of the free layer and not by its thickness.

As described in the previous section, the *Robustness Metrics* can be used to determine the variability margins of the STT-MRAM cell under analysis. The value of *RM* conveys the maximum allowed resistance variability for non-faulty operation. For an easier interpretation of the results, the relative *RM* to the nominal value of the MTJ resistance are depicted in Fig. 4. As expected, the relative *RM* shows that the cell designed with lower thermal stability and written with a longer voltage pulse is the most robust. On the other hand, this cell will have a higher probability of spontaneous data flip due to thermal fluctuations, but these effects do not pertain to our present study, and they will be ignored.

TABLE II. Extreme Values of the R_{MTJ} and the RM Metrics

Operation Conditions	Operation mode	Extreme resistance	RM
T = 300K τ_R = 10ns	Read	R_{LMAX-R} = 1628Ω; R_{HMIN-R} = 1628Ω.	RM_{R0} = *403*Ω RM_{R1} = *855*Ω
Δ=40; τ=20ns; T=300K	Write	R_{LMAX-W} =1525Ω; R_{HMAX-W} = 2983Ω.	RM_{W1} = *330*Ω RM_{W0} =*680*Ω
Δ=40; τ=40ns; T=300K	Write	R_{LMAX-W} = 1595Ω; R_{HMAX-W} = 3038Ω.	RM_{W1} =*400*Ω RM_{W0} =*735*Ω
Δ=70; τ=20ns; T=300K	Write	R_{LMAX-W} = 1519Ω; R_{HMAX-W} = 2971Ω.	RM_{W1} = *324*Ω RM_{W0} =*668*Ω
Δ=70; τ=40ns; T=300K	Write	R_{LMAX-W} = 1561Ω; R_{HMAX-W} = 3002Ω.	RM_{W1} = *366*Ω RM_{W0} =*699*Ω

Another information which can be extracted relates to the preferred stable operation. For instance, if RM_{NW1}>RM_{NR0} and RM_{NW0}>RM_{NR1}, the cell under study is more sensitive to read operations, while if the inequalities are reversed, the cell is more sensitive to the write operation. The results show that robustness during read operations in larger than the one of write operation, with the exception of *Cell2* (*Δ=40*; *τ=40ns*). Another conclusion we can draw is that the maximum MTJ resistance deviation from its nominal value should not exceed *27%* in parallel magnetization, and *29%* in anti-parallel magnetization to assure all cell designs (*Cell1-Cell4*) operate without any faulty behavior. For small memory arrays, where a *3σ statistical interval* is a reasonable assumption, the maximum standard deviations from nominal allowed for the MTJ electrical resistance are: $(\sigma/\mu)_{RH}$ =*9.7%* and $(\sigma/\mu)_{RL}$ =*8%*, respectively. Furthermore, an increase of the NMOS threshold voltage aggravates the situation. The maximum standard deviations from nominal allowed for the MTJ electrical resistance are: $(\sigma/\mu)_{RH}$ =*8.3%* and $(\sigma/\mu)_{RL}$ =*6.9%*, respectively, when V_{TH} is *10%* larger than its nominal value. The extracted values for relative standard deviation values are inferior to the ones given in Table I, i.e., $(\sigma/\mu)_{RH}$=*10.3%* and $(\sigma/\mu)_{RL}$=*9.3%*, respectively.

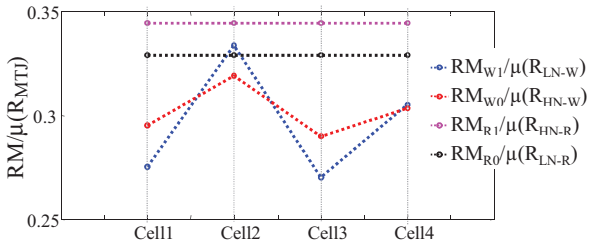

Fig. 4. The relative values of the *Robustness Margin* (*RM*) metrics to the nominal MTJ resistance values, for the four cells under study: (Cell1: *Δ=40*; *τ=20ns*; Cell2: *Δ=40*; *τ=40ns*; Cell3: *Δ=70*; *τ=20ns*; Cell4: *Δ=70*; *τ=40ns*).

A second analysis has been performed assuming the fabrication induced variability of the MTJ resistance be known (given in Table I). The *Robustness Margins* are evaluated as the minimum distance between the maximum

resistance variation point and the first resistance value causing a failure for each operation (Fig. 5).

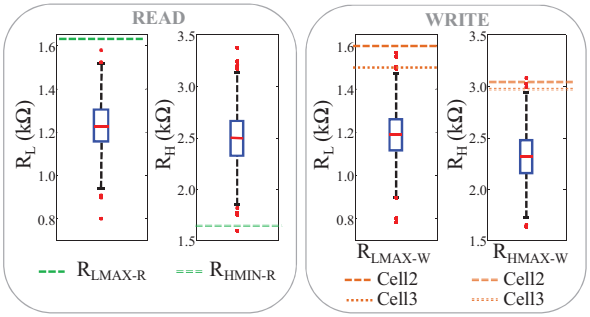

Fig. 5. The box-and-whiskers plots of the MTJ resistance distributions during read and write operations, together with the extreme resistance values for non-faulty operations.

The *Robustness Margins,* resulting current noise margins (*INM*), and the failure probabilities (*fP*) are summarized in Table III.

TABLE III. RM AND INM METRICS AND FP ESTIMATION

Design	RM	INM	*fP*
Cell2&3	RM_{R0} = 27Ω	0.5μA	0
	RM_{R1} = -5.8Ω	-	0.01%
Cell2	RM_{W0} = -4Ω	-	0.01%
	RM_{W1} = 24Ω	5.96μA	0
Cell3	RM_{W0} = -71Ω	-	0.02%
	RM_{W1} = -53Ω	-	0.03%

VI. CONCLUSION

In this paper, we present new *Robustness Margin* (*RM*) metrics for 1T-1MTJ STT-MRAM cell characterization. They are intended to enable the understanding of design limits and identifying the operation conditions in which the cell is more prone to failures. They provide a fast way to estimate maximum allowed process variation for correct operation, to extract current noise margins when the statistical distribution of the cell parameters is known, and to estimate the failure probability when the fabrication induced process variability causes faulty behavior. The proposed *RM* metrics can be used by designers for memory binning and by test engineers to identify the most likely failures.

REFERENCES

[1] M. Hosomi, et al., "A novel nonvolatile memory with spin torque transfer magnetization switching: spin-ram," in IEEE International Electron Devices Meeting IEDM Technical Digest 2005, pp. 459–462.

[2] J. Li, P. Ndai, A. Goel, S. Salahuddin, and K. Roy, "Design paradigm for robust spin-torque transfer magnetic ram (stt-mram) from circuit/architecture perspective," Very Large Scale Integration (VLSI) Systems, IEEE Transactions on, vol. 18, no. 12, pp. 1710–1723, 2010.

[3] Y. Chen, X. Wang, H. Li, H. Xi, Y. Yan, and W. Zhu, "Design margin exploration of spin-transfer torque ram (stt-ram) in scaled technologies," Very Large Scale Integration (VLSI) Systems, IEEE Transactions on, vol. 18, no. 12, pp. 1724–1734, 2010.

[4] W. Zhao and Y. Cao, "New generation of predictive technology model for sub-45 nm early design exploration," Electron Devices, IEEE Trans- actions on, vol. 53, no. 11, pp. 2816–2823, 2006.

[5] K. Munira, W. Soffa, and A. Ghosh, "Comparative material issues for fast reliable switching in stt-rams," in Nanotechnology (IEEE-NANO), 2011 11th IEEE Conference on, pp. 1403–1408, 2011.

[6] Y. Zhang, X. Wang, Y. Li, A. K. Jones, and Y. Chen, "Asymmetry of mtj switching and its implication to stt-ram designs," in Design, Automation Test in Europe Conference Exhibition (DATE), 2012, pp. 1313–1318, 2012.

[7] D. Apalkov, et al., "Spin-transfer torque magnetic random access memory (STT-MRAM)," J. Emerg. Technol. Comput. Syst., vol. 9, pp. 13:1–13:35, May 2013

[8] A. Nigam, C. Smullen, V. Mohan, E. Chen, S. Gurumurthi, and M. Stan, "Delivering on the promise of universal memory for spin-transfer torque ram (stt-ram)," in Low Power Electronics and Design (ISLPED) 2011 International Symposium on, pp. 121–126, 2011

[9] Xuanyao Fong; Roy, K., "Robust low-power multi-terminal STT-MRAM," Non-Volatile Memory Technology Symposium (NVMTS), 2013, pp.1-4

[10] Jing Li; Ndai, P.; Goel, A; Salahuddin, Sayeef; Roy, K., "Design Paradigm for Robust Spin-Torque Transfer Magnetic RAM (STT MRAM) From Circuit/Architecture Perspective," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol.18, no.12, pp.1710-1723, Dec. 2010

[11] Xuanyao Fong; Roy, K., "Low-power robust complementary polarizer STT-MRAM (CPSTT) for on-chip caches," IEEE International Memory Workshop (IMW), 2013, pp.88-91.

[12] K. Lee and S. H. Kang, "Design Consideration of Magnetic Tunnel Junctions for Reliable High-Temperature Operation of STT-MRAM", IEEE Transactions on Magnetics, Vol. 46, n. 6, pp. 1537-1540, June, 2010.

[13] Sato H, Yamanouchi M., Miura K., Ikeda S., Koizumi R., Matasukura F., and Ohno H., "Junction size effect on switching current and thermal stability in CoFeB/MgO perpendicular magnetic tunnel junctions," Appl. Phys. Lett., 99, 042501 (2011).

[14] J. Slonczewski, "Current-driven excitation of magnetic multilayers," Journal of Magnetism and Magnetic Materials, vol. 159, no. 12, pp. L1– L7, 1996.

[15] A. V. Khvalkovskiy, et al., "Basic principles of STT-MRAM cell operation in memory arrays", 2013 Journal of Physics D: Applied Physics 46.

[16] C. W. Smullen et al., "Relaxing non-volatility for fast and energy-efficient STT-RAM caches," IEEE International Symposium on High Performance Computer Architecture (HPCA), pp. 50-61, 2011.

[17] M. Durlam, et al., "A 1-Mbit MRAM based on 1T1MTJ bit cell integrated with copper interconnects," IEEE Journal of Solid-State Circuits, 2003, vol.38, no.5, pp.769-773.

[18] L. Jing, L. Haixin, S. Salahuddin, K. Roy, "Variation-tolerant Spin-Torque Transfer (STT) MRAM array for yield enhancement," IEEE Custom Integrated Circuits Conference (CICC), 2008, pp.193-196.

[19] S. Zhenyu, L. Hai, C. Yiran, W. Xiaobin, "Variation tolerant sensing scheme of Spin-Transfer Torque Memory for yield improvement," IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2010, pp.432-437.