A Closed Loop Transmitting Power Self-Calibration Scheme for Energy Efficient WiNoC Architectures

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***Abstract*—In a wireless Network-on-Chip (WiNoC) the radio transceiver accounts for a significant fraction of the total communication energy. Recently, a configurable transceiver architecture able to regulate its transmitting power based on the location of the destination node has been proposed. Unfortunately, the use of such transceiver requires a costly, time consuming and complex characterization phase performed at design time and mainly based on the use of field solver simulators whose accuracy has not yet been proved in the context of integrated on-chip antennas. In this paper we present a closed loop transmitting power self-calibration mechanism which allows to determine on-line the optimal transmitting power for each transmitting and receiving pair in a WiNoC. The proposed mechanism is general and can be applied to any WiNoC architecture with a low overhead in terms of silicon area. Its application to three well known WiNoC architectures shows its effectiveness in drastically reducing the overall communication energy (up to 50%) with a limited impact on performance.**

I. Introduction

Nowadays, several manycore architectures which use a Network-on-Chip (NoC) as interconnection backbone, are already in the market [1], [2]. The number of processing cores integrated into such architectures is currently in the order of the hundreds and it is expected to exceed the thousand by around 2020 [3]. The ever more increasing number of processing cores, makes the on-chip communication system the main responsible of the scalability limitations, in terms of performance and energy consumption, of next generation manycore architectures. It is mainly due to the multi-hop nature of traditional wire-based NoC architectures in which the communication latency increases with the network size.

To face with this problem, several emerging communication architectures such as 3D-stacked NoC, optical, and wireless NoC (WiNoC) architectures have been proposed [4]. In particular, the latter use a wireless backbone upon the traditional wire-based NoC [5], with the introduction of new elements such as antenna and transceiver. As such elements are fully compatible with traditional CMOS processes, WiNoCs represent a mid-term solution rather than an expensive and/or exotic solution. On the other hand, antennas and transceivers represent an overhead in terms of silicon area and power consumption. With regard to the power issue, the major contribution is due to the radio transmitter front-end connected to the antenna. For instance, in [6] the transmitter is responsible for about 65% of the overall transceiver power consumption, while in [7] this contribution is more than 74%. For this reason, in [8] has been proposed a configurable transmitter that can use different transmitting power based on the physical location of the receiver. It has been shown that such transmitter allows significant energy saving with a negligible impact in terms of area and delay.

The main limitation in [8] is that the transmitter has to be configured offline. In fact, the configuration task requires a long and extensive characterization phase in which either time consuming field solver simulations or direct measures from real prototypes have to be performed. The use of field solver simulators introduces several difficulties and approximations as follows.

- Determining radiating fields in CMOS substrates requires robust and accurate field solvers that have not yet been rigorously tested or verified in the area of integrated on-chip antenna [9].
- Metal structures near the antenna can affect the magnitude of the received signal and several design guidelines have been proposed in order to alleviate this phenomena [10]. Thus, in order to design a robust communication infrastructure, the analysis should take into account metal structures as discussed in [11]. Unfortunately simulating such metal structures at the current level of complexity is unrealistic with the existing CAD tools.
- Field solver simulation cannot take into account interferences (*e.g.*, process variability) that characterize the ultra-deep sub-micron technology nodes.

Based on the above considerations, the wireless medium attenuation levels might be either underestimated or overestimated. In the first case, the reliability of wireless communications is negatively affected due to the increase of the bit error rate which has, in turn, a negative impact on performance due to retransmissions. In the second case, wireless communications will be realized using a transmitting power higher than that needed with a consequent energy waste.

To address these problems, in this paper we propose a closed loop control scheme that dynamically regulates the transmitting power based on the actual attenuation level between transmitter and receiver. The proposed technique is general. It can be applied to any WiNoC architecture improving its energy efficiency with a low overhead in terms of silicon area. The application of the proposed technique to three well known WiNoC architectures shows its effectiveness in drastically reducing the communication energy with a limited impact on performance.

II. Related Work

As the operation frequency of MOS transistors continues to increase, and thanks to the fact that the size of radio-

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frequency devices, such as antennas and inductors, decreases when the operating frequency increases, it is already possible to integrate several radio devices into a single chip [12]. A NoC architecture in which electrical links are replaced by radio transceivers is presented in [13]. Hybrid architectures, in which both traditional wired communications and wireless communication coexist, have been also proposed [14]. Since radio hubs occupies a relevant fraction of the overall chip area, in [15] several criteria to establish the optimum number of wireless interfaces (WIs) under performance constrains have been introduced. In the same work, a new architecture which exploits the *small-world* property [16] has been introduced. An exhaustive overview on WiNoC architectures can be found in [5].

WiNoC architectures introduce new modules such as transceiver and antenna. The role of the transceiver is adapting information for transmission/reception to/from the wireless medium. This task requires an appropriate modulation scheme that, in the context of WiNoCs, is often based on ASK-OOK for its low implementation cost [17]. Given a certain modulation scheme, the desired bit error rate (BER) determines the transmitting power to be used which, in turn, depends on the attenuation level of the wireless medium. The traditional way to estimate such attenuation level is by means of CAD tools, like field-solver simulators, able to simulate the behavior of the electromagnetic fields and waves into silicon substrates. Here, a common design practice is computing the attenuation level for each source-destination pair and then set the transmitting power based on the worst case.

In [8] it has been shown that the variance of the attenuation map is relevant. Such information is used for designing a configurable transmitter which regulates its transmitting power based on the location of the destination node. In this way, the minimum transmitting power for each destination (which guarantees a certain BER) is used, with a consequent improvement of the energy efficiency. The main criticism in [8] is that computing the attenuation map is a difficult, expensive, time consuming, and imprecise task as outlined in the introduction section. In this paper we propose a closed loop transmitting power self-calibration scheme which allows to dynamically adapting the transmitting power of each transmitter in the WiNoC without the need of any expensive offline characterization phase.

III. Background

In this section we introduce the basic theory on how to compute the required transmitting power in order to guarantee a certain BER. Firstly, the Friis transmission is introduced in order to compute the fraction of transmitting power that reaches the receiving antenna. Consequently, the required transmitting power which determines a given BER for the OOK modulation scheme is derived.

A. Friis Transmission Equation

The required transmitting power depends on many factors, including, the kind of modulation, the transceiver noise figure, and the attenuation introduced by the wireless medium. Let us consider the scenario shown in Fig. 1 which consists of a transmitting antenna with an output power P_t and a relative angle of (θ_t, ϕ_t) respect to the receiving antenna, and a receiving antenna, located at distance R, with a relative angle

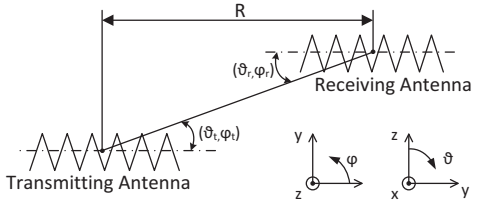

Fig. 1. Friis transmission equation: geometrical orientation of transmitting and receiving antennas. As indicated, considering a spherical coordinate system, ϕ is the azimuthal angle in the XY plane, where the X axis is 0° and Y axis is 90°. θ is the elevation angle where the Z-axis is 0°, and the XY plane is 90°.

of (θ_r, ϕ_r) respect to the transmitting antenna. The fraction of transmitting power G_a, that reaches the terminal of the receiving antenna, P_r, can be computed with the well known Friis transmission equation [18] using scattering parameters S_{11}, S_{12}, and S_{22} as:

$$G_a = \frac{P_r}{P_t} = \frac{|S_{12}|}{(1-|S_{11}|)(1-|S_{22}|)} \tag{1}$$

In practical cases, such parameters should be evaluated by using field solver simulation tools [12] or by direct measures from realized prototypes.

B. Signal Strength Requirements

Eqn. (1) allows to estimate the signal attenuation due to the wireless medium. Since the reliability of the ASK-OOK modulation is related to the energy per bit, E_b, spent to reach the receiver's antenna, we can determine the power required by the transmitter for each value of the attenuation G_a. In particular, for the ASK-OOK modulation the bit error rate can be computed as:

$$BER = Q\left(\sqrt{\frac{E_b}{N_0}}\right) \tag{2}$$

where N_0 is the transceiver noise spectral density and the Q function is the tail probability of the standard normal distribution. Since $E_b = P_r/R_b$, where P_r is the power received at the terminal of the receiver antenna while R_b is the data rate, we can compute the required transmitting power for a given data rate and BER requirement and for a given transceiver's thermal noise as:

$$P_r = E_b \cdot R_b = \left[Q^{-1}(BER)\right]^2 N_0 R_b \tag{3}$$

where Q^{-1} is the inverse of the Q function.

Based on the above considerations, the minimum transmitting power to reach a certain receiver guaranteeing a maximum BER can be computed as:

$$P_t(dBm) = P_r(dBm) - G_a(dB) \tag{4}$$

where $P_r(dBm)$ is given by Eqn. (3) while $G_a(dB)$ is computed by using a field solver with the Friis formula when power is expressed in dBm.[1]

[1]The absolute power, P, can be expressed in dBm by $P_{dBm} = 10 \cdot \log(P \cdot 10^3)$

IV. Closed Loop Adaptive Transmitting Power

Based on theory introduced in Sec. III, the computation of the minimum transmitting power for guaranteeing a certain BER requires the knowledge of scattering parameters that are difficult to estimate. In this section we present a scheme that allows to avoid the characterization phase for the estimation of the scattering parameters and that uses a closed loop self-calibrating mechanism for optimizing, at runtime, the transmitting power of each transmitter at packet granularity.

A. The Architecture in a Sketch

The core of the proposed architecture is the Variable Gain Amplifier Controller (R-VGA) which is an evolution of the VGA controller presented in [8]. In fact, it introduces the reconfigurability feature to the transceiver which is traditionally considered as a static block in current WiNoC implementations. Since each source/destination pair involves a different attenuation *Ga* (Sec. III-A) and, consequently requires a different transmitting power [Eqn. (4)], the role of the R-VGA is driving the configurable power amplifier of the transmitter [7], [14] by selecting one of the several transmitting power levels based on the destination address of the packet to be transmitted. This operation is supported by means of a lookup table that, given the destination address, returns the optimal transmitting power level for reaching that destination. Such optimal transmitting power is computed at runtime as follows.

The lookup table of the generic R-VGA controller is initially configured for selecting the maximum power level irrespective of the destination. The generic radio receiver R has a set of counters, each associated to a specific transmitter T. $PC[T]$ counts the number of packets received from transmitter T. $PC[T]$ is initialized to a reconfiguration period RP and it is decremented each time R receives a packet from T. When $PC[T]$ is zero and no errors have been detected, the radio receiver R informs the R-VGA of T (through a dedicated control network, *cf.*, Sec. IV-C) of decreasing the transmitting power of T for communications having as destination R. As soon as R detects an error in an incoming packet with source address T, and irrespective of the value of $PC[T]$, R informs the R-VGA of T of increasing its transmitting power for communications with destination R. This simple algorithm is formalized in Alg. 1. The algorithm is activated as soon as a packet is received from T or an error is detected in a packet with source T (in this case *error_detected* is true). The functions SendCmdPLInc(T,R) and SendCmdPLDec(T,R) use the control network for sending a reconfiguration command to the R-VGA of T for increasing or decreasing the transmitting power when communicating with R.

From an architectural viewpoint, Fig. 2 shows a block diagram of the radio transmitter and receiver. The chain of bubbles labeled as *CSw* represents the control network used by the radio receivers for sending commands to radio transmitters for updating their transmitting power levels. In the next subsections, the main elements of the proposed architecture, namely, the R-VGA controller and the control network, will be presented in more detail.

B. Reconfigurable Variable Gain Controller

The R-VGA controller is shown in Fig. 3. It works in two modes, namely, configuration mode and calibration mode. In the configuration mode (UPDATE is high), the entry of the lookup table selected by the HUB ADDR input is updated based on the status of the input UP/DOWN. If UP/DOWN is high, the power level stored in such entry is increased, otherwise it is decreased. In the calibration mode (UPDATE is low), the output PWR LEVEL provides the content of the entry of the lookup table selected by the HUB ADDR input.

Algorithm 1 Proposed closed loop transmitting power self-calibration scheme.

Require: T, *error_detected*

```
1:  if error_detected then
2:      SendCmdPLInc(T,R)
3:      PC[T] ← RP
4:  else
5:      PC[T] ← PC[T] − 1
6:      if PC[T] = 0 then
7:          SendCmdPLDec(T,R)
8:          PC[T] ← RP
9:      end if
10: end if
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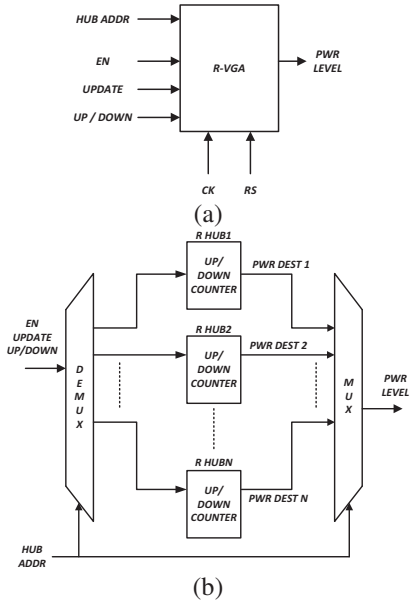


Fig. 3. Reconfigurable Variable Gain Amplifier Controller (R-VGA). Top level view (a) and internal architecture (b).

C. Control Network

The control network allows radio receivers to notify radio transmitters about the opportunity of increasing, decreasing, or not changing their transmitting power. In order to minimize the cost of the control network and given that there are not stringent performance requirements due to the fact that the control messages are dispatched once every RP received flits, we considered a ring based topology for connecting the radio hubs as shown in Fig. 4.

The control switch (*CSw*) receives commands from the radio receiver. A command is a 3-tuple $(addr_{rx}, addr_{tx}, cmd)$. $addr_{rx}$ is the address of the current radio hub. $addr_{tx}$ is the address of the transmitting radio hub whose transmitting power has to

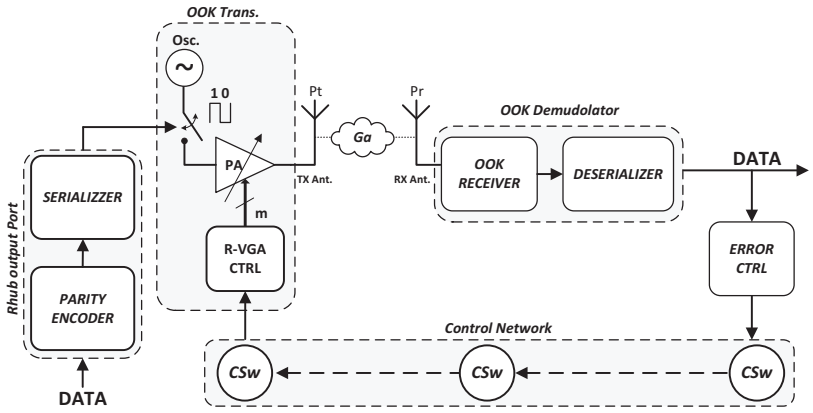


Fig. 2. Block diagram of the architecture implementing the closed loop transmitting power self-calibration scheme.

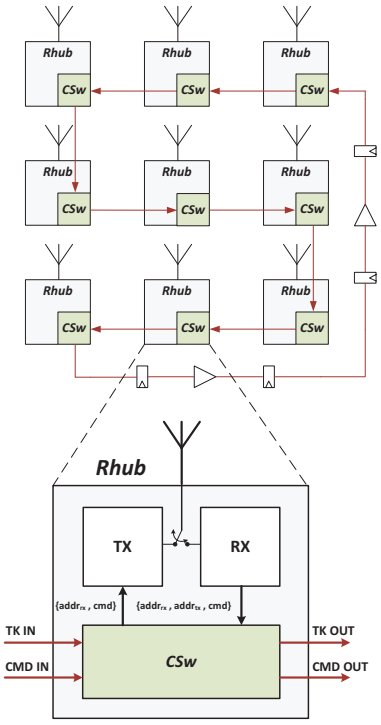


Fig. 4. Control network: a possible floor-plan for a WiNoC with 3×3 radio hubs.

be regulated. *cmd* defines how the transmitting power has to be regulated, namely, increased or decreased. *CSw* stores the commands into an internal FIFO buffer. A token circulates among the *CSw*s enabling the *CSw* holding the token to forward the command (at the head of the FIFO buffer) to the output port CMD OUT. The *CSw* that does not hold the token, simply forwards the command received in its input port CMD IN to its output port CMD OUT. Further, if the $addr_{tx}$ field of the received command is equal to the address of the current radio hub, the *cmd* field is used by the R-VGA controller as described in Sec. IV-B. The token is released and forwarded to the next *CSw* through the output port TK OUT when one of the two following conditions is met: 1) the command completes a round trip (*i.e.*, when $addr_{rx}$ is equal to the address of the current radio hub), or 2) the internal FIFO buffer is empty.

TABLE I
HFSS SETUP PARAMETERS.

Parameter	Value
Chip Size	20 mm $\times$ 20mm
Technology	28 nm SOI
Silicon Resistivity	$\rho = 5$ KΩcm
Substrate Thickness	350 μm
Oxide (SiO_2) Thickness	30 μm
Antenna Elevation	2 μm
Antenna Thickness	2 μm
Antenna Axial Length	2×340 μm
Operation frequency	60 GHz
Absolute Bandwidth	16 GHz

V. Experimental Results

In order to evaluate the expected attenuations between each transceiver pair, we considered a zigzag antenna modelled and characterized with Ansoft HFSS [19] (High Frequency Structural Simulator). Please note that, the use of HFSS in this analysis is for determining the attenuation levels that are used by the simulator for estimating the bit error rate starting from the transmitting power. In fact, the application of the proposed technique does not require the knowledge of the attenuation levels. Tab. I shows the setup parameters. We considered the transceiver proposed in [7], also used in [14], which provides seven adjustable output power steps.

The estimated transmitting power ranges from 8 μW (-21 dBm) to 794 μW (-1 dBm), that in terms of energy per bit correspond to 0.42 pJ/bit and 1.4 pJ/bit, respectively. Based on this, we have selected seven equally spaced power steps into such range. Precisely, the i-th power step is $8 + (i-1) * 786/6$ μW.

For estimating the overhead due to the control network, R-VGA, and the encoding/decoding logic for the error detection, they have been modelled in VHDL and synthesized using Synopsys Design Compiler considering a 28 nm CMOS standard cell library from TSMC operating at 2 GHz (based on the working frequency of the synthesized router). Figs. 5(a) and 5(b) show the area and power breakdown of the radio hub, respectively. Some of the elements which form the radio hub (*e.g.*, the R-VGA, the *CSw* of the control network, and the error control logic) depend on the number of radio hubs

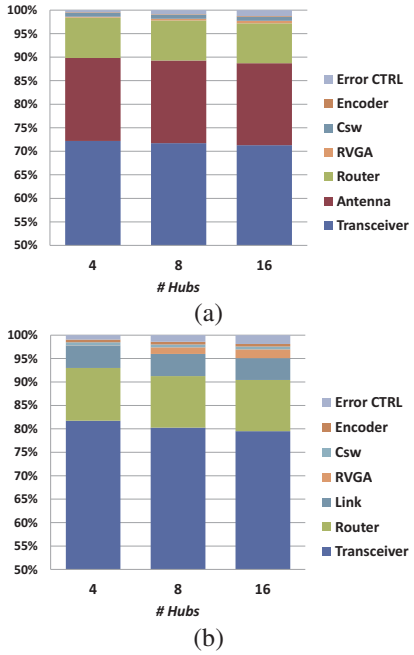


Fig. 5. Area (a) and power (b) breakdowns of the radio hub for three network configurations with 4, 8, and 16 radio hubs.

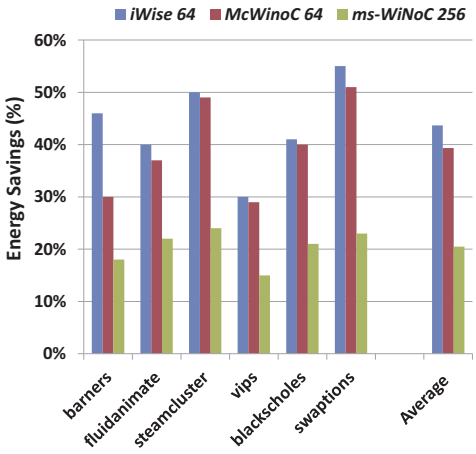


Fig. 6. Energy savings obtained by applying the proposed technique on three different WiNoC architectures.

in the networks. This is due to the fact that the number of bits used for encoding the address of the radio hub and the number counters in the R-VGA depend on the total number of radio hubs in the network. For this reason we considered three scenarios corresponding to a network in which 4, 8, and 16 radio hubs are used. As it can be observed, in the worst case analyzed, the total overhead for implementing the proposed scheme does not exceed 2.6% and 5% of the radio hub area and power, respectively.

Energy figures have been used for back-annotating a cycle accurate NoC simulator based on Noxim [20] and augmented with wireless communication. The attenuation map has been obtained by HFSS and used as input by the simulator for the injection of errors in wireless communication. Simulations have been performed considering three typical WiNoC

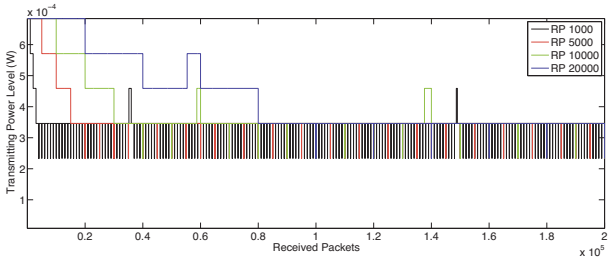


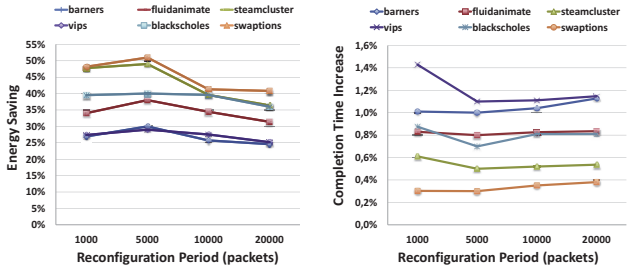
Fig. 7. Variation of the transmitting power level selected at runtime for different reconfiguration periods *RP*.

architectures, including, two mesh-based WiNoC architectures, namely, McWiNoC [21] and iWise64 [14], and a small-world based WiNoC, namely, mSWNoC [15]. For this latter, the optimum number (twelve) and optimal location of radio hubs, computed using the approach presented in [15], has been considered. Fig. 6 shows the energy savings obtained by applying the proposed technique. As it can be observed, on average, the application of the proposed scheme results in an energy saving of 40%, 39%, and 21% for McWiNoC, iWise64, and mSWNoC, respectively.

The less effectiveness of the proposed scheme when it is applied to mSWNoC is due to three main reasons. First, the number of radio hubs used in mSWNoC is less than that used in McWiNoC and iWise64. Second, on average, the utilization of the radio medium by mSWNoC is less than that of McWiNoC and iWise64. Third, in mSWNoC radio communications are mainly used for long-range communications whereas in McWiNoC and iWise64 a relevant fraction of radio communications involve even mid-range communications. Thus, since the communication energy reduction of the proposed technique is as higher as lower is the attenuation level between the source and destination node, and due to the fact that low attenuation levels are mainly observed when source and destination nodes are close each other, the energy saving is more relevant in McWiNoC and iWise64 than mSWNoc.

The above analysis has been carried out using a reconfiguration period *RP* (Sec. IV-A) of 5,000 packets. In fact, the performance and energy figures of the proposed scheme depend on *RP* as it determines the frequency with which the transmitting power level is selected as shown in Fig. 7. For the sake of example, the figure shows the variation of the transmitting power level for different reconfiguration periods *RP* and for a transmitting and receiving radio hub distant 7.5 mm each other.

Fig. 8 shows the impact of *RP* on energy and delay metrics. Although the results refer to the application of the proposed technique to McWiNoC, the same conclusions are valid for the remaining architectures. A low *RP* value makes the system more responsive and more rapid in selecting low transmitting power levels. If from one hand it has a positive impact on energy saving (since lower power levels are more frequently selected), on the other end, errors are more frequently detected (since the bit error rate increases) with a consequent latency and energy penalty due to retransmissions. Conversely, a high *RP* value makes the system less responsive in terms of its adaptation to the optimal transmitting power. At the same time, as soon as the optimal transmitting power level is selected,



(a) (b)

Fig. 8. Impact of the reconfiguration period, *RP*, on energy (a) and execution time (b).

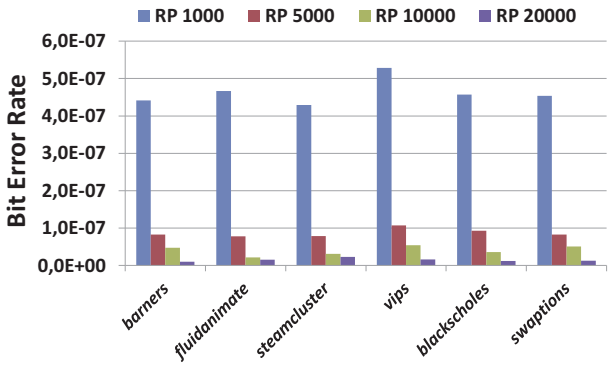


Fig. 9. Measured BER for different reconfiguration periods.

it is maintained for long time with a consequent reduction of retransmissions. Fig. 9 shows the measured bit error rate (BER) for different reconfiguration periods. As it can be observed, the measured BER for the case of *RP* 1,000 is, on average, five times higher than the BER measured for the other *RP*s. This difference justifies the higher negative impact on execution time [Fig. 8(b)] when *RP* is 1,000.

VI. Conclusions

State-of-the-art WiNoC architectures assume that radio communications are realized by using the same transmitting power irrespective of the physical location of the transmitting (source) and receiving (destination) node. In [8] it has been shown that 1) transmitting power in on-chip radio communications accounts for a significant fraction of the total communication energy, and 2) the minimum transmitting power for guarantee a certain reliability level (in terms of bit error rate) strongly depends on the physical location of the transmitter (source node) and receiver (destination node). Based on this, in [8] it has been proposed a configurable transceiver able to use different transmitting power based on the physical location of the destination node. Unfortunately, the applicability of [8] requires a complex, costly and time consuming characterization phase performed at design time. Such characterization phase is carried out by means of field solver simulators whose accuracy have not yet been verified in the context of on-chip integrated antenna and in a nanometer regime. To deal with this problem, in this paper we have presented a closed loop transmitting power self-calibration scheme which is able to select, at runtime, the optimal transmitting power for the on-chip radio communications. The proposed technique is general and can be applied to any WiNoC architecture improving its energy efficiency and with a negligible overhead in terms of silicon area. It has been applied to three well known WiNoC architectures showing its effectiveness in drastically reducing the overall communication energy (up to 50%) with a limited impact on performance.

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