Layout-Aware Sizing of Analog ICs using Floorplan & Routing Estimates for Parasitic Extraction

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***Abstract*—The design of analog integrated circuits (ICs) is characterized by time-consuming and non-systematic iterations between electrical and physical design steps in order to achieve successful post-layout designs. This paper presents an innovative methodology for automatic optimization-based sizing of analog ICs that takes into consideration complete layout-related data for both circuit's geometric requirements, which are obtained from the real-time in-loop floorplan packing, and circuits' electrical performance that is evaluated using circuit simulator and considering accurate layout parasitic estimates. In order to boost the parasitic extraction efficiency, the need for expensive detailed layout generation, as found in previous state-of-the-art layout-aware sizing approaches, is here circumvented. However, the interconnect parasitic capacitances that are major contributors to performance degradation and on-die signal integrity problems, must be accurately accounted for. Therefore, an empirical-based parasitic extraction is performed on an early-stage layout obtained from the floorplan, computing the optimal electromigration-aware wiring topology and shortest rectilinear paths in-loop, without the need for detailed routing. Finally, the methodology is demonstrated for the UMC 130nm design process using well-known analog building blocks proving the generality, accuracy and fast execution of the proposed approach.**

I. Introduction

The absence of mature computer-aided-design tools for electronic design automation (EDA) for analog IC creates a great dependence on human intervention in all phases of the design process, which, despite being supported by circuit simulators, layout editing environment and verification tools, results in a time-consuming and error-prone design flow. In the traditional flow, the layout generation task is only triggered when the sizing task is complete. However, to achieve post-layout successful designs that meet all specifications, time-consuming and non-systematic iterations between these electrical and physical design phases are required. Without them, performance overdesign results in wasted power and area, and if underestimated, the circuits' post-layout performance can be compromised [1][2].

Thus, to address post-layout performance degradation and geometric requirements earlier in the design flow, the, so called, layout-aware or layout-driven design approaches include layout effects during the sizing loop. However, both complete automatic layout generation and parasitic extraction are still time consuming and hard to setup operations [3]. The time cost appears either in the processing time, when using custom automatic layout generator plus layout extraction inside the sizing optimization loop [4], or in the design time of circuit specific template-based [2][5] or procedural [3][6][7][9] generators with parasitic estimation.

Automatic layout generation for accurate parasitic extraction is the bottleneck of layout-aware methodologies. This paper presents a methodology for automatic layout-aware sizing of analog ICs that uses a built-in extractor to accurately compute the impact of parasitic from both floorplan and early-stages of routing. The computational efficiency is improved by avoiding the need of a time-consuming detailed layout generation needed by off-the-shelf tools for parasitic extraction. Moreover, prior knowledge of the circuit's parasitics is not required, i.e., there is no need for circuit specific equations or models [9]. The applicability of the approach is demonstrated with post-layout performances attained for the circuits designed with the proposed layout-aware methodology, versus, the traditional optimization-based sizing.

This paper is organized as follows. In Section II, an overview of the related work is presented. Section III introduces the AIDA's layout-aware flow and Section IV the in-loop layout generation. In Section V the geometric layout properties and estimated parasitics are detailed, after, in Section VI the experimental results and, finally, in Section VII, the conclusions are drawn.

II. Related Work & Contributions

The automation of analog circuit sizing is commonly achieved using optimization-based techniques that may or may not use a circuit simulator to evaluate the performance of tentative solutions during sizing [8], as shown on Fig. 1. In layout-aware approaches, integrating layout generation or layout-related data in sizing optimization helps trim down effects of parasitic disturbances that affect analog circuits' performance, along with realistic considerations for geometrical requirements [2].

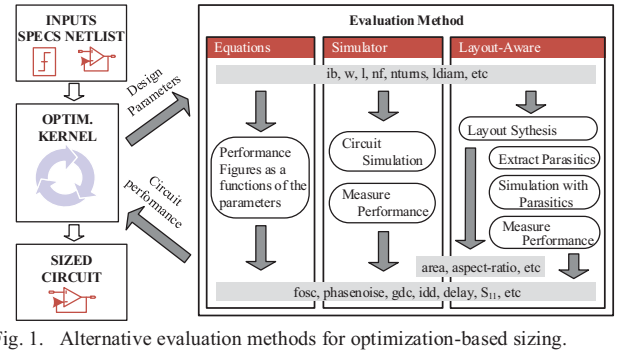

Fig. 1. Alternative evaluation methods for optimization-based sizing.

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In Table I a summary of the state-of-the-art approaches is presented. The key points of the overviewed tools can be summarized as follows:

- In [3][6][7][9] parametric generators, on which the whole layout of the circuit is coded and require huge setup times, are used (in-loop or for layout sampling). In [2][5] the flexibility of the floorplanner is improved by the use of a template approach supported on a slicing model, however, due to the multitude of different sizing solutions found throughout the whole Pareto solution set it is almost impossible to pack all the solutions properly. The alternative is fully automatic generation with an exhaustive search [4], but at expense of an increase in computation time. However, for all approaches, routing setup/template is the same for all design solutions and is not fitted to the solutions as they vary in a multitude of devices' sizes/shapes and performances.
- Interconnect parasitc capacitances are pointed as major contributors to performance degradation and signal integrity problems [10]. These parasitic are obviously dependent of the wire topology (WT), i.e., terminal-to-terminal connectivity, selected and total wiring area and congestion attained by the end of the routing phase. Moreover, routing quality is strongly related with electric-currents measured for the corresponding circuit sizing, but this is seldom considered.

The contributions of the proposed methodology, also presented on Table I, can be listed as follows:

- In the proposed layout-aware flow with AIDA, the embedded layout generator computes the optimal electrical-current correct WT and global routing in-loop for each different sizing solution, which was never considered on previous approaches to layout-aware electrical sizing. In this way, not only the geometric requirements of the floorplan and parasitic-aware performances, but also, the routing quality will follow the optimization process.
- By using a lightweight built-in extractor it is possible to accurately compute the impact of layout parasitics for both floorplan and early-stages of routing, without requiring a detailed and final layout (i.e., all design-rules and layout-versus-schematic errors solved), unlike previous approaches. Traditionally, the last step required in the automatic layout generation flow is the detailed routing, which is by far the most computational intensive and time consuming step. By avoiding the need of a detailed layout and consequently an external extractor, the overall optimization time is greatly reduced.

III. AIDA'S LAYOUT-AWARE SIZING FLOW

The analog IC design automation framework, AIDA [11], implements an automatic design flow from circuit-level specification to physical layout description. AIDA's original flow evolved to cover layout-aware sizing and is illustrated in Fig. 2.

The optimization-based circuit-level sizing is carried by AIDA-C [12], where the circuit's performance is measured using the electrical circuit simulators Spectre®, Eldo® or HSPICE®. The circuit is optimized by an NSGA-II multi-objective multi-constraint kernel, using simulated binary crossover and mutation operators, tournament selection, and constrained-based dominance check, modified to evaluate the fitness of the individuals. The number of design variables defines the space order, while the variable ranges define the size of the search space. The electrical circuit simulator is probably the most well established tool in analog design flow, being used to verify the performance of the circuit since early design stages until post-layout validations. Using circuit simulator eases the inclusion of automation in the design flow, while maintaining accuracy in the obtained solution. The inputs required from the designer are circuit and testbench(es) netlist(s), along with design variables and specifications.

The layout generator AIDA-L [13] (Section IV) was integrated in the loop of the automatic sizing, and generates the layout for each tentative solution at each generation. The inputs are the floorplan constraints and the set of electric-currents for each terminal, specific for each sizing solution, obtained with AIDA-C.

Given the multi-objective optimization performed in AIDA-C, the output of AIDA is a family of Pareto non-dominated layout-aware sized circuits that meet all the specifications in the presence of layout parasitics and geometrical requirements, representing feasible tradeoffs between the different optimization objectives. A Pareto optimal front (POF) for a single ended 2-stage OpAmp is shown on Fig. 3.

By following the loop of the optimization process presented on Fig. 3, the major steps are highlighted by order:

1. AIDA-C selects *i* different sizing solutions, each one with a new set of *x* design variables (e.g., devices' widths, lengths, number of fingers, etc.);
2. For each sizing solution *i* the DC constraints are measured using the electrical simulator, also, the DC electric-currents for each terminal are obtained. If a solution is

TABLE I. COMPARISON BETWEEN STATE-OF-THE-ART WORKS ON LAYOUT-AWARE SIZING

Work	Circuit Synthesizer	Performance Evaluation	Layout Generator		Layout-related data Included	
			Placer	Router	Geometric	Parasitics extracted
Vancorenland et al. [6]	Performance models and Genetic algorithms	Fitted functions	Procedural generator		Equations	1/2-D modeling of the critical nets
Ranjan et al. [3]	Optimization-based	Symbolic models	Procedural generator (design space sampled)		No	Area and interconnect using external extractor
Pradhan [9]	Multi-objective Opt.	Symbolic models	Procedural generator (design space sampled)		No	Bulk, device and interconnect
Youssef et al. [7]	Simulation-based Opt.	Circuit simulator and Design plans	Procedural generator		Yes	Modeling of the stress effects of the devices
Habal et al. [4]	Simulation-based Deterministic nonlinear	Circuit simulator	Enumeration of all possible floorplans	Exhaustive setup for Cadence Chip Assembly Router®	Yes	Complete extraction using Cadence Assura®
Lopez [2][5]	Simulation-based Multi-objective Opt.	Simulator (Spectre® or HSPICE®)	Coded Slicing-tree	Template-based	Yes	3-D analytical-geometrical
This work, AIDA	Simulation-based Multi-objective Opt.	Simulator (Spectre®, Eldo® or HSPICE®)	Multiple B*-trees	Automatic electromigration-aware WT and global routing in-loop	Yes	2-D/2.5-D modeling of the devices and routing

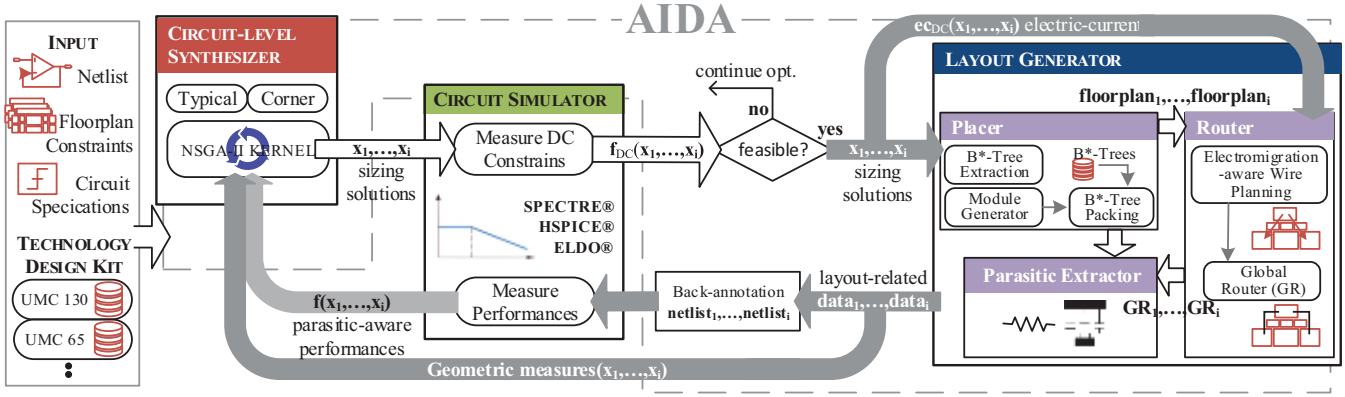


Fig. 2. Layout-aware sizing with AIDA.

unfeasible (i.e., a DC constraint violated) the layout-related data is not considered for further optimization, otherwise, the solution is provided to AIDA-L;

3. AIDA-L generates the *i* floorplans and the one that suits most the geometrical requirements is provided to the Router, where a electromigration-aware wiring topology and global routing is devised for each sizing *i*;
4. The parasitics are extracted using the built-in Pex module and back annotated in the *i* different netlists;
5. The parasitic-aware performances are measured from the complete set of testbenches (DC, AC, TRAN, etc.) using the electrical simulator and used together with the accurate geometrical properties of the circuit, measured by the floorplanner, in the optimization process.

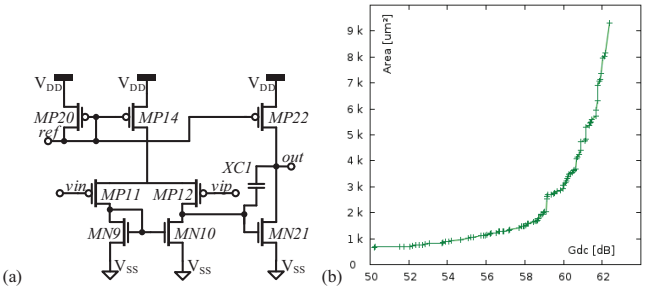


Fig. 3. (a) Single ended 2-Stage amplifier schematic; (b) POF: area versus gain.

IV. AIDA-L: In-Loop Layout Generation

First, the constraint-based Placer is executed, and then, the best floorplan is provided to the fully-automatic Router.

A. Multi-template Contraint-based Placer

In the constraint-based Placer the floorplan is defined using simple rectangular constructs, stored in a template file, that capture the desired proximity and topological relations between cells. These are automatically mapped to multiple B*-tree representations of the floorplan, as described in [13]. However, even the flexibility of a non-slicing floorplan may not be sufficient throughout the whole Pareto solution set of different sizing solutions provided by AIDA-C. The Pareto set encompasses very different circuit solutions and a single template would hardly be the best choice for all, enforcing unreasonable topological constraints in many of them. To prevent such over-constraining of the search space, not one, but multiple topological constraints may be used to allow better packing of the layout throughout the entire solution set. Fig. 4 illustrates 2 different floorplans for the amplifier of Fig. 3 obtained for the same dimensions of the devices, by varying the topological constraints while packing the layout.

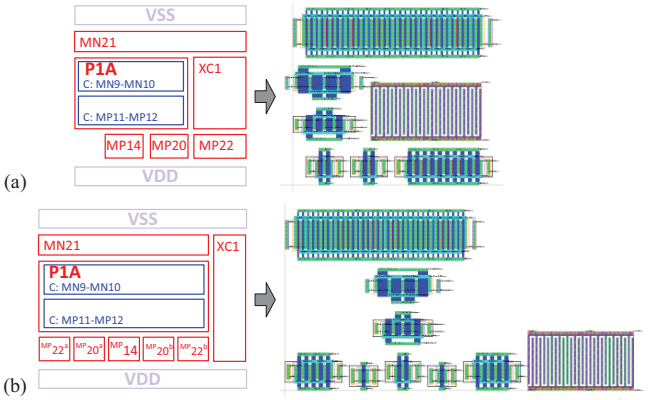


Fig. 4. Different placements for the same sizing with different templates: (a) Template 1, area: 361.7 μm²; (b) template 2, area: 634.7 μm²;

B. Fully-automatic Router

In Fig. 5, the electromigration-aware WT and global routing for only 3 different nets (for illustration purposes) using the floorplan of Fig. 4 (a) are presented.

1) Electromigration-aware Wiring Topology: The pre-parasitic netlist is obviously common to all sizing solutions of a circuit. But given any floorplan and any set of electric-currents for each device terminal, the current-correct tree that provides the optimal terminal-to-terminal connectivity and flows, and that minimizes the wiring area is computed for each of the circuit's nets as described in [14].

2) Global Router: In the global Router, a path-finding algorithm operating over a sparse non-uniform multilayer grid is used to transform the terminal-to-terminal connections into a rectilinear path. The concept of multiport terminal was considered. The ports selected from the corresponding terminals' multiports are the ones that minimize the wire area in the absence of obstacles (i.e., design rules are not enforced in the grid). The width of each wire is a function of the electric-current assigned to it during the creation of the WT [14]. Also, wiring symmetry information is automatically extracted and applied in the global paths.

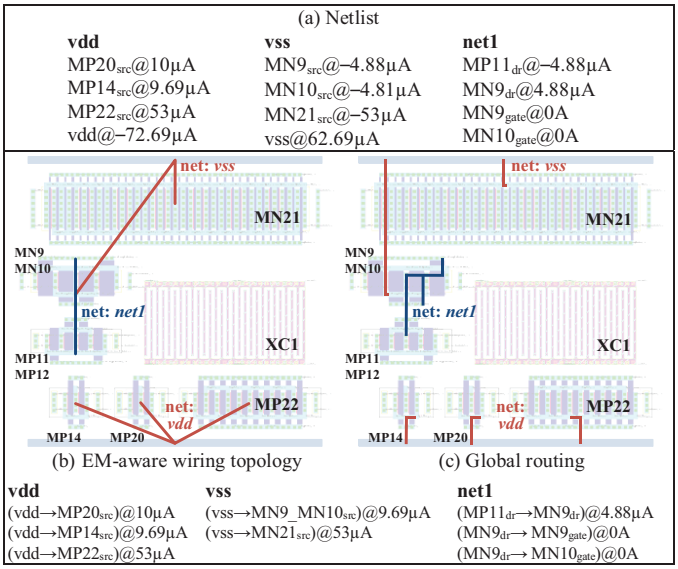


Fig. 5. (a) Netlist and generic electric-currents associated to each terminal; (b) EM-aware wiring topology and (c) global routing. The wires' widths are function of the electric-current imposed on them.

V. LAYOUT-RELATED DATA INCLUDED IN THE CIRCUIT-LEVEL SIZING

There are two sources of layout-related data to be included during the automatic sizing. First, the geometric information from the floorplan, which can be selected as objective or constraint for optimization, and second, the layout parasitics that are back-annotated in the parameterized netlist and whose impact is reflected in the circuit's performance.

A. Floorplan Geometry

The multi-template Placer provides the optimizer with real geometric layout information, e.g., area, width, length, wasted area, etc. All templates are used to produce a floorplan and the best floorplan, i.e., the one with best geometric properties is considered by the optimizer and further provided to the Router. As stated, these geometric measures can be selected as objectives or constraints, and are defined in equation (1). The *global-width*, *global-height*, *area* and *aspect-ratio* refer to the complete floorplan, the *empty-area* is the unused space inside the rectangle delimitating the floorplan, the *empty-area-ratio* is the ratio between the empty-area and the area, and the *max-module-ratio* measures the maximum aspect ratio of the modules and is usually used to constrain the shape of the modules.

$$
\begin{aligned}
&global\_width, global\_height \\
&area = global\_width \times global\_height \\
&aspect\_ratio = \frac{global\_width}{global\_height} \\
&empty\_area = area - \sum module\_area \\
&empty\_area\_ratio = \frac{empty\_area}{area} \\
&max\_module\_ratio = \max_{i=1..D}(module\_ratio_i) \\
&\text{where } module\_ratio = \frac{\max(module\_width, module\_height)}{\min(module\_width, module\_height)}
\end{aligned}
\tag{1}
$$

B. Layout Parasitics

In this subsection, the estimated parasitic resistances of the interconnects, parasitic capacitances between terminals' shapes of the devices, between terminals' shapes and interconnects, and between pairs of global routing interconnects are detailed.

By avoiding an external extractor it is required to derive reliable estimates for the parastics. For MOS transistors it is common the use of geometric methods, where the device's width, length and number of fingers are used in an equation that provides the estimated parasitic. However, the technology-dependency of those equations, the difficulty found to derive them for more complex layout styles (e.g., common centeroid) and the inapplicability to wires, forced a different approach.

1) Parasitic Resistance: The parasitic resistance $R_{parasitic}$ for each wire' segment, which is defined by a *width* and *length*, is computed directly from the resistence per unit quare R_c tabulated for a given conductor, at a temperature T:

$$R_{parasitic} = R_C(T) \times \frac{length}{width} \tag{2}$$

Each wire has any number of segments/bends, so all partial resistance components are considered for square counting, as illustrated on Fig. 6.

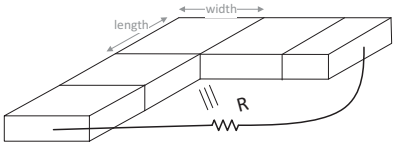


Fig. 6. Parasitic interconnect resistance computed by square counting.

2) Parasitic Capacitances: For capacitive parasitic extraction the alternatives found in the literature are: the computationally expensive numerical methods, which are hardly usable within the optimization loop; approximated analytic methods obtained from electromagnetic models; or empirical techniques, where the extensive experimental data provided by the foundry for a particular technology is used and fitted to a certain model [10]. In our approach, an empirical-based technique where the technology-dependent parameters are obtained for the best possible match it is used. Here, several realistic 3-D effects (e.g., coupling capacitances between two interconnects, crossings in different conductors, etc.) are modeled as a combination of 2-D structures, for a 2.5-D modulation of the problem [15].

a) Substrate/Active area Capacitance: The total substrate/active area capacitance $C_{substrate}$ considered has two components:

$$C_{Substrate} = C_S + C_{power} \tag{3}$$

C_s, which is the sum of the capacitive component between the shapes of a device's terminal (or interconnect) to the plane below, i.e., substrate, well or active areas, as presented in Fig. 7 (a), and is computed according to equation (4):

$$C_S = (C_a(width) \times width) + (2 \times Cf(width) \times length) \tag{4}$$

where the area capacitive component C_a and fringe capacitive component C_f are obtained by interpolation of the technology-dependent data provided by the foundry in function of the conductor's *width*.

C_{power}, are the coupling and lateral capacitances to the corresponding power supply net (e.g., *vdd*, *vss*) that bias the

plane below, and can be computed with the following equations.

b) Coupling Capacitance: It is computed between two conductors (shapes of a device's terminal or interconnet) on different layers, as presented in Fig. 7 (b). The coupling capacitance $C_{coupling}$ has also area and fringe components, as defined in equation (5). If no area component C_a exists the coupling capacitance is ignored.

$$C_{Coupling} = \left(C_a(width) \times overlapwidth\right) + \left(2 \times Cf(width) \times overlaplength\right) \quad (5)$$

c) Lateral Capacitance: The lateral capacitance $C_{lateral}$ is considered between two conductors running in parallel or perpendicular on the same layer, Fig. 8. Here, the fringe components are negligible, and is defined as:

$$C_{lateral} = C_c(width, space) \times parallellength \quad (6)$$

where $C_c(width,space)$ is the coupling capacitive component obtained by the interpolation in conductor's *width* and *space* of the foundry provided values. The C_c value for distant parallel or narrow perpendicular conductors tends to zero.

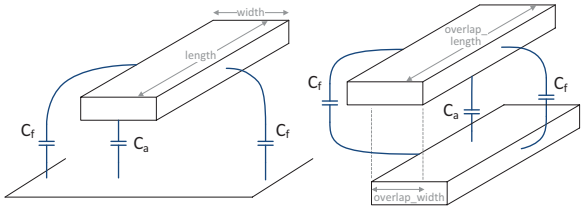


Fig. 7. (a) Parasitic capacitance to the substrate; (b) Coupling capacitance between two conductors on different layers; C_a (area) and C_f (fringe) components.

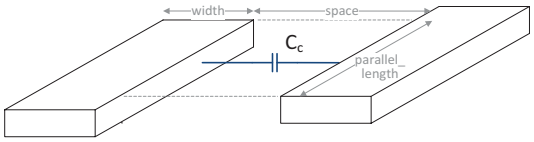


Fig. 8. Parallel capacitance between two conductors on the same layer: C_c (coupling) component.

In Table II some post-layout simulation results for the single ended 2-stage amplifier (Fig. 3) using the developed AIDA's parasitic extractor (PEx) module and a commercial tool are presented.

TABLE II. POST-LAYOUT MEASURES: PARTIAL AND COMPLETE EXTRACTION WITH AIDA'S PEX AND WITH MENTOR GRAPHICS' CALIBRE®

			AIDA's PEx[1]			
	Measure	Netlist	Intra[2]	Floor[3]	All[4]	Calibre®[5]
design1	GBW(Mhz)	55.909	54.290	53.836	53.498	53.039
	PM (º)	54.606	54.330	54.324	53.869	53.745
	NO(µVrms)	180.4	178.5	177.9	178.1	177.6
design2	GBW(Mhz)	88.186	84.857	84.172	83.700	82.652
	PM (º)	53.263	53.114	52.839	52.140	52.184
	NO(µVrms)	203.7	200.4	200.2	200.9	199.7

[1] In AIDA's PEx parasitic are extracted without generating the detailed layout; [2] Only parasitics between module terminals are considered (i.e., C_{gs}, C_{gd}, C_{ds}, C_{gb}, C_{db}, C_{sb}); [3] The parasitic in [2] together with coupling parasitics between terminals of all modules in the floorplan; [4] The parasitics for the interconnects are considered in addition to the previous ones. [5] Extracted with Calibre®, detailed routing generated with AIDA.

The precision lost when using the lightweight AIDA's PEx when comparing to Calibre®, is not only rewarded by the small extraction time required for this simplified PEx, but specially by the fact that the built-in procedure operates over a global routing avoiding the need of the final detailed layout during the optimization iterations. Still it confirms the precision is sufficient to guide the parasitic-aware optimization in the right direction.

VI. EXPERIMENTAL RESULTS

A. 2-Stage Miller Differential Amplifier

The two-stage operational amplifier of Fig. 3, loaded with a 10KΩ resistor in parallel with a 1 pF capacitor and biased with a current of 50µA, is optimized for minimum area. The optimization variables are the width, length, number of fingers and number of rows of the MOS devices, and the length and number of fingers of the MOM capacitor. The performance measures considered are indicated in Table III, and the variables and their ranges are indicated in Table IV.

TABLE III. 2-STAGE AMPLIFIER: PERFORMANCE MEASURES

Meas	Description	Meas	Description
Area	Area	Voff	Structural voltage offset
Gdc	DC Gain	No	RMS noise
Gbw	Unit-gain frequency	Sn	Noise density
Pm	Phase margin	ov[1]	Vgs –Vt[3]
Idd	Current consumption	ov[2]	Vgs –Vt[3]
PSRR	Power supply rejection ration @ 1MHz	d[1, 2]	Vds – Vdsat[3]

[1] The constraint applies to: MP11 and MP12; [2] The constraint applies to MP14, MP20, MN21 and MP22; [3] For PMOS devices the overdrive is Vt – Vgs and delta is Vdsat – Vds

TABLE IV. 2-STAGE AMPLIFIER: VARIABLE RANGES

Variable	Min	Max	Grid
lc[1] [µm]	4.4	100	0.1
nfc[1]	14	198	2
lb[2,3,4], lp[5], lal[6], l2g[7] [µm]	0.120	10	0.05
wb[2,3,4], wp[5], wal[6], w2g[7] [µm]	1	10	0.1
nfbp[3], nfb2[4], nfp[5], nfal[6], nf2g[7]	1	200	2
nrb[2,3,4], nrp[5], nral[6], nr2g[7]	1	4	1

[1] The variables lc and nfc are the length and number of fingers of the MOM capacitor C1; [2] lb, wb and nrb are the length, width and number of rows of MP20; [3] lb, wb, nfbp and nrb are the length, width, number of fingers and number of rows of M14; [4] lb, wb, nfb2 and nrb of MP22; [5] lp, wp, nfp and nrp of MP11 and MP12; [6] lal, wal, nfal and nral of MN9 and MN10; [7] l2, w2 ,nf2 and nr2 of MN21;

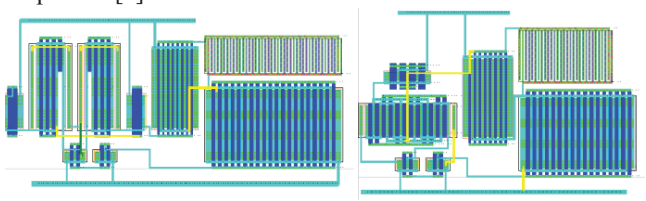
Both the traditional simulation-based sizing and layout-aware sizing were done starting from an already sized solution, but unfeasible for the design constraints shown in the first column of Table V. The first sizing took around 16 minutes while the second took around 40 min. A last step of detailed

TABLE V. 2-STAGE AMPLIFIER: PRE/POST-LAYOUT SIMULATION

		Traditional[1]		Layout-Aware[2]	
	Specs	Pre	Calibre	PEx	Calibre
Area	Min [µm²]	602	**719**	658	
Gbw	≥ 270 MHz	275.71	**263.19**	275.78	272.24
Gdc	≥ 60 dB	62.05	62.02	62.11	62.03
Idd	≤ 2.5 mA	2.09	2.04	1.79	1.75
PSRR	≥ 55 dB	55.03	55.06	55.07	55.04
Voff	≤ 1 mV	0.05	0.05	0.11	0.13
No	≤ 400 µVrms	197.8	199.5	217.3	217.8
Sn	≤ 100 nV/√Hz	8.78	8.93	9.49	9.52
Pm	≥60 º	60.81	**59.22**	60.32	60.30
ov[3]	≥ 50 mV	68.98	68.96	79.71	79.66
ov[4]	≥ 100 mV	120.15	118.54	126.62	124.72
D[3, 4]	≥ 100 mV	108.75	109.24	116.35	116.74

[1] Post layout measures obtained parasitic extraction of the layout shown Fig. 9 (a); [2] Post layout measures obtained after parasitic extraction of the layout shown Fig. 9 (b);[3] The constraint applies to: MP11 and MP12, the value shown is the one closest to the specification limit; [4] The constraint applies to MP14, MP20, MN21 and MP22, the value shown is the one closest to the specification limit;

routing [13] is required to ensure design-rule-correctness of the previous phases and perform parasitic extraction in Calibre®. The performance measures before and after layout are summarized in Table V, and Fig 9 shows the layout for the solutions obtained for both scenarios, after placement and complete routing. The impact of parasitics is not considered in the traditional flow, leading to a post-layout design that does not meet specifications. By considering parasitic effects during the entire optimization, what may look overdesign is in fact a feasible solution when considering the parasitic effects. Like in previous efforts on the area, unit-gain frequency and phase margin are the most sensitive measures for typical analog amplifiers [2].



(a) (b)

Fig. 9. (a) Layout after the traditional simulation-based sizing, using the Layout Generator; (b) Solution obtained using the layout-aware flow, layout after the detailed routing. The figures are in scale.

B. *Folded Cascode OpAmp*

The second example is the folded cascode amplifier of Fig. 10, loaded with a 10KΩ resistor in parallel with a 1 pF capacitor, is optimized for minimum current consumption. The optimization variables are again the width, length, number of fingers and number of rows of the MOS devices, and the length and number of fingers of the MOM capacitor and the bias current.

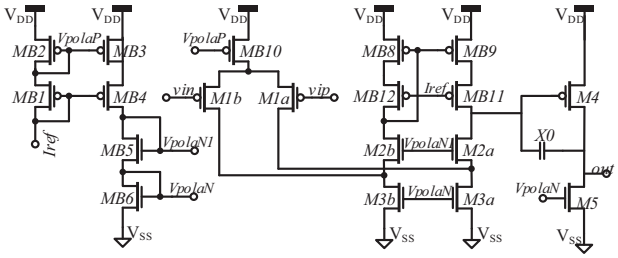


Fig. 10. Folded cascade OpAmp schematic.

Once more, both the traditional simulation-based sizing and layout-aware sizing were done. The first sizing took around 1 hour while the second took around 1.5 hours. The performance measures before and after layout are summarized in Table VI. This circuit has more elements and is larger than the previous one, in this case the difference between PEx and Calibre® are larger, which is due to the fact that the estimates in PEx are somewhat conservative. However, if the detailed routing was considered in the layout-aware optimization, the computational time was expected to increase several hours.

VII. Conclusion

The proposed layout-aware sizing methodology for automatic sizing of analog ICs addresses some drawbacks of the existing state-of-the-art approaches. It merges an in-house circuit optimizer with an in-house layout generator, which offers an innovative solution for parasitic estimation of interconnects by computing the optimal electrical-current correct WT and global routing in-loop for each different sizing solution. The lightweight built-in extractor estimates the impact of layout parasitics for both floorplan and early-stages of routing without requiring a detailed layout, greatly reducing overall evaluation time to in parasitic-aware optimization. Moreover, as the routing template/setup is not fixed, not only the parasitic-aware performances and geometric requirements are considered, but also, the routing topology follows the optimization process. The analog building blocks synthesized for the UMC 130nm, shown the generality, accuracy and fast execution of the proposed approach.

TABLE VI. Folded Cascode Amplifier: Pre/Post-Layout Simulation

Specs		Traditional		Layout-Aware	
		Pre	Calibre	PEx	Calibre
Idd	Min [mA]	5.35	5.35	6.27	6.27
Gbw	≥ 400 MHz	402.07	**389.39**	415.84	425.9
Gdc	≥ 70 dB	73.53	73.53	74.85	74.99
Area	≤ 20k μm²	12.09k	15,89k	16.68k	
No	≤ 500 μVrms	197.05	194.23	199.88	193.38
Pm	≥55 º	57.97	55.24	55.21	56.31
ov	≥ 50 mV	59.48	59.48	59.61	59.51
D	≥ 100 mV	100.33	106.31	101.37	105.03

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