A TSV Noise-Aware 3-D Placer

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***Abstract*—In this work, a three-dimensional partitioning-based force-directed placer is developed to minimize coupling noise between through silicon vias (TSVs) in three-dimensional integrated circuits. TSV decoupling force is introduced and determined by the TSV coupling noise to separate TSVs with strong coupling noise. The experimental results indicate that TSV coupling noise can be effectively reduced by 36.3% on average with only 6.0% wirelength overhead. Besides, the developed 3-D placer shows great performance in wirelength that is competitive to a state-of-the-art 3-D placer.**

I. Introduction

The three-dimensional (3-D) integration technology promises to further increase the integration density, beyond the Moore's Law, and potentially reduce interconnect delays and improve system performance. The shortened wirelength also lessens power consumption of designs. Furthermore, it provides the heterogeneous integration ability by integrating disparate technologies. The main idea of 3-D integration is to use through silicon vias (TSVs) to vertically connect different tiers. Though TSVs play important roles in 3-D integration circuits (ICs), they have negative impacts such as area consumption, routing congestion, and crosstalk issues between TSVs.

As the two-dimensional (2-D) physical design, the placement is a critical stage of 3-D physical designs and significantly impacts the performance of a circuit. Many 3-D placement techniques have been proposed, and the major optimal objective for most of them is still wirelength [1], [2]. Since TSVs can cause area overhead and other negative impacts, the number of used TSVs needs to be considered either. In [1], an analytical placement method was developed to minimize a series of penalty functions including wirelength and TSV number objectives. The bell-shaped function was utilized to define the spreading force of cells and TSVs. In [2], first, a partition process was used to assign cells to different tiers and determine the number of TSVs. Then, a force-directed method [3] was used to spread cells and TSVs. The wirelength of its placement results is shorter than that of [1].

Due to the huge dimension of TSVs, the coupling noise between TSVs is non-negligible [4]–[6], and it might degrade signal integrity (SI) and cause functional errors. To analyze the TSV effect, a high-frequency scalable electrical model of TSV was developed, its electrical behavior was studied, and its impact on physical dimensions and other parameters was investigated in [4]. A compact circuit model of on-chip TSV-to-TSV coupling was developed for the full-chip SI analysis, and two coupling noise reduction techniques, buffer insertion and TSV shielding, were proposed after the cell placement and TSV placement in [5]. Though the coupling model is accurate for two TSVs, it overestimates the coupling capacitance in multi-TSVs. Reference [6] modified and extended it to a multi-TSV version.

In this work, we focus on the crosstalk problem between TSVs and develop a TSV noise-aware 3-D placer. Our contributions are listed as follows.

1) With the circuit partition technique hMETIS [7] and introduced TSV cells, a well-known force-directed 2-D placer SimPL [8] is extended to be the kernel of the proposed TSV noise-aware 3-D placer. After minimizing the number of TSVs by minimizing the cut size between partitions, we assign standard cells to each tier, and define TSV cells. Then, the look-ahead legalization (LAL) algorithm developed by [8] is utilized to spread cells in each tier.
2) To suppress coupling noise of TSVs, the TSV noise-aware 3-D placer utilizes the coupling noise models [5], [6] to define decoupling forces between TSVs and use them to pull apart aggressor TSVs (*a*-TSVs) and victim TSVs (*v*-TSVs) during the global placement stage. To the best of our knowledge, this is the first work to present the 3-D placement by considering coupling noise between TSVs.
3) The developed TSV noise-aware 3-D placer can reduce the total coupling noise of TSVs by 36.3% with only 6.0% wirelength overhead.

This paper is organized as follows. First, Section II reviews the TSV coupling model, and the force directed method used in the developed placer. After that, Section III states our TSV noise-aware 3-D placer by utilizing the TSV decoupling force, and Section IV shows the experimental results. Finally, Section V concludes this work.

II. Preliminaries

A. TSV Coupling Model

Several TSV coupling models have been proposed in recent literature [4]–[6], [9]. Since we are going to use the model in full-chip physical design, a compact model that is accurate enough and supports multi-TSVs should be chosen.

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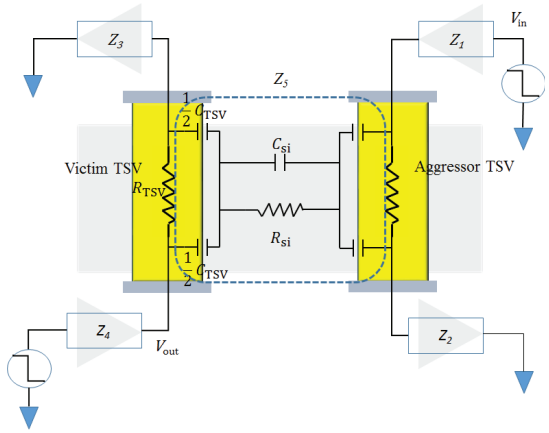


Fig. 1. The 2-TSV model. [5]

As shown in Fig. 1, by modeling a TSV with a resistor (R_{TSV}) and a capacitor (C_{TSV}) in parallel, and the silicon substrate with a resistor (R_{si}) and a capacitor (C_{si}) in parallel, a TSV-to-TSV coupling model was proposed in [5]. Later, Song et. al extended the above model to a multi-TSV coupling model as shown in Fig. 2, and extracted each modeling component as follows [6].

First, R_{TSV} and C_{TSV} can be calculated as

$$R_{\text{TSV}} = \frac{l_{\text{TSV}}}{\sigma_{\text{TSV}} \pi r_{\text{TSV}}^2}, \tag{1}$$

$$C_{\text{TSV}} = \frac{\pi \epsilon_{\text{si}}}{2 \ln(\frac{r_{\text{TSV}}+t_{\text{ox}}}{r_{\text{TSV}}})} l_{\text{TSV}}, \tag{2}$$

where σ_{TSV}, r_{TSV}, l_{TSV}, and t_{ox} are the conductivity, radius, height, and oxide liner width of TSV, respectively. ϵ_{si} is the permittivity of silicon substrate.

After that, the substrate inductance between each pair of TSVs is calculated and utilized to build a $[L_{\text{si}}]$ matrix consisting of self-loop inductances and mutual-loop inductances. Then, the relation between the inductance matrix and the capacitance matrix in a homogeneous medium is utilized to obtain the capacitance matrix $[C_{\text{si}}]$ [10]. The related values are calculated as follows.

$$L_{\text{si},ij} = \begin{cases} \frac{\mu_{\text{si}} l_{\text{TSV}}}{\pi} \ln\left(\frac{d_{i0}}{r_{\text{TSV}}+t_{\text{ox}}}\right) & \text{when} \quad i = j \\ \frac{\mu_{\text{si}} l_{\text{TSV}}}{2\pi} \ln\left(\frac{d_{i0} d_{j0}}{d_{ij}(r_{\text{TSV}}+t_{\text{ox}})}\right) & \text{when} \quad i \neq j \end{cases} \tag{3}$$

where μ_{si} is the permeability of silicon substrate, d_{i0}/d_{j0} is the pitch between aggressor TSV i/TSV j and victim TSV 0, and d_{ij} is the pitch between aggressor TSVs i and j.

$$[C_{\text{si}}] = \mu_0 \epsilon_{\text{si}} l_{\text{TSV}}^2 [L_{\text{si}}]^{-1}, \tag{4}$$

where μ_0 is the permeability of free space.

The coupling capacitance $C_{\text{si},i0}$ and resistance $R_{\text{si},i0}$ between aggressor TSV i and victim TSV 0 can be given as

$$C_{\text{si},i0} = \sum_{k=1}^{N} C_{\text{si},ik}, \tag{5}$$

$$R_{\text{si},i0} = \frac{\epsilon_{\text{si}}}{C_{\text{si},ii} \sigma_{\text{si}}}, \tag{6}$$

where N is the number of aggressors.

The above model is used to determine the coupling capacitances and resistances between TSVs for calculating the coupling noise.

B. Overview of SimPL [8]

A circuit can be represented by a hypergraph $G = (V, E)$. V is the set of cells, and E is the set of nets. Denoting the x-coordinates of cells by a vector $\mathbf{x} = (x_1, x_2, \cdots, x_n)^T$ and y-coordinates by $\mathbf{y} = (y_1, y_2, \cdots, y_n)^T$, generally, the conventional global placement tries to determine physical positions of cells without violating cell density constraints and minimize the half-perimeter wirelength (HPWL) of a design.

$$\phi_N = \sum_{e \in E} \max_{i \in e} x_i - \min_{i \in e} x_i + \max_{i \in e} y_i - \min_{i \in e} y_i. \tag{7}$$

Instead of using (7), the quadratic approximation is used in many placers since it is differentiable, and the optimum can be found efficiently. The new objective is set by pricing every edge by its squared length with a certain weight.

$$\phi_G = \sum_{i,j} w_{x,ij}(x_i - x_j)^2 + w_{y,ij}(y_i - y_j)^2. \tag{8}$$

Equation (8) can be represented as matrix forms.

$$\phi_x = \frac{1}{2}\mathbf{x}^T \mathbf{Q}_x \mathbf{x} + \mathbf{c}_x^T \mathbf{x} + const. \tag{9a}$$

$$\phi_y = \frac{1}{2}\mathbf{y}^T \mathbf{Q}_y \mathbf{y} + \mathbf{c}_y^T \mathbf{y} + const. \tag{9b}$$

The matrix $\mathbf{Q}_x/\mathbf{Q}_y$ captures connectivities between movable cells, and the vector $\mathbf{c}_x/\mathbf{c}_y$ reflects connections of movable cells and fixed modules. $\mathbf{Q}_x/\mathbf{Q}_y$ is positive semi-definite without fixed modules, on the contrary, it is positive definite with fixed modules. ϕ_x and ϕ_y are convex, and their minimum values can be obtained by solving the linear system.

$$\nabla \phi_x = \mathbf{Q}_x \mathbf{x} + \mathbf{c}_x = 0. \tag{10a}$$

$$\nabla \phi_x = \mathbf{Q}_y \mathbf{y} + \mathbf{c}_y = 0. \tag{10b}$$

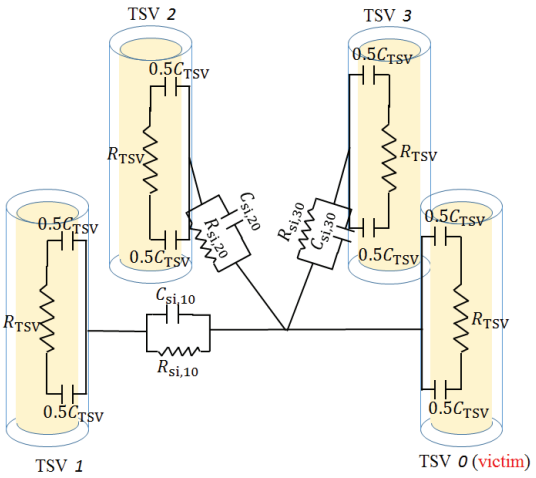


Fig. 2. The multi-TSV model. [6]

Since many nets have more than two pins, to get (8) every multi-pin net should be transformed into a set of 2-pin nets. This work chooses the Bound2Bound (B2B) net model [3] since it can accurately estimate the HPWL in the quadratic objective function ϕ_G. The weights for each p-pin net are

$$w_{x,ij}^{B2B} = \frac{1}{(p-1)|x_i - x_j|}. \tag{11a}$$

$$w_{y,ij}^{B2B} = \frac{1}{(p-1)|y_i - y_j|}. \tag{11b}$$

Solving (10) would lead to considerable cell overlaps. To spread cells, the iterative force-directed approach interprets the quadratic placement problem as a classical mechanics problem of finding the equilibrium configuration for a spring system.

SimPL [8], a flat partition-based and force-directed 2-D placement, shrank the wirelength gap between a upper-bound placement and a lower-bound placement to converge a final placement. A developed LAL algorithm by applying top-down geometric partitioning and nonlinear scaling techniques is applied to build an almost legal upper-bound placement for guiding the spreading force generation. The lower-bound placement is obtained by minimizing the quadratic objective (8) with the spreading force and B2B net model.

The LAL algorithm is briefed as bellow. By splitting up the entire chip into bins, the cell density of each bin is calculated to capture cell distribution. A bin is γ-overfilled if its density exceeds a given threshold γ ($0<\gamma<1$). Adjacent γ-overfilled bins are clustered to form a window by the breadth-first search until the density of expanded window meets the constraint. After that, a cutline C_b from the median of available area inside the window is used to separate the window into two sub-regions. The other cutline C_c from the median of total cell area within the window partitions cells into two sub-groups. Strips are created from boundaries of obstacles within each sub-region and split evenly up to ten if its width is larger than a limited value. Then, cells of each sub-group are scaled to each strip in corresponding sub-region by considering the remaining available area. Hence, C_c moves toward to C_b such that the densities of two sub-regions are equalized, and cells are evenly distributed. These two sub-regions are partitioned recursively to further spread cells in the window until a limited partition level or minimum area of sub-region is reached. The pseudo fixed points from the resulted positions of above procedure are used to evaluate the legal forces that spread cells apart from overlapped regions.

In this work, we implement the SimPL algorithm and adapt it to a 3-D version. Accordingly, we not only use the legal force to spread cells but also utilize our developed decoupling force to pull apart aggressor TSVs and victim TSVs for reducing the noise between TSVs during the global placement.

III. TSV Noise-Aware Placement

The proposed TSV Noise-Aware 3-D Placement is shown in **Algorithm 1**. Given a circuit netlist, first, the k-way min-cut partition is executed by using hMETIS [7] to assign cells to each tier, then, the number of TSVs is determined by the cut size of partition. As all tiers are configured, TSVs are inserted into the netlist as cells. Two TSV cells are built for each TSV i: one TSV cell named TSVi is inserted into the upper tier, and its position in the metal 1 layer is recorded; the other TSV cell named FTSVi is inserted into the lower tier, and its position in the metal top layer is also recorded. Here, i is the index of that TSV. Next, an initial placement is constructed with the B2B net model. After that, the legal force is calculated by the LAL algorithm [8], and the TSV decoupling force is calculated by our decoupling force generation that will be detailed in Section III-B. Then, (10) is solved with simultaneously considering the legal force and TSV decoupling force. The above procedure is repeated until the result is converged. Finally, the detail placement is executed by FastDP [11].

A. TSV Noise-Aware 3-D Placer

1) TSV Cell Connecting: After parsing the netlist of each tier, the pair of TSV cells for each TSV i, TSVi and FTSVi, are connected by giving them the same index of x-direction and y-direction as shown in Fig. 3.(a). This index is used to describe the coordinate of the cell in the linear system matrix. With this setting up, the TSV cells of a TSV are always at the same position after solving the linear system.

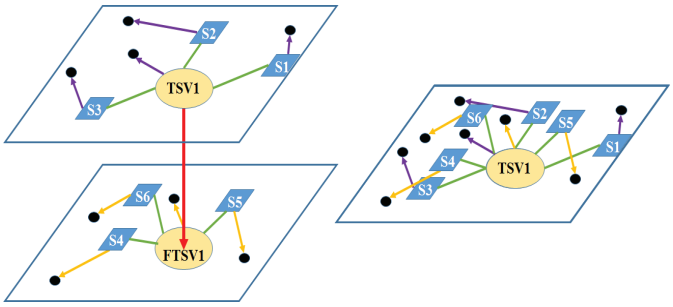
Algorithm 1 TSV Noise-Aware 3-D Placement

```
Partition the netlist into different tiers
Build TSV cells and FTSV cells
for each tier do
    for each TSV do
        Connect its TSV cell to its FTSV cell
    end for
end for
Construct the initial placement
while not convergence do
    for each tier do
        Calculate cell legal force by the look-ahead legalization
        Generate TSV decoupling force
    end for
    Solve the linear system
end while
Detail placement by FastDP
```

2) Initial Placement: The goal of initial placement is to minimize the quadratic approximation of total interconnect length but ignoring the cell overlapping. Our initial placement is obtained by solving the linear system (10) with the B2B net model. Since the B2B net weight is position-dependent, the circuit graph G is updated after solving (10), and each net weight is also updated. This system solving and graph updating procedure is repeatedly performed until the improvement of HPWL is stopped.

3) Global Placement: In the global placement stage, first, with the density distribution of each tier, the LAL algorithm is executed for each tier separately to define the legal force of each cell, and the target position of each functional cell is determined as illustrated in Fig. 3.

Then, the TSV decoupling force for each TSV is calculated by performing the proposed decoupling force generation. With



(a) (b)

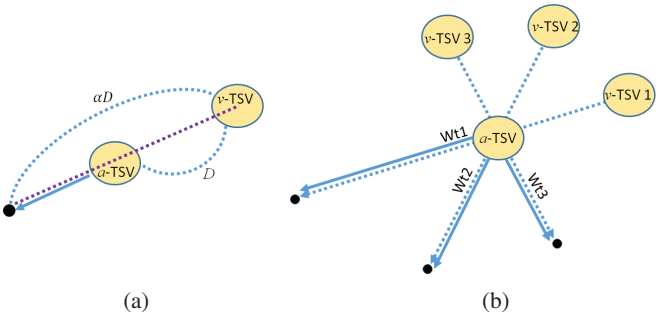
Fig. 3. Target position decision of a 3-D IC. Green lines imply the net connection, red line bounds the upper tier and lower tier TSV cells, black dots are the pseudo fixed points, and purple and wheat lines are the pseudo nets. (a) Side view. (b) Top view.

the legal and decoupling forces of TSV cells, the target position of each TSV is also determined as shown in Fig. 3.

After all the forces and target positions are determined, the linear system (10) is solved with the B2B net model, and the circuit graph G is updated. Finally, similar to the initial placement, the above force calculating, system solving, and graph updating procedure is repeatedly performed until the HPWL of design stops improving for five consecutive iterations, and the improvement of TSV coupling noise is less than 1%.

In our experience, the proposed TSV noise-aware 3-D placement can converge in 50 iterations. Practically, the decoupling force generation step is not activated until a few of iterations, since the TSV decoupling force might disturb the composition of forces, and, hence, influence the wirelength seriously.

4) Legalization and Detail Placement: The legalization and detail placement is done by FastDP [11] tier by tier. First, the top tier with fixed pins is legalized. Then, the coordinates of TSV cells are sent to their connected TSV cells on the next tier, and the next tier is legalized. By this rule, all tiers are legalized, and the placement result is reported.



(a) (b)

Fig. 4. Illustration of the TSV target position determination. (a) The distance between the target node and v-TSV is α times of the distance between a-TSV and v-TSV. (b) Since an a-TSV could be many victims' aggressor, weights are assigned to different pseudo nets for decoupling forces.

B. TSV Decoupling Force Generation

To generate decoupling forces of TSVs, the coupling models reviewed in Section II-A are used to calculate the coupling noise of two TSVs, and the noise is applied to define the decoupling force.

First, the simple lumped RC model is used to model the impedance between a TSV cell and its connected cells, $Z_1 \sim Z_4$, and their wirelength is estimated by the HPWL between a TSV cell and its connected cells. With the estimated HPWL and the parameters of capacitance and resistance per unit length of wire, the equivalent resistance and capacitance values can be calculated. By this way, $Z_1 \sim Z_4$ can be fast and roughly estimated.

After the coupling circuits of all TSVs are determined, each TSV is treated as a v-TSV individually. For each v-TSV, the rest TSVs are sorted by their distances from this v-TSV, and the nearest β TSVs are picked as its a-TSVs. Then, the inductance matrix is constructed by using (3), the coupling capacitance and resistance are calculated by utilizing (4)–(6) for each aggressor, and Z_5 can be built.

Once $Z_1 \sim Z_5$ are determined, using the formula shown in [5], the magnitude of the transfer function of noise for each pair of TSVs represented in Fig. 1 can be derived as[1]

$$|H_{\text{noise}}(j\omega)| = \left|\frac{V_{\text{out}}}{V_{\text{in}}}\right| = \frac{|Z_A|}{|Z_B + Z_C Z_5|}, \tag{12}$$

where

$$Z_A = Z_2 Z_3 Z_4, \tag{13a}$$
$$Z_B = Z_1 Z_2 Z_3 + Z_1 Z_2 Z_4 + Z_1 Z_3 Z_4 + Z_2 Z_3 Z_4, \tag{13b}$$
$$Z_C = Z_1 Z_3 + Z_1 Z_4 + Z_2 Z_3 + Z_2 Z_4. \tag{13c}$$

Though (12) only fits the 2-TSV model, it is still a good reference to see how the aggressor attacks the victim. Given $Z_1 \sim Z_4$, to suppress (12) to reach a noise threshold h_{th} at a given operating frequency ω_{o}, let the coupling impedance Z_5 be changed to αZ_5. To simplify the calculation, a conservative approximation of (12) is used to obtain α as follows.

$$h_{\text{th}} = \frac{|Z_A|}{|Z_B| + |Z_C Z_5 \alpha|}. \tag{14}$$

Therefore,

$$\alpha = \left|\frac{Z_A}{Z_C Z_5 h_{\text{th}}}\right| - \left|\frac{Z_B}{Z_C Z_5}\right|. \tag{15}$$

Z_5 is composed of C_{TSV}, C_{si}, and R_{si}. Since C_{TSV} is fixed with the dimension of TSV, Z_5 only varies with the rest two variables. By replacing R_{si} to be $\frac{\epsilon_{\text{si}}}{C_{\text{si}}\sigma_{\text{si}}}$, the impedance of the parallel connected C_{si} and R_{si} is

$$Z_{C_{\text{si}}} \parallel Z_{R_{\text{si}}} = \frac{R_{\text{si}}}{1 + j\omega C_{\text{si}} R_{\text{si}}} = \frac{\epsilon_{\text{si}}}{\sigma_{\text{si}} + j\omega\epsilon_{\text{si}}} \frac{1}{C_{\text{si}}}. \tag{16}$$

Since (16) is inversely proportional to C_{si}, C_{si} needs to be reduced for increasing Z_5. Hence, heuristically, we increase the distance between this pair of TSVs by α times as illustrated in Fig. 4.(a). The direction of this decoupling force is away from the v-TSV. After the target is determined, an pseudo fixed node is put at the target and connected to the a-TSV with a net. Since an a-TSV could be many victims' aggressor, weight

[1] R_{TSV} is ignored since it is very small.

TABLE II
COMPARISON BETWEEN THE WIRELENGTH-DRIVEN OPTION AND THE TSV NOISE-AWARE OPTION OF THE PROPOSED PLACEMENT.

Ckts	Wirelength-driven				TSV Noise-aware			
	t-Noise (V)	*max*-Noise (V)	HPWL (mm)	Runtime (s)	*t*-Noise (V)	*max*-Noise (V)	HPWL (mm)	Runtime (s)
ckt1	342	1.14	377	42	246	1.14	400	45
ckt2	546	1.18	1030	94	331	1.10	1070	121
ckt3	1255	1.17	3208	460	879	1.15	3352	484
ckt4	1894	1.18	5535	1437	1024	1.08	6061	1414
Average				1.000×				1.015×
Geometric mean	1.000×		1.000×		0.637×		1.060×	

TABLE I
HPWL COMPARISON BETWEEN REFERENCE [2] AND OUR PLACEMENT WITH WIRELENGTH-DRIVEN OPTION.

Ckts	Node# (K)	TSV#	[2]	Our method	
			HPWL (mm)	HPWL (mm)	Runtime (s)
ckt1	25	535	484	377	42
ckt2	69	744	1074	1030	94
ckt3	201	2289	3289	3208	460
ckt4	310	4218	5551	5535	1437
Geometric mean			1.000×	0.924×	

values are assigned to different pseudo nets for decoupling forces as shown in Fig. 4.(b). To take the coupling magnitude into account, the weight is 0.01 times the iteration number and $|H_{\text{noise}}(j\omega_o)|/h_{\text{th}}$.

C. Complexity for Calculating Legal and TSV Decoupling Forces

The time complexity for calculating cell legal forces by the LAL algorithm is $O(n \log n)$ for n cells. The TSV decoupling force generation for p TSVs costs $O(p \log p)$ runtime complexity to sort a-TSVs for a v-TSV, and it takes $O(\beta^3)$ runtime to solve the inverse matrix and calculate the noise and forces for β aggressors, so the complexity of TSV decoupling force generation is $O(p(p \log p + \beta^3))$. Hence, the total runtime complexity is $O(n \log n + p^2 \log p + p\beta^3)$. It can be observed that the TSV decoupling force generation causes little runtime overhead for each placement iteration.

IV. EXPERIMENTAL RESULTS

The developed TSV noise-aware 3-D placer supports two placement options: 1) the wirelength-driven option, and 2) the TSV noise-aware option (simultaneously minimizing wirelength and TSV coupling noise). It is implemented by C++ language and tested on Linux with Intel Core i5-3470 Quad 3.2GHz CPU. The nearest twenty TSVs close to a victim TSV are viewed as its aggressors, and the number of partitions is two. Eigen [12], a C++ template library for linear algebra, is used as our solver. The test circuits are provided by the GTCAD Laboratory [13] and synthesized with the Nangate 45nm open cell library [14]. The legalization and detail placement is performed by FastDP [11].

To verify the results, first, the placement results are routed by SOC Encounter [15]. After routing, the parasitic RC of interconnect is extracted by SOC Encounter. Finally, the coupling noise is evaluated by HSPICE [16].

A. Wirelength-driven Placement Results

The placement results obtained by the wirelength-driven option of the developed 3-D placer are compared with those obtained by a partition-based wirelength-driven 3-D placement method [2] from GTCAD laboratory [13]. Since we only have their placement results, we only compare the HPWL. As shown in TABLE I, the HPWL of our wirelength-driven placement is about 7.6% shorter than theirs on average. The runtime only includes the initial placement and global placement stages since the legalization and detail placement is not executed by our own tool.

B. TSV Noise-aware Placement Results

The quality of the proposed TSV noise-aware 3-D placer is evaluated by the reduction of total coupling noise of TSVs. A 3GHz pulse signal with 1.2V amplitude is simultaneously input to the m nearest TSVs of a victim TSV. The summation of noise measured at the output node of each victim TSV is calculated.

The comparison between the wirelength-driven option and the TSV noise-aware option of the proposed 3-D placer is shown in TABLE II. Here, m is chosen to be 20 for measuring TSV coupling noise. This environment setting might be worse than the practical situation, since, generally, signals might hardly change states simultaneously in so many nets. "*t*-Noise" is the peak-noise summation of all TSVs, and "*max*-Noise" is the maximum peak noise of all TSVs.

TABLE II demonstrates that, with the TSV decoupling force technique, the total TSV noise can be reduced by 36.3% with only 6.0% wirelength overhead on average. The runtime overhead is 1.5% on average, and it is uncertain. Since the number of iterations for the TSV noise-aware option also depends on the coupling noise criterion, it might converge earlier or later than the wirelength-driven option because of different circuits.

Although TABLE II shows that the reduction of maximum peak noise is insignificant, the trend of peak noise distribution moves from the high voltage to the low voltage as illustrated in Fig. 5. For the TSV peak noise distribution of ckt4 (4218 TSVs) as the 20 nearest aggressors close to each victim simultaneously switch, the peak noise over 0.60V is only 5.53% (233/4218) by using the TSV noise-aware option.

However, there are 28.29% (1193/4218) of TSVs over 0.6V by using the wirelength-driven option. After obtaining the placement by executing the proposed TSV noise-aware 3-D placer, according to the design behavior, designers can use the proposed mechanism to decide which TSVs still violate the peak noise limit, and the buffer insertion and TSV shielding techniques [5] can be incorporated to further suppress the high voltage noise.

Figure 6 presents the TSV peak noise distribution of ckt4 with different number of nearest aggressor TSVs close to each victim TSV simultaneously switching. Obviously, as the number of nearest aggressor TSVs decreases, the number of victim TSVs having high peak noise voltages (over 0.6V) is also decreased. The percentage is down to 2.16% (91/4218), 0.12% (5/4218), and 0.00% (0/4218) for m = 15, 10, and 5, respectively.

V. Conclusion

An effective TSV noise-aware 3-D placer by utilizing the decoupling force defined by the coupling noise between TSVs has been built. The experimental results have demonstrated that this technique can reduce total TSV coupling noise effectively with acceptable wirelength overhead. Furthermore, its wirelength-driven placement results are competitive with a state-of-the-art 3-D placer.

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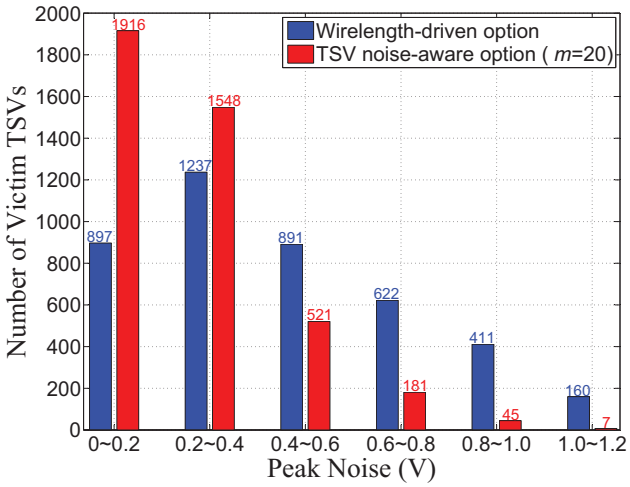

Fig. 5. The TSV peak noise distribution of ckt4 as the 20 nearest aggressor TSVs close to each victim TSV simultaneously switch.

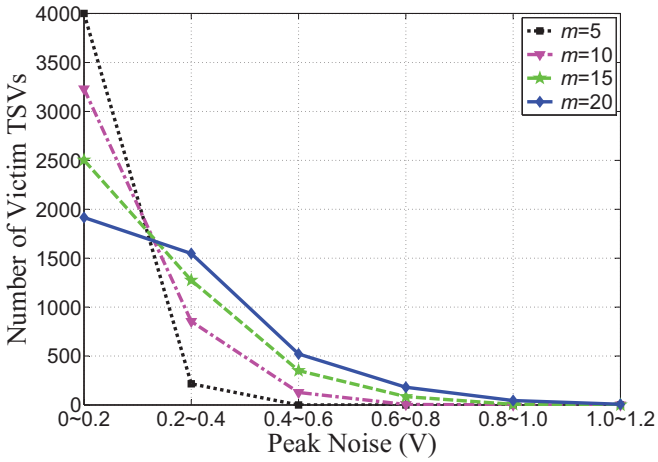

Fig. 6. The TSV peak noise distribution of ckt4 with different number of the nearest aggressor TSVs close to each victim TSV simultaneously switching.

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