Digital Circuits Reliability with In-Situ Monitors in 28nm Fully Depleted SOI

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Abstract— **Aging induced degradation mechanisms occurring in digital circuits are of a greater importance in the latest technologies. Monotonic degradation such as Bias Temperature Instability (BTI) or Hot Carrier Injection (HCI) but also sudden degradation such as Dielectric Breakdown (DB) are identified as the major sources of reliability hazard. The impact of these phenomena on the digital circuits is usually observed in terms of timing degradations and thus may result in setup/hold violation. In this paper we will focus on the impact of aging related degradation mechanisms on timing.**

In-situ monitor is a promising strategy to measure timing slacks and to provide pre-error warnings prior to timing violation. In this paper, we have developed a dedicated test structure to measure and benchmark the behavior of different monitors. The design of monitors is mostly based on delay elements. Three types of delays are proposed in this paper: flip-flop's Master delay, Buffers delay and Passive delay. In addition, we investigate the impact of global and local variations on the accuracy of the measurements by providing complete monitors characterization. The technology used for the test structure and in-situ monitors is 28nm Fully Depleted Silicon On Insulator. Experimental results show a good agreement with SPICE simulation. Finally the proposed in-situ monitors will be compared and their applications to circuit aging prediction will be discussed.

Keywords— in-situ monitors; timing; reliability; BTI; HCI; Dielectric Breakdown; aging; simulations; 28FullyDepleted-SOI.

I. INTRODUCTION

Process, voltage and temperature (PVT) variations must be accurately assessed by simulation to guarantee the functionality without any performance penalty. PVT variations under wear-out mechanism are difficult to handle because it mainly depends on activity, workload and above all, they use conditions responsible for aging.

Several strategies are available to monitor timing degradation under PVT variations during aging.

Replica paths are one of the solutions to mimic the timing behavior of the original path in combinational logic. The effect of temperature or supply voltage reduction of the original delay path can be estimated by measuring the delay of the replicas [1]. However the replica paths suffer local and global variations compared to original path; it results in a drastic inaccuracy and lack of prediction.

Another solution consists in adding in-situ delay monitors to measure the timing inside a real circuit and provide reliable timing information under both local and global variations. The timing is initially impacted by process, voltage and temperature; then by aging induced phenomena with time. Delay monitors, placed at the end of paths, such as "Razor I" [2] and "Razor II" [3] detect timing errors in actual paths and correct them [4, 5]. Slack-probe methodology [6] is another approach which inserts timing slack monitors like probes at a selected set of nets, including intermediate nets along critical paths. The Adaptive Voltage Scaling (AVS) approach in [7] proposes error correction by using in-situ monitors able to detect timing errors.

Another approach consists in detecting timing pre-errors instead of timing errors by detecting critical transitions [8, 9]. In this case, the in-situ delay monitors can be used as a reliability technique to provide alerts prior to timing violations in digital circuit. Indeed circuit timing is degraded with time and in-situ monitors can provide real time information of the timing degradation [10]. Moreover according to the pre-error information, a decision can be made by AVS technique [8, 11], thus the power consumption is reduced and the performance is optimized and compensates the aging.

In this paper, we present different in-situ monitors named Pre-error flip-flops to detect timing pre-errors in digital circuits. Different cell designs of these monitors based on delay elements are proposed, fabricated and measured. A dedicated test structure for characterizing these in-situ monitors is also introduced. Then experimental data of in-situ monitors obtained with the dedicated test structure are compared to Monte Carlo simulations.

Three wear-out mechanisms are investigated and quantified in a delay chain under different activities and stress temperatures: the monotonic degradation by Bias Temperature Instability (BTI) and Hot Carrier Injection (HCI) will be distinguished from sudden degradation by Dielectric Breakdown (DB). These results are then obtained through accelerated stress conditions and projected at nominal operating conditions.

Finally the in-situ monitors are used for reliability monitoring in digital circuits. The different solutions of

monitors are compared and their respective failure rates to guarantee a slack margin consumption are reviewed.

II. Test Structure

The in-situ monitors and their considered test structure in this paper are processed in a 28nm Fully Depleted SOI (FDSOI) CMOS technology. The structure is composed of regular V_{th}-flavor standard cell issued from Design Platform. CAD simulations have been performed with a user defined corner that is aligned with the process.

The dedicated test structure to be used for aging, as depicted in **Figure 1a-b**, is composed of four ring oscillators who play the role of clock and two delay paths. Oscillation frequency can be selected among several values; here we used 500MHz, 1GHz, 1.5GHz and 2GHz.

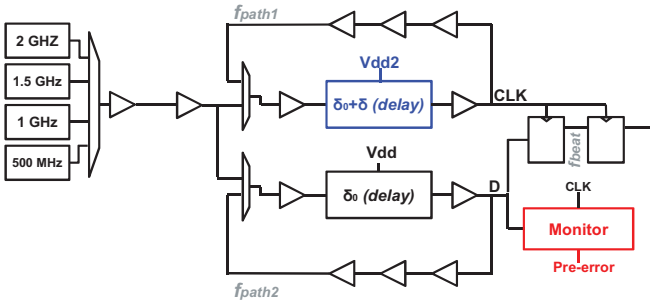

Figure 1a. The architecture of the test structure.

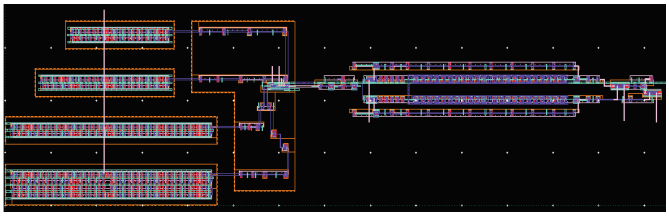

Figure 1b. Layout of the test structure.

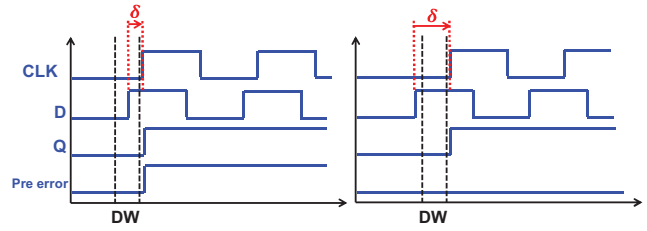

Figure 1c. Timing diagram of the Test Structure during monitoring the delay. The detection window (DW) of the monitor is delimited by black dotted lines. The applied δ delay between CLK and D is delimited by red dotted lines.

In monitor mode, this oscillating signal propagates in two identical paths aimed at generating the clock signal *CLK* and the data signal *D* for testing and characterizing the in-situ monitor. The *CLK* is delayed from the data *D* by applying a δ delay, obtained with a dedicated supply voltage V_{dd2} (see **Figure 1c**). To characterize the monitor, a sweep of V_{dd2} from 0.8V to 1V is performed until the pre-error rises. This sweep of V_{dd2} corresponds to a sweep of δ delay. We first determine the δ delay between D and CLK by determining the minimum V_{dd2} value for which the pre-error starts rising.

In measurement mode, the two paths CLK and D can be individually connected as Ring Oscillators (RO) if the oscillation frequency f_{path1} and f_{path2} need to be measured. The data measured on the circuit is the δ delay between CLK and D. We can obtain it by two ways.

The first method consists in measuring the oscillation frequency of the two paths connected in RO. In this case the δ delay represents the timing difference between these two frequencies. The measurements and simulations of f_{path1}, f_{path2} and δ delay are plotted in **Figure 2**.

The second method consists in extracting the δ delay from f_{beat} measurement and is also the difference between f_{path1} and f_{path2}, as shown in **Figure 3**.

The second method is easier to handle and requires less area. Indeed only a flip-flop (FF with f_{beat} output in **Figure 1.a**) is needed in this case. For the first method, a multiplexer and inverters must be added to create a RO with an oscillation frequency in the range of measurable one. In both cases, an oscillation frequency is measured so the precision depends on the test bench.

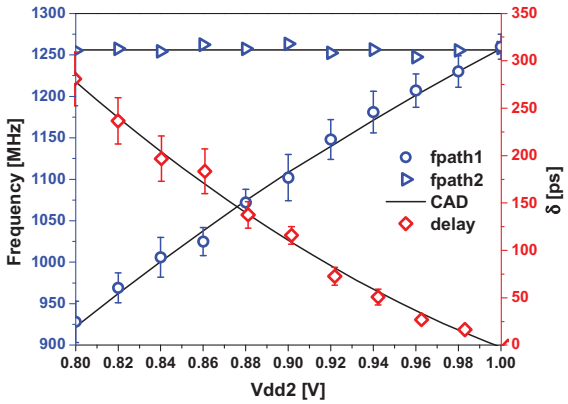

Figure 2. Measurements and simulations of the frequencies (in blue) f_{path1} and f_{path2} and the extracted delay δ (in red) with the supply voltage V_{dd2} at 25°C. A sample of 192 dice has been measured on the same wafer.

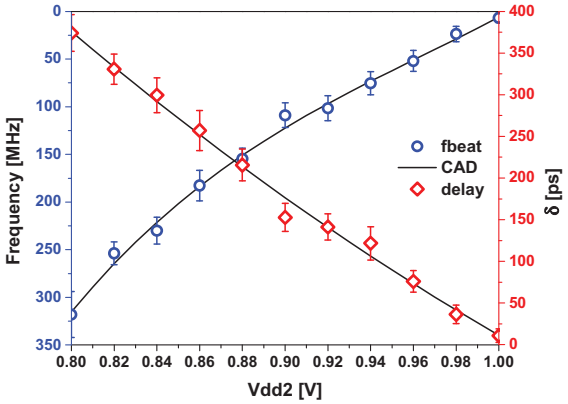

Figure 3. Measurements and simulations of the frequency (in blue) f_{beat} and the extracted delay δ (in red) with the supply voltage V_{dd2} at 25°C. A sample of 192 dice has been measured on the same wafer.

III. In-situ Monitors

The in-situ delay monitors are usually flip-flops (or latches) placed at the end of critical paths to probe the timing. Pre-error flip-flops are able to distinguish between normal and critical operation of the circuit. They are composed of a conventional

flip-flop with additional circuitry enabling it to detect Pre-errors and data transitions.

A pre-error is a warning signal that indicates that data comes too close to the rising edge of the clock at the considered flip-flop. They can be based on the duty-cycle of the clock signal or on a delay element. In the first case the low phase of the clock signal is exploited as the pre-error detection window, in the second case the detection window is the delay element. Warning information provided by Pre-error flip-flops inserted at the end of critical paths can be used for a closed-loop reliability control.

The in-situ monitors throughout this paper are based on a delay element pre-error approach. It means that they are composed of a shadow flip-flop with delayed data added in parallel to the regular flip-flop in a false path. The two flip-flop outputs are compared and a pre-error signal to predict the occurrence of timing errors is generated, as shown on **Figure 4**. We propose three approaches for the delay element: delay buffers (see **Figure 4a**), a passive element (see **Figure 4b**) and the node after the master of flip-flop (see **Figure 4c**).

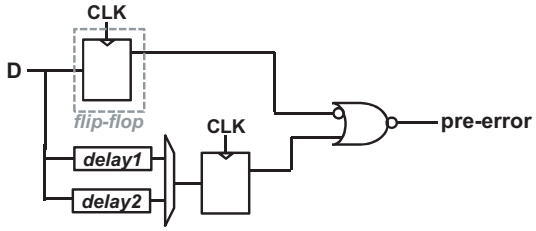

Figure 4a. Schematic of the in-situ monitor with Buffer delay.

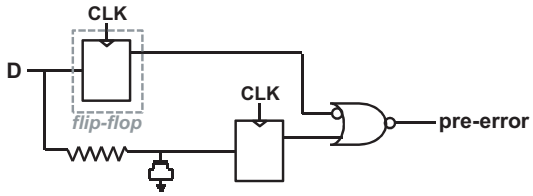

Figure 4b. Schematic of the in-situ monitor with Passive delay.

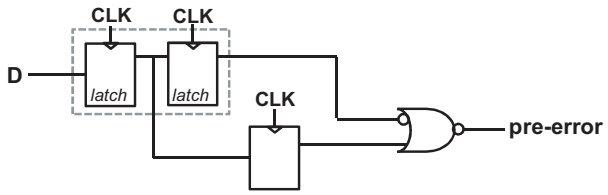

Figure 4c. Schematic of the in-situ monitor with Master delay.

If a data transition occurs close to the clock rising edge, the data in the false path that includes the additional delay will arrive at the shadow flip-flop too late so the input data will not be latched and the pre-error pulse is generated. The detection window of an in-situ monitor indicates the timing margin between a pre-error and an error in the corresponding path of a circuit. The delay element is responsible for to the length of the detection window. Furthermore for a reliability application it is important to define a detection window as accurate and robust as possible.

The detection window is obtained with the test structure by measuring the range of V_{dd2} for which the pre-error rises. A length of δ delay range corresponds to this measured V_{dd2} range. When the δ delay range of a die is calculated with the test structure characterization of this die, only the local variability of the monitors is taken into account; if it is calculated with the median of all the dies characterizations, the variability of the delay path is taken into account too.

A sample of 192 dies has been measured on the same wafer. The evolution of the detection window with the supply voltage V_{dd} is measured for the considered monitors at 25°C, as shown in **Figure 5**. The detection window length at nominal V_{dd} varies between 28ps and 48ps for the considered in-situ monitors. The monitor with Buffer delay has the strongest voltage dependence and the passive one the lowest: for respectively a deviation of the detection window equal to 46ps and 11ps at V_{dd}=0.7V.

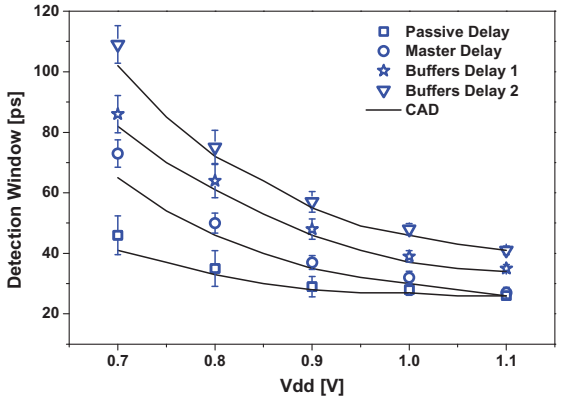

Figure 5. Measurements and simulations of the Detection Window with supply voltage for the considered monitors at 25°C.

The distributions of the detection window for the in-situ monitors with Master and Buffer delay are plotted in **Figure 6** and **Figure 7** for different V_{dd} at 25°C. The blue distributions present the variability of the in-situ monitors and the magenta ones the variability of the in-situ monitors and the delay path.

In **Figure 7**, for the monitors with Master delay the variability due to the delay path can be observed for V_{dd} lower than the nominal one. The detection window and the mismatch increase with V_{dd} decrease because of the sense effect. The standard deviations of the blue distributions for the monitor with master and buffers delay are presented in **Table I**.
The case of monitor with Buffer delay is the worst because the buffers used for the delay elements contribute to increase the variability impact and so the distribution dispersion. Monte Carlo simulations (in black) have been performed to reproduce the distributions of the detection window for both in-situ monitors for V_{dd}=0.7V and 1V at 25°C.

Standard Deviation	0.7V	0.8V	0.9V	1V	1.1V
Master delay	4.52 ps	3.31 ps	2.28 ps	1.99 ps	1.79 ps
Buffers delay	6.18 ps	5.63 ps	3.39 ps	1.87 ps	1.44 ps

Table I. Standard deviations of the distributions of the detection windows of the monitors with master delay and buffers delay at 25°C.

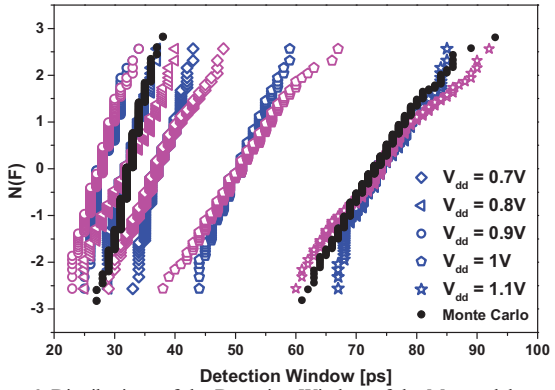

Figure 6. Distributions of the Detection Window of the Master delay monitor for different V_{dd} at 25°C considering either the variability of the monitor (in blue) or the variability of the monitor and the delay path (in magenta).

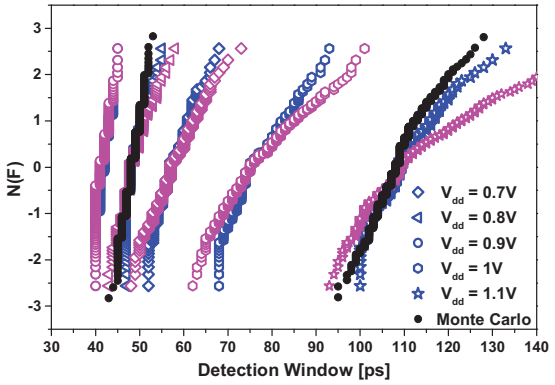

Figure 7. Distributions of the Detection Window of the Buffer delay monitor for different V_{dd} at 25°C considering either the variability of the monitor (in blue) or the variability of the monitor and the delay path (in magenta).

IV. Aging of a Delay Chain

When investigating wear-out mechanisms, we need to exacerbate degradation induced aging with accelerated stress conditions under moderate stress times. This study enables to extract behaviors and models of the degradation mechanisms. These models are used to predict aging of circuit at nominal operating conditions.

In this part, the aging of a buffer chain will be measured. The following degradation mechanisms: Bias Temperature Instability, Hot Carrier Injection and Dielectric Breakdown will be studied and quantified in term of timing degradation. To be close to normal operating conditions of a circuit, the AC-DC effects will be considered. Then the measurements of timing degradation will be projected at nominal conditions. In the last part of this paper, these results will be used to predict the timing degradation due to aging covered by the proposed in-situ monitors.

A. Degradation by BTI and HCI

The BTI degradation occurs when there is a vertical field and no carriers in the channel of a MOS transistor, unlike in hot-carrier conditions; it means that this is a static degradation mechanism. This degradation represents any physical parameters drift of a MOS transistor under a gate voltage (Negative for NBTI on PMOS device and Positive for PBTI on NMOS device) mostly at high temperature [12, 13]. Otherwise the HCI degradation occurs when a MOS device is biased under both gate and drain voltages [14, 15]. From a circuit point of view, BTI degradation comes up when the signal is high (PBTI) or low (NBTI) and HCI degradation occurs during the transitions as shown in **Figure 8** [16, 17]. Moreover the degradation by BTI and HCI are monotonic with time.

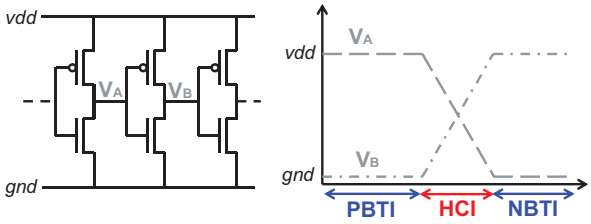

Figure 8. Schematic of an inverters path and the associated chronogram showing the degradation mechanisms at stake.

In this part, the delay buffer chain is stressed under $V_{stress1}$ at 25°C and 125°C. The buffer chain is stressed in open loop; it means that the input signal of the chain is either a signal whose frequency is selected between 2GHz, 1GHz and 500MHz, or a DC signal. The variation ΔDelay per gate induced by BTI and HCI is measured at nominal V_{dd} at different stress times. For each stress condition, 10 dies are tested and the median of all the ΔDelay per gate is plotted.

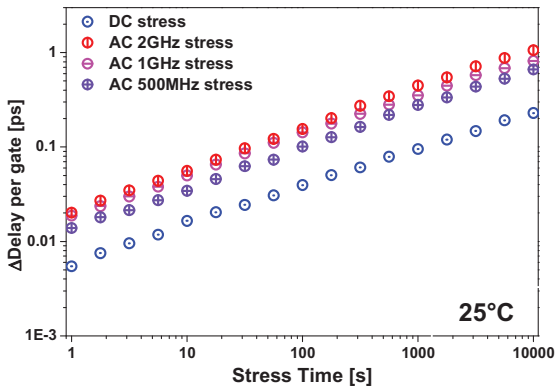

Figure 9. Measurements of the ΔDelay per gate with stress time under $V_{stress1}$ for different AC-DC stress conditions at 25°C.

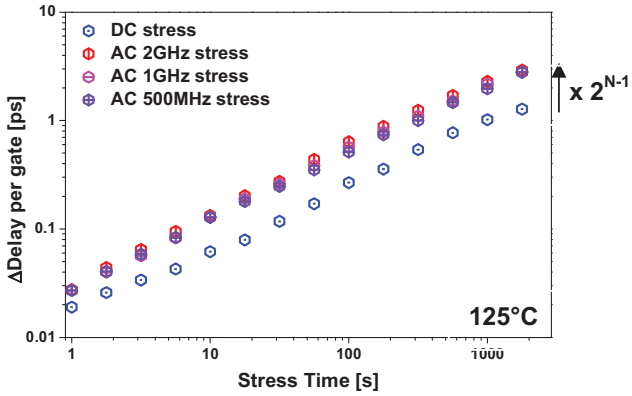

Figure 10. Measurements of the ΔDelay per gate with stress time under $V_{stress1}$ for different AC-DC stress conditions at 125°C.

The AC-DC effect is higher for 25°C temperature in **Figure 9**. Indeed the HCI mechanism is dominant at 25°C while the BTI has a small contribution. Higher the oscillation

frequency of the signal is, higher the number of transitions, and higher ΔDelay per gate are, confirming the growing role of permanent damage at high frequency with respect to the recovery component.

On the contrary the BTI mechanism is dominant at 125°C as pointed out in **Figure 10**. There is no AC effect [18, 19]: whatever the frequency of the AC stress, the induced ΔDelay per gate remains the same. This suggests that under AC stress, equal amount of permanent and recoverable BTI damage is involved, independent on the frequency in this range. The difference between AC and DC stress at 125°C is due to the fact that AC test implies that each gate is stressed during 50% time stress while DC test implies one gate out of two being stressed. In fact there is a factor 2^{N-1} (with N the time power) between the timing degradations under AC and DC stress. In other words, the impact of BTI and HCI gives 2ps at 125°C for ΔDelay per gate and between 0.1 and 0.3ps at 25°C, for a 1000s AC stress. So the BTI is the worst case of damage.

For nominal operating conditions of a circuit, the timing degradation due to aging induced by BTI and HCI is equal to roughly 0.5ps per gate for 10 years of operation knowing that the nominal delay of the used buffer is 11ps. These values are obtained from the presented data, the law extracted and the voltage and time acceleration factors.

B. Degradation by Dielectric Breakdown

When a gate voltage is applied on a MOS device, defects are generated in the oxide and at a time, called Time to Breakdown, a percolation path is created that makes the oxide conductive and resulting in a gate current increase. Consequently the Dielectric Breakdown (DB) is a sudden degradation mechanism. However DB events do not always cause a functional failure in digital circuits [20, 21].

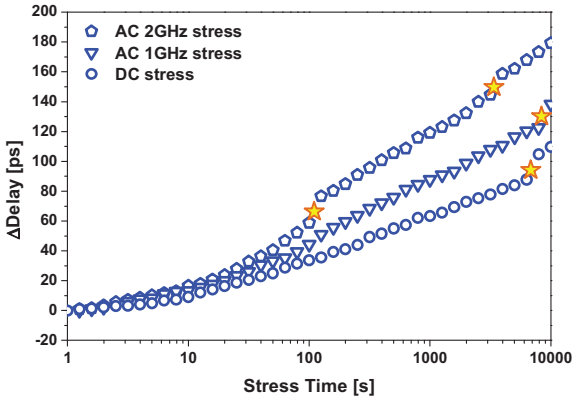

Figure 11. Measurements of the ΔDelay with stress time under $V_{stress2}$ for different AC-DC stress conditions at 125°C. Each step in the Δdelay is identified by stars related to a DB event.

This time the buffer chain is stressed under $V_{stress2}$ (>$V_{stress1}$) at 125°C to accelerate the occurrence of DB events. In **Figure 11**, the ΔDelay per gate measured at nominal V_{dd} is plotted with stressed time at 125°C. As previously shown there is degradation due to both HCI and BTI but there are also steps (highlighted by stars) that correspond to soft DB events. Consequently a DB event in a circuit comes out as a delay that suddenly increases [21, 22].

Then the buffers path is stressed at different voltages and the distributions of ΔDelay induced by DB event are plotted in **Figure 12**. The latter indicates that different stress voltage values lead to different DB severities. The stress conditions have accelerated the occurrence of DB events but have also exacerbated its impact on delay degradation. This way it seems reasonable to project the measured ΔDelay distributions at nominal V_{dd}. The method consists of extracting a law from the median of the ΔDelay distributions, enabling to project all data at V_{dd}=1V (red distribution in **Figure 12**). For one path, one DB event results in a 1.2ps additional delay, for a nominal gate delay of 11ps.

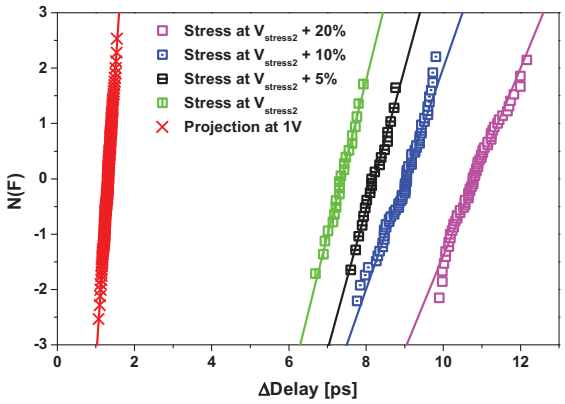

Figure 12. Distributions of the ΔDelay induced by a DB event for different stress voltages at 125°C and the projected ΔDelay (red symbols) induced by a DB event at nominal voltage.

V. Discussion

In this paper, different in-situ monitors based on delay elements also called Pre-error flip-flops have been designed, investigated and measured by means of a dedicated test structure. The detection window of the in-situ monitors with Passive delay is less deviant than the Buffer and Master delay ones with V_{dd} decrease; but using a passive element in a digital circuit is not a common choice. The in-situ monitor with Buffer delay is the easiest circuit to use and set up since it is a block composed of digital cells that can be directly connected to the data input. Moreover this in-situ monitor can be implemented as *soft* or *hard* cell: it means it can be inserted after the timing analysis or as a standard cell. The in-situ monitors presented in this paper can be used as passive design only to get information concerning the impact of aging phenomena on reliability. In the circuit operating conditions when the pre-error rises, we know that there is a time left corresponding to the detection window value before an error occurs. Considering the results from the Parts III and IV, it is possible to predict what is called local variations (transistor mismatch) or timing degradation due to aging during this time. In our case, we project both timing degradation due to BTI, HCI and DB and local variations of a data path to a 10 years use from the Part IV measurements and projections.

The **Figure 13** presents the distributions of the detection window of the in-situ monitor with Master delay and the corresponding time margins for 10 years of use considering mismatch, DB and aging due to BTI and HCI for different V_{dd}. The projected time margins increase with V_{dd} decrease because of the sense effect. We can observe that the major contribution is due to BTI/HCI aging phenomena except in the case of

larger timing window (or smaller V_{dd}) where the contribution of DB and mismatch start being significant.

Moreover the in-situ monitor detection window is increased by aging with time depending on the delay element but it may be negligible compared to the data path aging.

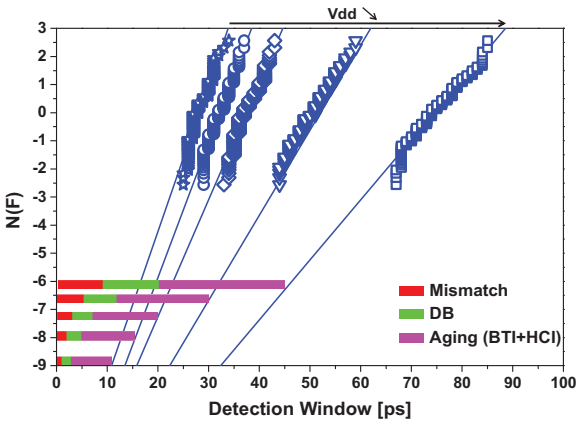

Figure 13. Distributions of the detection windows of the in-situ monitor with Master delay. The horizontal bars correspond to the covered delay variation for a 10 years use with the contributions of mismatch (in red), DB (in green) and monotonic aging (in magenta).

For each V_{dd}, the corresponding Cumulative Probability Failures (CPF) to the 10 years use induced timing degradation of the path is plotted for the three different in-situ monitors in **Figure 14**. The CPF is more V_{dd} dependent for the in-situ monitor with Buffer delay than those with Passive delay and Master delay. For nominal operating conditions, the CPF is weaker for the in-situ monitors with Buffer delay because the detection window is strongly dependent with the V_{dd}.

Once a flag rises it is possible to compensate the aging of data paths either by increasing the supply voltage or by using body bias. The latter solution is the best because it does not induce additional degradation [23].

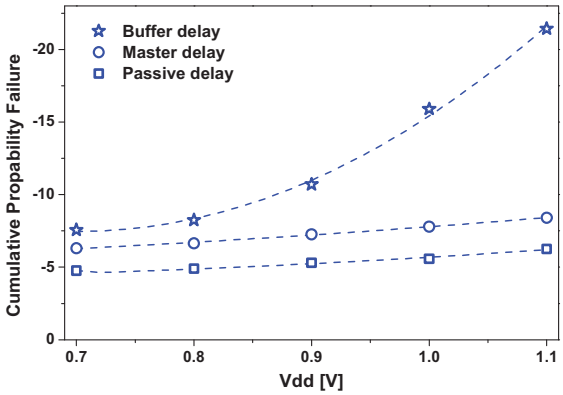

Figure 14. Evolution of the Cumulative Probability Failure of the different in-situ monitors with V_{dd} considering the timing margin for aging and mismatch.

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