Silicon Proof of the Intelligent Analog IP Design Flow for Flexible Automotive Components

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Abstract—**In this brief paper we present the successful silicon validation of the Intelligent Analog IP (IIP) design flow applied to the design of a SMART sensor IC for automotive requirements. Using a library of reconfigurable and robust analog IP we fast create parameterized cells up to high complexity levels including the corresponding layouts. This allows us (1) to overcome time-consuming handcrafted analog re-design cycles, (2) to include the effects of layout parasitics into the optimization loop, and thus (3) to fast achieve different specifications even for multiple technologies. We show that the IIP design flow leads to a strong improvement of design efficiency, silicon performance, and yield.**

Keywords—Intelligent IP; Reuse; Design Flow; Post-Layout; Optimization; Yield

I. INTRODUCTION

The market of System-on-Chip (SoC) is largely increasing due to the trend towards ever smaller, more complex and energy efficient devices. For the reason of cost and performance, analog parts are placed on the same chip being a noisy and "unfriendly" environment for those sensitive analog circuitries. Analog design is the main issue regarding time-to-marked requirements due to the complex dependencies between blocks and the lack of analog design automation [1].

Typically, the designer starts from schematic entry without any information about layout parasitics. Missing layout automation makes it necessary to estimate layout-induced parasitics. Since this estimation is not exact, either performance or power and area are wasted [2]. On the other hand, we observe that a fully automated design flow would be hardly accepted by analog designers.

Therefore, we developed a novel Intelligent IP (IIP) design flow using a hierarchical library of standard basic circuit elements up to complex circuits. These cells encapsulate expert knowledge to provide the creation of overall design data including well-suited layout structures within seconds to minutes. We used the IIP flow for high efficient design of different versions of a SMART sensor IC meeting opposing specifications for automotive and biomedical application [3]. These ASICs were measured for silicon proof of the IIP design flow benefits.

II. IIP DESIGN FLOW

The flow (see Fig. 1), based on a flexible IIP library, incorporates topology optimization (topology selection and sizing), automatic cell generation and post-layout (yield) optimization taking parasitics into account.

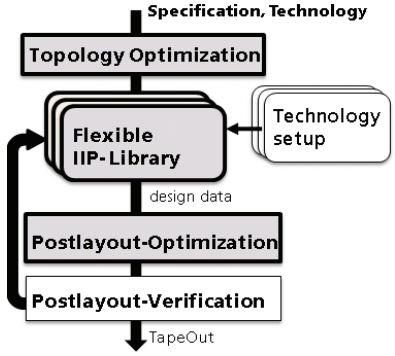

Fig. 1. IIP design flow with its three key features

A. Topology Optimization

Since analog demands have to be satisfied by a workable topology, proper choice is of fundamental importance. An appropriate topology for a particular specification is automatically selected and subsequently sized using third-party optimization tools [4], [5]. A suitable methodology to automate topology selection by using gradient-based or stochastic optimization [6] was applied here.

By reusing existing, previously characterized, and flexible IPs (multiple fixed sets of design parameters for different topologies and their simulation results), one can further speed up system design and optimization.

B. Flexible IIP Library

The Intelligent analog IP library comprises the following main aspects: (1) "Intelligent" denotes built-in expert knowledge like sizing rules [7] and matching [8], technology independence and flexibility regarding design parameters and specification (soft IP), (2) the IP includes analog circuit cells with all relevant views such as layout, schematic, symbol, and behavioral model in a static library representation, as established in hand-crafted designs, and (3) the IIP library is built hierarchically reusing lower-level IIP blocks.

The IIP description code is strictly generic related to technology. Furthermore, a deterministic and relative placement of layout blocks, based on expert knowledge, is applied ensuring correct-by-

construction layouts. Finally, layout automation features, such as automatic layout shape adaption, were developed to ensure optimized layout area.

Using the latter paradigms we developed a hierarchical IIP library up to a high complexity level of ADCs and DACs. For example, the IIP library of flexible ADCs currently contains:

- Flash (8 - 125 MS/sec, 1.3 - 11 mW, 2 - 5.8 bit ENOB),
- Pipelined (20 - 40 MS/sec, 120 - 150 mW, ≤ 9.5bit ENOB)
- Cyclic (12 - 36 kS/sec, 50 - 370 µW, 10 - 12.7 bit ENOB).

C. Postlayout (Yield) Optimization

Since every block of our design is an instance of the IIP library and is therefore automatically generated including layout view, we are able to overcome estimation of parasitics. We directly extract parasitic elements out of the generated layout and use this information for precise simulations including yield analysis and optimization (using third-party tools [4], [5]).

III. Application to Automotive IP Design

The key components of the IIP design flow allowed the fast assembly of three versions (v1, v2, v3) of our SMART sensor IC, dedicated to automotive and biomedical application. The ASIC is fabricated in an X-FAB 180 nm technology [9] and is featured by: low-power 12-bit cyclic ADC for slow signal processing and precise sensor readout, temperature sensor with ± 0.8 °C accuracy for T = -40 … 125 °C, high-ohmic (>1 GΩ) differential frontend for biomedical high sensitive measurements, and an ambient light sensor.

Each version of the IC includes a different ADC for various specifications. A valid topology of an operational amplifier, the key component of the ADC, is automatically selected by *topology optimization*. Thus, we reduced initial effort and additionally, we added new parameter sets to the IIP library.

IV. Results

Compared to hand-crafted design, we easily optimized sizing including parasitics by fast re-generation of the ADC layout. We could prove the reduction of design effort by applying *flexible IIP library* components in combination with *postlayout optimization* in our productive design projects: for the particular designs considered here, we reduced the design effort by 30%. The *postlayout-optimization* helped us avoiding inefficient overmargin design. The optimization result could be proven to be close to silicon performance: The discrepancy of INL error between postlayout verification and measurement was below 0.5 bit. The predicted close-to-silicon yield was increased to automotive requirements (-40 to 125 °C) by using *postlayout yield optimization* (see Fig. 3). One measured FFT spectrum of chip v3 is given in Fig. 2. All key measurement results are shown in Table 1.

V. Conclusion

Using the Intelligent IP design flow we significantly improve design efficiency and robustness for automotive mixed-signal ICs – we presented the silicon prove for low-power 12-bit ADC SMART sensor ICs for multiple opposite specifications. A reduction of design effort by 30 %, yield improvement, and fast adaption of circuit performance were achieved. Future designs will benefit even more from this IIP design flow since an increasing library will be applicable to a larger number of circuits and various technologies.

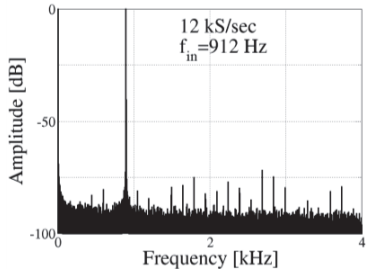

Fig. 2. FFT spectrum (input signal 912 Hz, 1.5 V_{pp}, device IC v3)

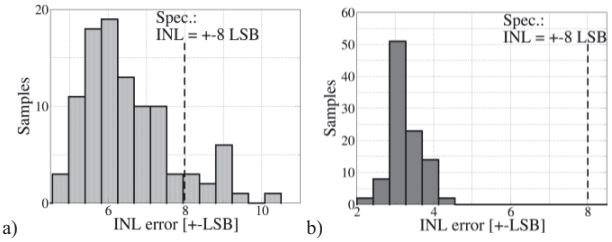

Fig. 3. Yield optimization for T = - 40 ... 125 °C, confidence level = 95 %
a) Handcrafted, Yield = 78 %, Sigma-To-Target = 1.2
b) IIP design flow, Yield = 96 %, Sigma-To-Target = 11.4

TABLE 1. IP Features low-power ADCs, T = - 40 … 125 °C

Device type	**Key measures** (2.4V Supply, worst case)					
	Rate [kS/s]	*Power [mW]*	*ENOB [bit]*	*SFDR [dB]*	*Si area [mm²]*	*Design effort reduction [%]*
Handcrafted	12	0,28	11.0	58,0	0,3	0
IC v1	24	0,18	12.7	68,0	0,3	-30%
IC v2	12	0,05	12.7	68,0	0,3	-30%
IC v3	40	0,37	11.9	72,0	0,3	-30%

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